

DATA SHEET

74F273A Octal D flip-flop

Product specification

1996 Mar 12

IC15 Data Handbook

Octal D flip-flop

74F273A

FEATURES

- High impedance inputs for reduced loading (20µA in Low and High states)
- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- See 74F377A for clock enable version
- See 74F373 for transparent latch version
- See 74F374 for 3-State version

DESCRIPTION

The 74F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{\text{MR}}$ are common to all elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F273A	170MHz	25mA

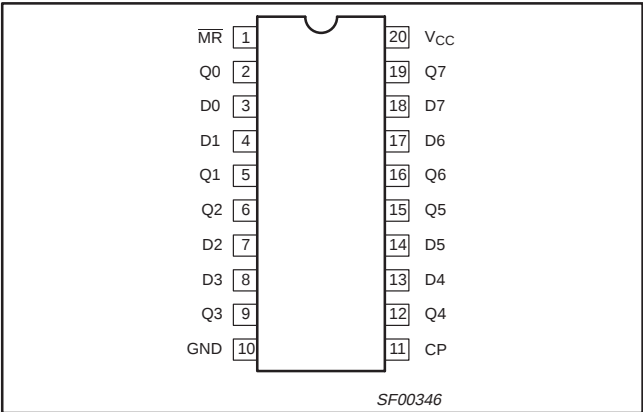
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$; $T_{\text{amb}} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	PKG. DWG. #
20-pin plastic DIP	74F273AN	SOT146-1
20-pin plastic SOL	74F273AD	SOT163-1

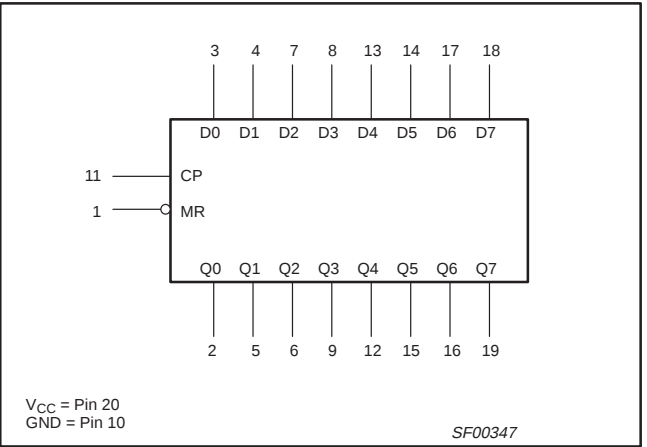
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/0.033	20µA/20µA
$\overline{\text{MR}}$	Master Reset input (active-Low)	1.0/0.033	20µA/20µA
CP	Clock pulse input (active rising edge)	1.0/0.033	20µA/20µA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

PIN CONFIGURATION



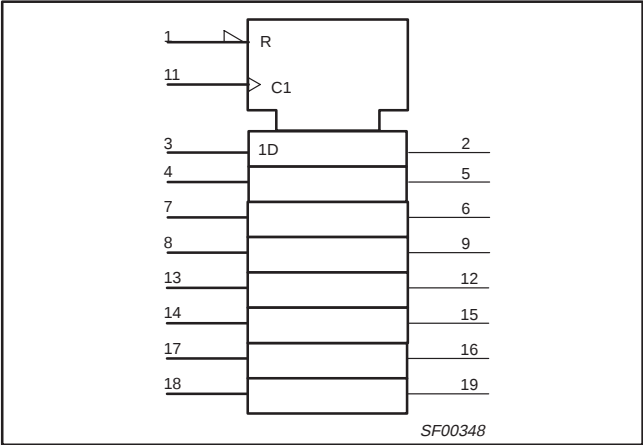
LOGIC SYMBOL



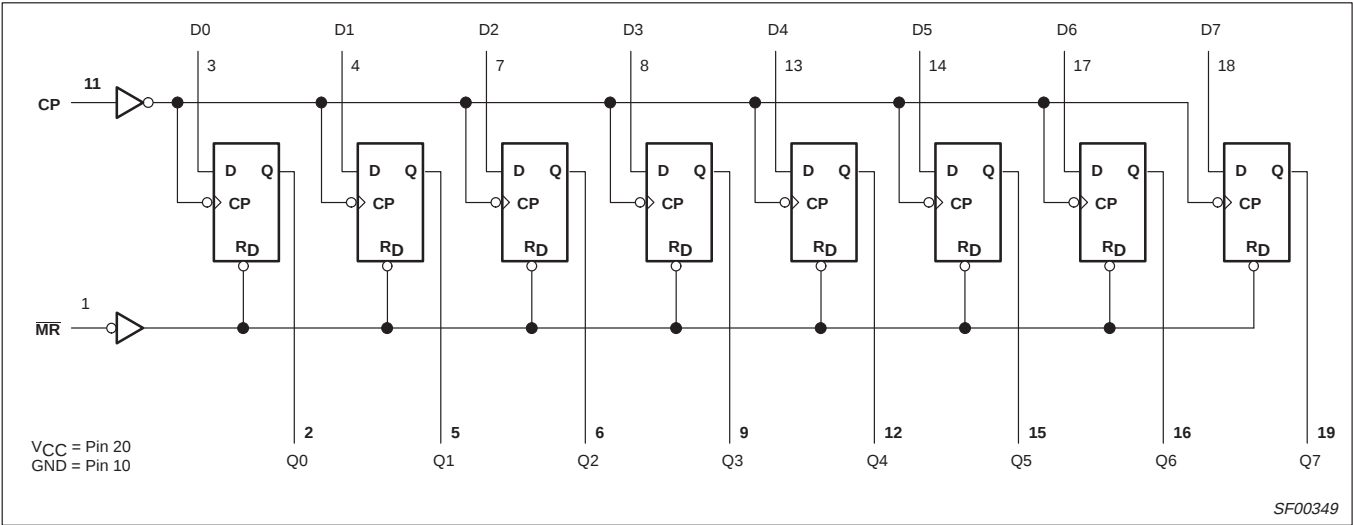
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LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	Dn	Q0 – Q7	
L	X	X	L	Reset (clear)
H	$\uparrow$	h	H	Load "1"
H	$\uparrow$	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
 $\uparrow$ = Low-to-High clock transition

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT
				MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	MR & CP inputs	V _{CC} = MIN, V _{IL} = 0.0V ³ , V _{IH} = 4.5V ³ , I _{OH} = MAX	±10%V _{CC}	2.5		V
				±5%V _{CC}	2.7	3.4	V
		other inputs	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.5		V
				±5%V _{CC}	2.7	3.4	V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}		0.30	V
				±5%V _{CC}		0.30	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}		-0.73	-1.2	V
I _I	Input current at maximum input voltage		V _{CC} = 0.0V, V _I = 7.0V			100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V			-20	μA
I _{OS}	Short-circuit output current ⁴		V _{CC} = MAX	-60		-150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX		24	38	mA
		I _{CCL}			27	43	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- To reduce the effect of external noise during test.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS FOR 'F273A

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ±10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	150	170		125		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Qn	1	3.5 5.0	5.0 7.0	8.0 9.5	3.0 4.5	9.0 10.0	ns
t _{PHL}	Propagation delay MR to Qn	2	5.0	7.0	9.0	5.0	9.5	ns

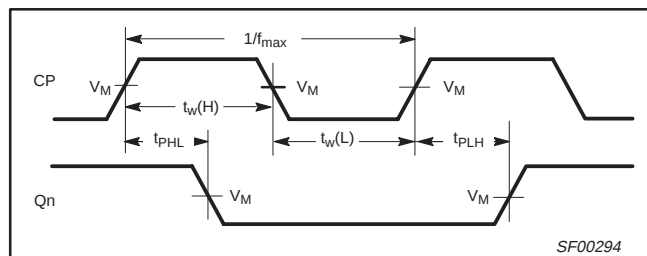
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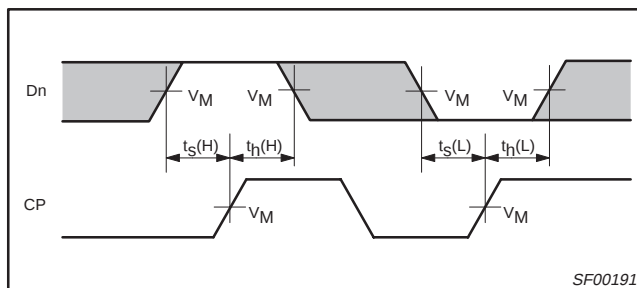
AC SETUP REQUIREMENTS FOR 'F273A

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ±10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low Dn to CP	3	3.0 2.0			2.5 2.5		
t _h (H) t _h (L)	Hold time, High or Low Dn to CP	3	0.5 0.0			2.5 1.0		ns
t _w (H) t _w (L)	Clock pulse width High or Low	1	4.5 3.5			5.0 4.0		ns
t _w (L)	Master Reset pulse width, Low	2	3.0			3.5		ns
t _{REC}	Recovery time MR to CP	2	4.0			5.0		ns

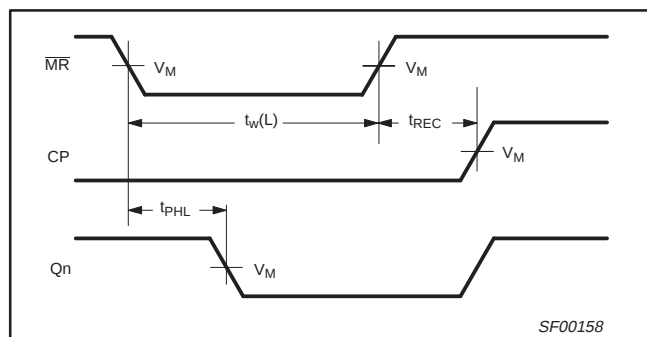
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. Data Setup and Hold Times



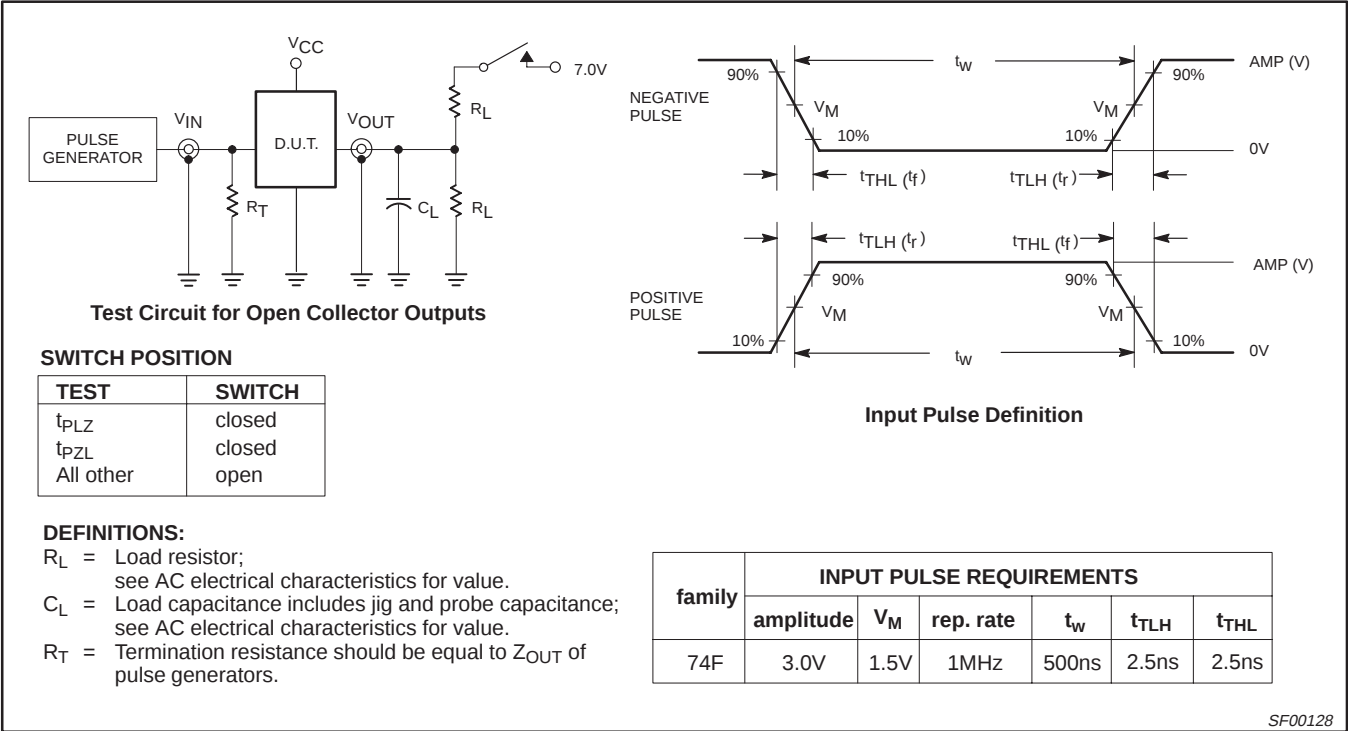
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5\text{V}$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORMS



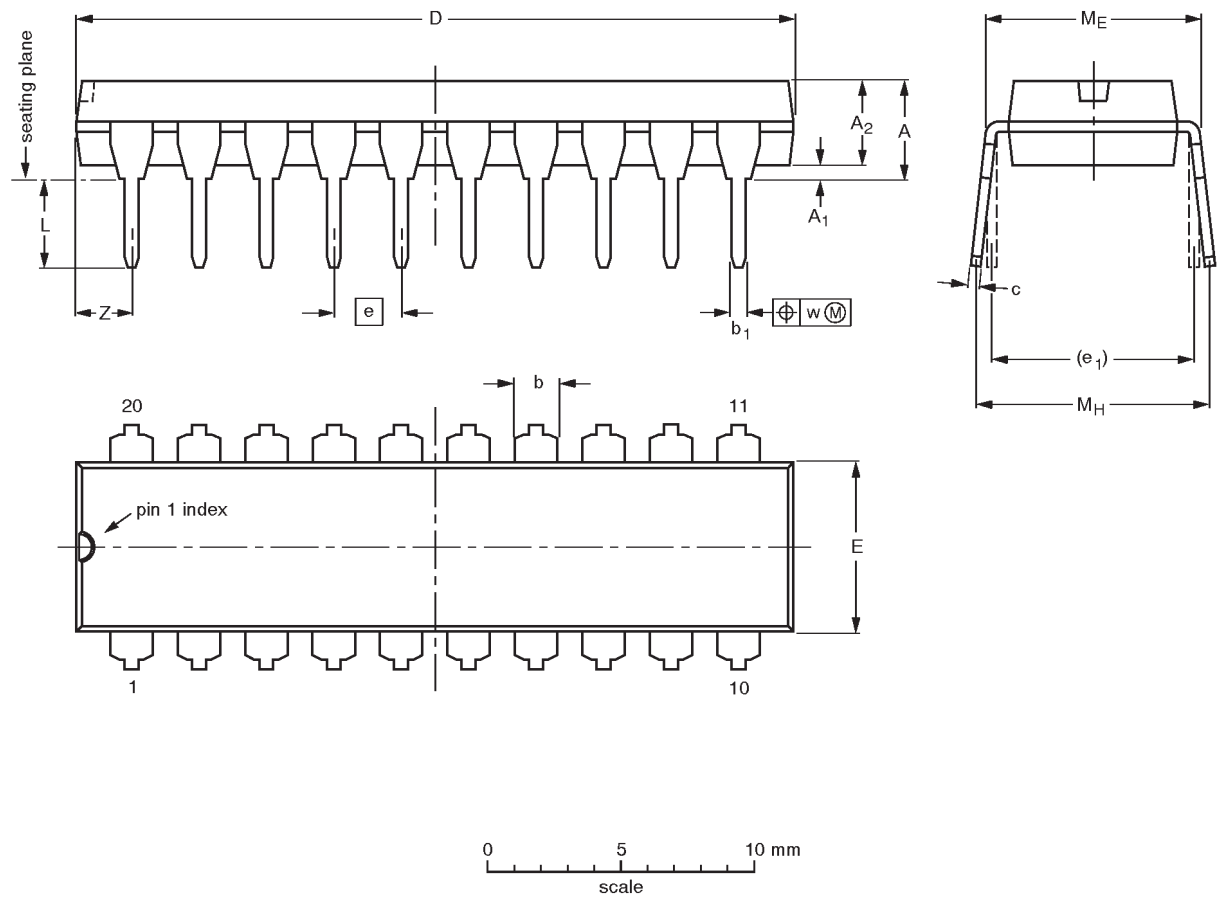
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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

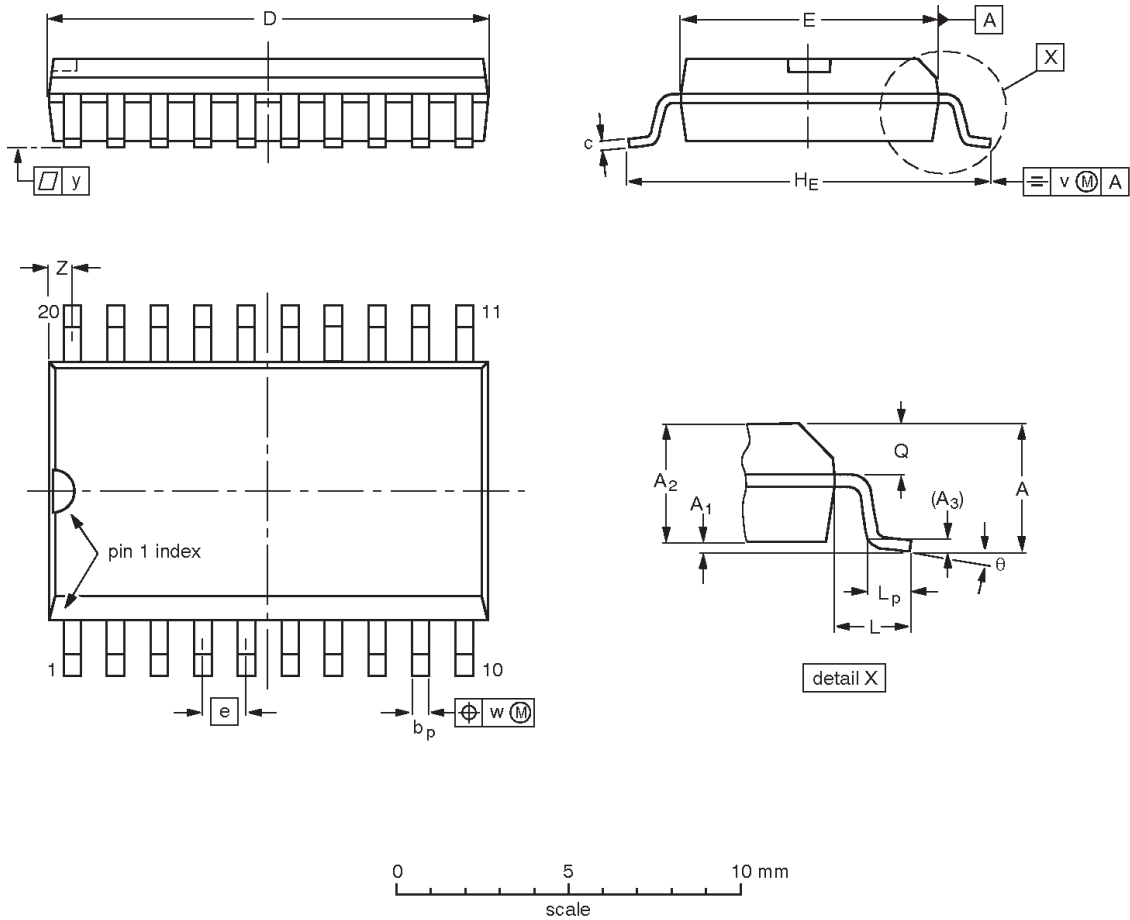
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				-95-01-24 97-05-22

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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74F273A; Octal D flip-flop

General description	Features	Applications	Datasheet
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General description

The 74F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the MR input. The device is useful for applications where the true output only is required and the CP and MR are common to all elements.

Features

- High impedance inputs for reduced loading (20μA in Low and High states)
- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- See 74F377A for clock enable version
- See 74F373 for transparent latch version
- See 74F374 for 3-State version

Applications

AN202_1: Testing and specifying FAST logic (date 01-Jun-87)

Doc AN2021_1: Thermal considerations for FAST logic products (date 13-Mar-95)

~~Doc~~ AN203_2: Test Fixtures for High Speed Logic (date 02-Apr-98)

AN216_2: Arbitration in shared resource systems (date 18-Jul-88)

Datasheet

<u>Type number</u>	<u>Title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>	<u>File size (kB)</u>	<u>Datasheet</u>
74F273A	Octal D flip-flop	3/12/1996	Product specification	10	89	 Download

Blockdiagram(s)

Block diagram of N74F273AD

Parametrics

<u>Type number</u>	<u>Package</u>	<u>Description</u>	<u>Propagation Delay(ns)</u>	<u>Voltage</u>	<u>No. of Pins</u>	<u>Power Dissipation Considerations</u>	<u>Logic Switching Levels</u>	<u>Output Drive Capability</u>
N74F273AD	SOT163 (SO20)	D-Type Flip-Flop with Reset; Positive-Edge Trigger	6~10	5 Volts +	20	None	TTL	Low
N74F273AN	SOT146-1 (DIP20)	D-Type Flip-Flop with Reset; Positive-Edge Trigger	6~10	5 Volts +	20	None	TTL	Low

Products, packages, availability and ordering

<u>Type number</u>	<u>North American type number</u>	<u>Ordering code (12NC)</u>	<u>Marking/Packing</u>  IC packing info	<u>Package</u>	<u>Device status</u>	<u>Buy online</u>
N74F273AD	N74F273AD	9350 535 60602	Standard Marking * Tube (Signetics)	SOT163 (SO20)	Full production	 order this 
	N74F273AD-T	9350 535 60623	Standard Marking * Reel Pack, SMD, 13" (Signetics)	SOT163 (SO20)	Full production	 order this 
N74F273AN	N74F273AN	9350 535 70602	Standard Marking * Tube (Signetics)	SOT146-1 (DIP20)	Full production	 order this 

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