

# MSD1819A-RT1

Preferred Device

## General Purpose Amplifier Transistor

### NPN Silicon Surface Mount

This NPN Silicon Epitaxial Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC-70/SOT-323 package which is designed for low power surface mount applications.

#### Features

- High  $h_{FE}$ , 210–460
- Low  $V_{CE(sat)}$ ,  $< 0.5$  V
- Moisture Sensitivity Level 1
- ESD Protection: Human Body Model  $> 4000$  V  
Machine Model  $> 400$  V
- Pb-Free Package is Available

#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	60	Vdc
Collector-Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current – Continuous	$I_C$	100	mA <sub>dc</sub>
Collector Current – Peak	$I_{C(P)}$	200	mA <sub>dc</sub>

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation (Note 1)	$P_D$	150	mW
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	–55 to +150	$^\circ\text{C}$

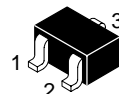
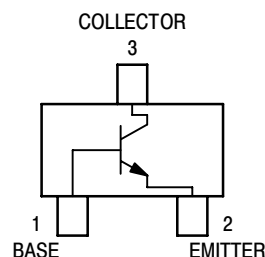
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.



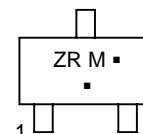
ON Semiconductor®

<http://onsemi.com>



SC-70 (SOT-323)  
CASE 419  
STYLE 3

#### MARKING DIAGRAM



ZR = Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)  
\*Date Code orientation may vary depending upon manufacturing location.

#### ORDERING INFORMATION

Device	Package	Shipping†
MSD1819A-RT1	SC-70/ SOT-323	3000/Tape & Reel
MSD1819A-RT1G	SC-70/ SOT-323 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage ( $I_C = 2.0 \text{ mAdc}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	–	Vdc
Collector-Base Breakdown Voltage ( $I_C = 10 \text{ } \mu\text{Adc}$ , $I_E = 0$ )	$V_{(BR)CBO}$	60	–	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 10 \text{ } \mu\text{Adc}$ , $I_C = 0$ )	$V_{(BR)EBO}$	7.0	–	Vdc
Collector-Base Cutoff Current ( $V_{CB} = 20 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	0.1	$\mu\text{A}$
Collector-Emitter Cutoff Current ( $V_{CE} = 10 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	0.1	$\mu\text{A}$
DC Current Gain (Note 2) ( $V_{CE} = 10 \text{ Vdc}$ , $I_C = 2.0 \text{ mAdc}$ ) ( $V_{CE} = 2.0 \text{ Vdc}$ , $I_C = 100 \text{ mAdc}$ )	$h_{FE1}$ $h_{FE2}$	210 90	340 –	–
Collector-Emitter Saturation Voltage (Note 2) ( $I_C = 100 \text{ mAdc}$ , $I_B = 10 \text{ mAdc}$ )	$V_{CE(sat)}$	–	0.5	Vdc

2. Pulse Test: Pulse Width  $\leq 300 \text{ } \mu\text{s}$ , D.C.  $\leq 2\%$ .

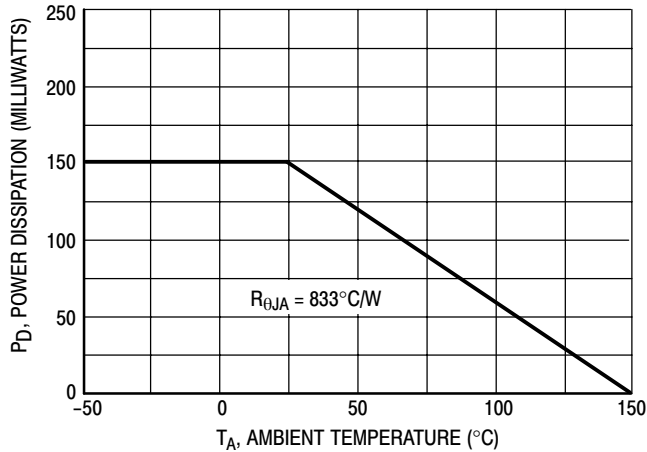


Figure 1. Derating Curve

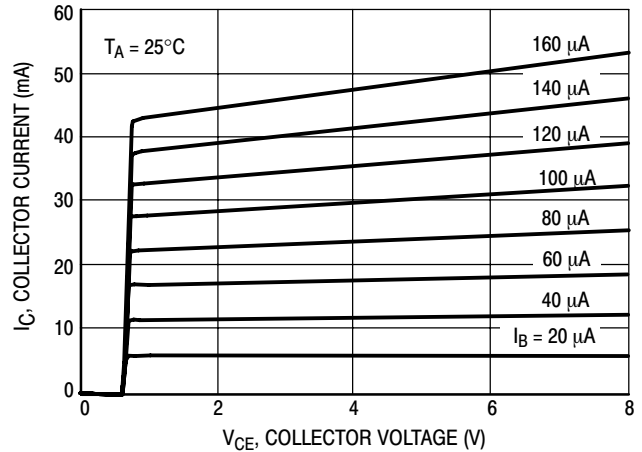
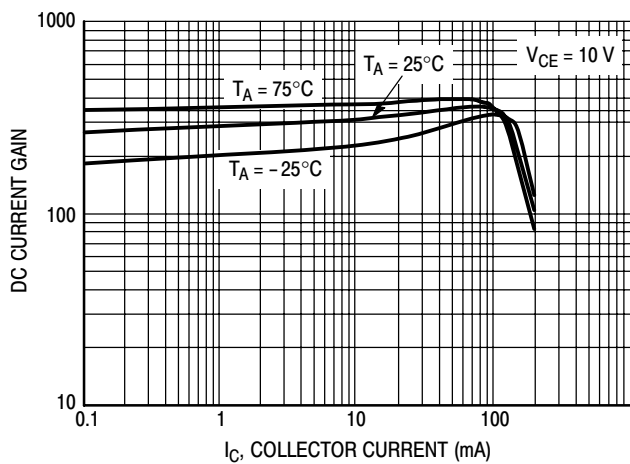
Figure 2.  $I_C - V_{CE}$ 

Figure 3. DC Current Gain

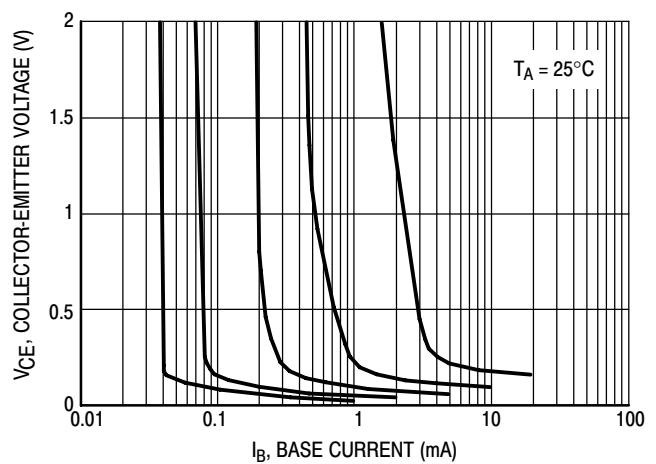


Figure 4. Collector Saturation Region

## MSD1819A-RT1

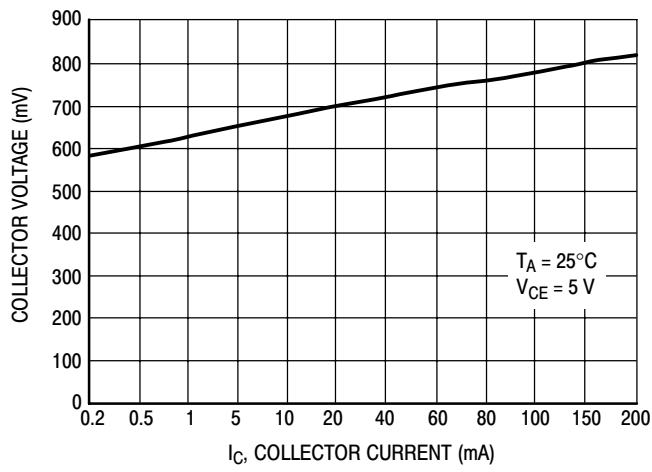


Figure 5. On Voltage

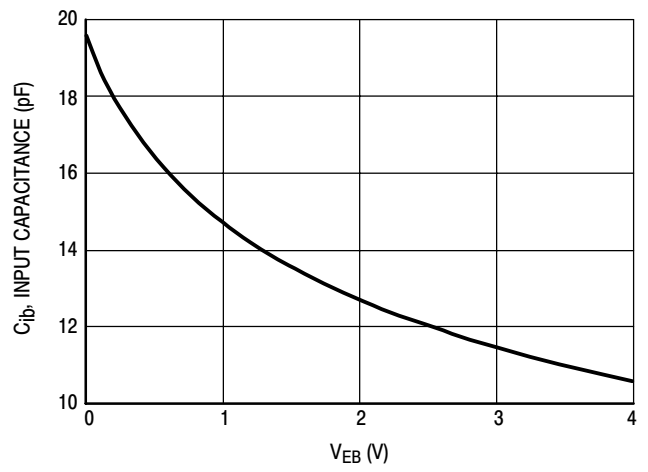


Figure 6. Capacitance

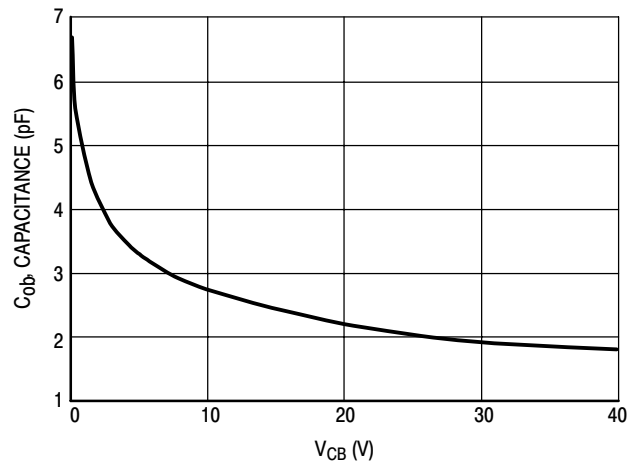
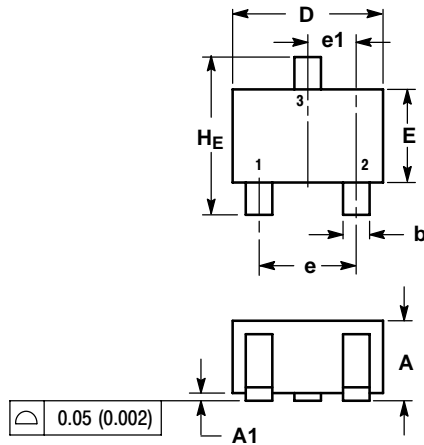


Figure 7. Capacitance

# MSD1819A-RT1

## PACKAGE DIMENSIONS

### SC-70 (SOT-323) CASE 419-04 ISSUE M

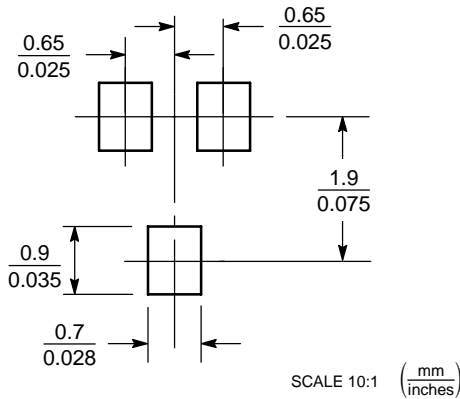


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.


DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.7 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.425 REF			0.017 REF		
HE	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 3:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.