

# LM4816 Boomer® Audio Power Amplifier Series 1W Stereo Audio Amplifier

# + Adjustable Output Limiter

Check for Samples: LM4816

#### **FEATURES**

- Stereo BTL Amplifier
- Adjustable Output Voltage Magnitude Limiter
- "Click and Pop" Suppression Circuitry
- Unity-Gain Stable Audio Amplifiers
- Thermal Shutdown Protection Circuitry
- TSSOP (PW) Package

#### **APPLICATIONS**

- Notebook Computers
- Multimedia Monitors
- Desktop Computers
- Portable Televisions

## **KEY SPECIFICATIONS**

- P<sub>OUT</sub> (BTL): V<sub>DD</sub> = 5V, THD = 1%, R<sub>L</sub> = 8Ω 1.0W (typ)
- Power Supply Range 3.0V to 5.5V
- Limiter Adjustment Range GND to V<sub>DD</sub>/2
- Shutdown Current 0.06µA (typ)

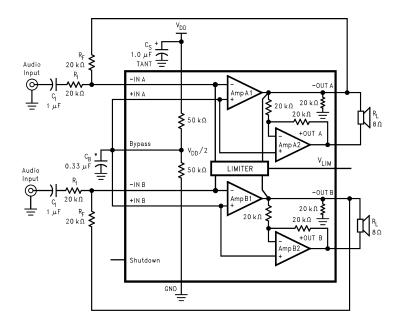
# **Typical Application**

#### DESCRIPTION

The LM4816 combines a bridged-connected (BTL) stereo audio power amplifier with an adjustable output voltage magnitude limiter. The audio amplifier delivers 1.0W to an  $8\Omega$  load with less than 1.0% THD+N while operating on a 5V power supply. With  $V_{LIM}$  set to 1.0V, the amplifier outputs are clamped to  $6V_{D-D}$ ,  $\pm 800$ mV.

The LM4816 features an external controlled micropower shutdown mode and thermal shutdown protection. It also utilizes circuitry that reduces "clicks and pops" during device turn-on and return from shutdown.

Boomer<sup>™</sup> audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.



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## **Connection Diagram**

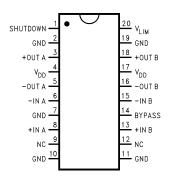


Figure 1. TSSOP - Top View See Package Number PW



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# **Absolute Maximum Ratings**(1)(2)

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Supply Voltage			6.0V	
Storage Temperature		−65°C to +150°C		
Input Voltage		-0.3V to V <sub>DD</sub> +0.3V		
Power Dissipation (3)		Internally limited		
ESD Susceptibility <sup>(4)</sup>		2000V		
ESD Susceptibility <sup>(5)</sup>		200\		
Junction Temperature			150°C	
Solder Information	Small Outline Deckers	Vapor Phase (60 sec.)	215°C	
Solder information	Small Outline Package	Infrared (15 sec.)	220°C	
See the AN-450 Application	on Report for other methods of sol	dering surface mount devices.		
Thermal Resistance	θ <sub>JC</sub> (typ)—PW		20°C/W	
Thermal Resistance	θ <sub>JA</sub> (typ)—PW		80°C/W	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) The maximum power dissipation is dictated by T<sub>JMAX</sub>, θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub> and must be derated at elevated temperatures. The maximum allowable power dissipation is P<sub>DMAX</sub> = (T<sub>JMAX</sub> T<sub>A</sub>)/θ<sub>JA</sub>. For the LM4816, T<sub>JMAX</sub> = 150°C. For the θ<sub>JA</sub>s for different packages, please see the Application Information section or the Absolute Maximum Ratings section.
- (4) Human body model, 100pF discharged through a  $1.5k\Omega$  resistor.
- (5) Machine model, 220pF–240pF discharged through all pins.

## **Operating Ratings**

Temperature Range $(T_{MIN} \le T_A \le T_{MAX})$	-40°C ≤ T <sub>A</sub> ≤ 85°C
Supply Voltage	$3.0V \le V_{DD} \le 5.5V$

Product Folder Links: LM4816



# Electrical Characteristics (1)(2)

The following specifications apply for  $V_{DD}$ = 5V unless otherwise specified. Limits apply for  $T_A$ = 25°C.

Symbol	Parameter	Conditions	LM4	816	Units
			Typical <sup>(3)</sup>	Limit <sup>(4)</sup>	(Limits)
V <sub>DD</sub>	Supply Voltage			3.0	V (min)
				5.5	V (max)
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V, I_{O} = 0A^{(5)}$	9.0	15 5	mA (max) mA (min)
I <sub>SD</sub>	Shutdown Current	V <sub>DD</sub> applied to the SHUTDOWN pin	0.06	2	μA (min)
V <sub>IH</sub>	Shutdown Logic High Input Threshold Voltage			3.0	V (min)
V <sub>IL</sub>	Shutdown Logic Low Input Threshold Voltage			1.8	V (max)
Vos	Output Offset Voltage	V <sub>IN</sub> = 0V	5	50	mV (max)
_	Output Power <sup>(6)</sup>	THD+N = 1%, f = 1kHz, $R_L = 8\Omega$	1.0	0.9	W (min)
Po	Output Power (**)	THD+N = 10%, f = 1kHz, $R_L = 8\Omega$	1.5		W
THD+N	Total Harmonic Distortion +	20Hz ≤ f ≤ 20kHz, A <sub>VD</sub> = 2	0.03		%
I UD+N	Noise	$R_L = 8\Omega$ , $P_O = 400$ mW	0.03		%
V <sub>LIM</sub>	Limiter Clamp Voltage	$V_{LIM} = 1.0V, R_L = \infty, V_{IN} = 4V_{P-P}$ $V_{O P-P} = (V_{OUT+} - V_{OUT-})$	6.0	5.2 6.8	V <sub>P-P</sub> (min) V <sub>P-P</sub> (max)
PSRR	Power Supply Rejection ratio	$\begin{aligned} &V_{DD} = 5\text{V}, \ V_{RIPPLE} = 200\text{V}_{RMS} \\ &R_L = 8\Omega, \ C_B = 1.0\mu\text{F} \\ &\text{Inputs Floating} \\ &\text{Inputs terminated with } 10\Omega \end{aligned}$	67 43		dB dB
X <sub>TALK</sub>	Channel Separation	$f = 1kHz$ , $C_B = 1.0\mu F$	90		dB
SNR	Signal to Noise Ratio	$V_{DD} = 5V, P_{O} = 1.0W, R_{L} = 8\Omega$	98		dB

<sup>(1)</sup> Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

- (2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
- (3) Typicals are measured at 25°C and represent the parametric norm.
- (4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
- (5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
- (6) Output power is measured at the device terminals.

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# **Typical Performance Characteristics**

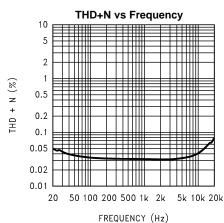
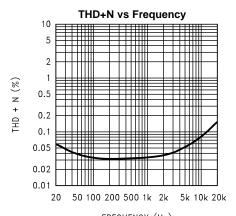


Figure 2.  $V_{DD} = 5V$ ,  $R_L = 8\Omega$ ,  $P_{OUT} = 150$ mW



FREQUENCY (Hz) Figure 4.  $V_{DD}$  = 3V,  $R_L$  = 8 $\Omega$ ,  $P_{OUT}$  = 150mW

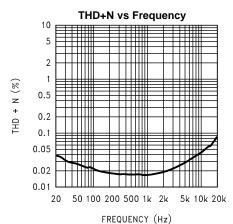


Figure 6.  $V_{DD} = 5.5V$ ,  $R_L = 8\Omega$ ,  $P_{OUT} = 150mW$ 

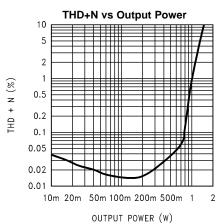


Figure 3.  $V_{DD} = 5V$ ,  $R_L = 8\Omega$ ,  $f_{IN} = 1kHz$ 

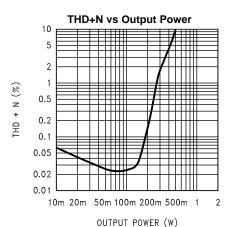


Figure 5.  $V_{DD} = 3V$ ,  $R_L = 8\Omega$ ,  $f_{IN} = 1$ kHz

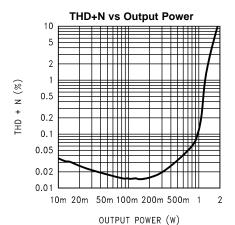
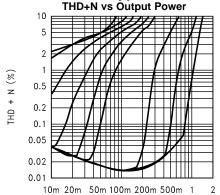


Figure 7.  $V_{DD}$  = 5.5V,  $R_L$  =  $8\Omega$ ,  $f_{IN}$  = 1kHz







OUTPUT POWER (W)

Figure 8.  $V_{DD} = 5V$ ,  $R_L = 8\Omega$ ,  $f_{IN} = 1kHz$ , at (from left to right at 7% THD+N):  $V_{LIM} = 2V$ , 1.9V, 1.8V, 1.7V, 1.6V, 1.5V, 1.0V, 0.5V, 0V

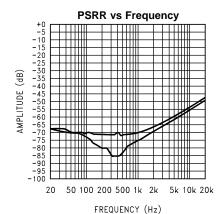
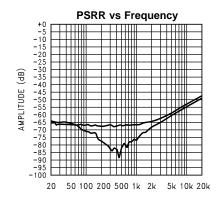


Figure 10.  $V_{DD}$  = 5V,  $R_L$  = 8 $\Omega$ ,  $R_{SOURCE}$  =  $\infty$ ,  $V_{RIPPLE}$  = 200m $V_{P-P}$ , at (from top to bottom at 500Hz):  $C_{BYPASS}$  = 0.1 $\mu$ F,  $C_{BYPASS}$  = 1.0 $\mu$ F



FREQUENCY (Hz) Figure 12.  $V_{DD}=3V,\,R_L=8\Omega,\,R_{SOURCE}=\infty,\,V_{RIPPLE}=200mV_{P-P},\,at$  (from top to bottom at 500Hz):  $C_{BYPASS}=0.1\mu F,\,C_{BYPASS}=1.0\mu F$ 

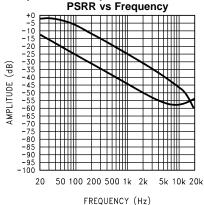
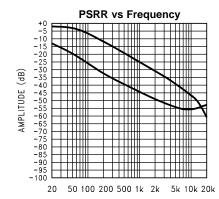
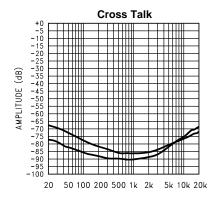


Figure 9.  $V_{DD}$  = 5V,  $R_L$  = 8 $\Omega$ ,  $R_{SOURCE}$  = 10 $\Omega$ ,  $V_{RIPPLE}$  = 200m $V_{P-P}$ , at (from top to bottom at 500Hz):  $C_{BYPASS}$  = 0.1 $\mu$ F,  $C_{BYPASS}$  = 1.0 $\mu$ F



FREQUENCY (Hz)

Figure 11.  $V_{DD}$  = 3V,  $R_L$  = 8 $\Omega$ ,  $R_{SOURCE}$  = 10 $\Omega$ ,  $V_{RIPPLE}$  = 200mVP-P, at (from top to bottom at 500Hz):  $C_{BYPASS}$  = 0.1 $\mu$ F,  $C_{BYPASS}$  = 1.0 $\mu$ F



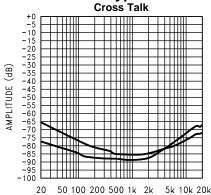
 ${\tt FREQUENCY}~({\tt Hz})$ 

Figure 13. V<sub>DD</sub> = 5V, R<sub>L</sub> = 8Ω, P<sub>OUT</sub> = 150mW, at (from top to bottom at 2kHz):

-N A driven, V<sub>OUTB</sub> measured;
-N B driven, V<sub>OUTA</sub> measured



## **Typical Performance Characteristics (continued)**



FREQUENCY (Hz) Figure 14.  $V_{DD} = 3V$ ,  $R_L = 8\Omega$ ,  $P_{OUT} = 150$ mW, at (from top to bottom at 2kHz):

-N A driven,  $V_{OUTB}$  measured;

-N B driven,  $V_{OUTA}$  measured

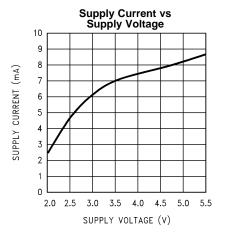


Figure 16.  $R_L = 8\Omega$ ,  $V_{IN} = 0V$  $R_{SOURCE} = 50\Omega$ 

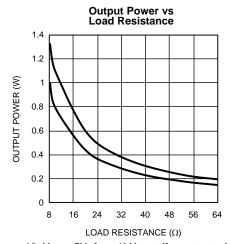
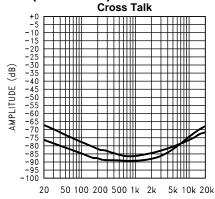


Figure 18.  $V_{DD}$  = 5V,  $f_{IN}$  = 1kHz, at (from top to bottom at 32 $\Omega$ ): THD+N = 10%, THD+N = 1%



FREQUENCY (Hz) Figure 15.  $V_{DD}$  = 5.5V,  $R_L$  = 8 $\Omega$ ,  $P_{OUT}$  = 150mW, at (from top to bottom at 2kHz):

-N A driven,  $V_{OUTB}$  measured;
-N B driven,  $V_{OUTA}$  measured

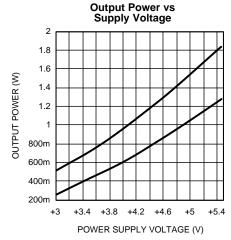


Figure 17. R<sub>L</sub> =  $8\Omega$ ,  $f_{IN}$  = 1kHz, at (from top to bottom at 4.6V): THD+N = 10%, THD+N = 1%

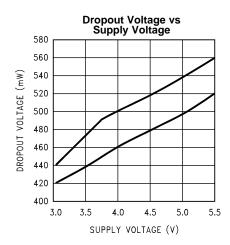


Figure 19.  $R_L = 8\Omega$ ,  $f_{IN} = 1 kHz$ , at (from top to bottom at 4.5V): positive signal swing, negative signal swing



# **Typical Performance Characteristics (continued)**

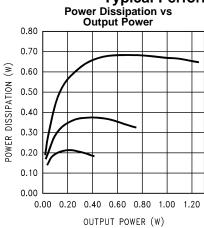


Figure 20.  $V_{DD}$  = 5V,  $f_{IN}$  = 1kHz, at (from top to bottom at 0.20W):  $R_L$  =  $8\Omega$ ,  $16\Omega$ ,  $32\Omega$ 

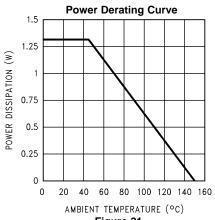
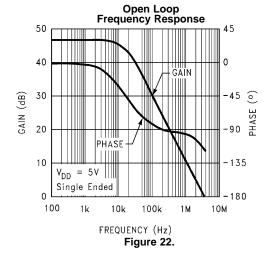


Figure 21.



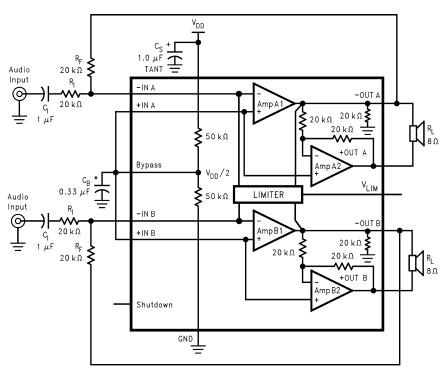


# **External Components Description**

(Refer to Figure 23.)

Components		Functional Description								
1.	R <sub>i</sub>	The Inverting input resistance, along with $R_f$ , set the closed-loop gain. $R_i$ , along with $C_i$ , form a high pass filter with $f_c = 1/(2\pi R_i C_i)$ .								
2.	C <sub>i</sub>	The input coupling capacitor blocks DC voltage at the amplifier's input terminals. $C_i$ , along with $R_i$ , create a highpass filter with $f_c = 1/(2\pi R_i C_i)$ . Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS, for an explanation of determining the value of $C_i$ .								
3.	$R_f$	The feedback resistance, along with R <sub>i</sub> , set the closed-loop gain.								
4.	Cs	The supply bypass capacitor. Refer to the POWER SUPPLY BYPASSING section for information about properly placing, and selecting the value of, this capacitor.								
5.	C <sub>B</sub>	The capacitor, C <sub>B</sub> , filters the half-supply voltage present on the BYPASS pin. Refer to the SELECTING PROPER EXTERNAL COMPONENTS section for information concerning proper placement and selecting C <sub>B</sub> 's value.								

#### **APPLICATION INFORMATION**



<sup>\*</sup> Refer to the section SELECTING PROPER EXTERNAL COMPONENTS, for a detailed discussion of C<sub>B</sub> size. Pin out shown for the WSON package. Refer to the Connection Diagram for the pinout of the TSSOP package.

Figure 23. Typical Audio Amplifier Application Circuit

### **BRIDGE CONFIGURATION EXPLANATION**

As shown in Figure 23, the LM4816 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors  $R_f$  and  $R_i$  set the closed-loop gain of Amp1A, whereas two internal  $20k\Omega$  resistors set Amp2A's gain at -1. The LM4816 drives a load, such as a speaker, connected between the two amplifier outputs, -OUTA and +OUTA.



Figure 23 shows that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between -OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 \times (R_f / R_i) \tag{1}$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the AUDIO POWER AMPLIFIER DESIGN section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

### **POWER DISSIPATION**

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended}$$
 (2)

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4816 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and an  $8\Omega$  load, the maximum single channel power dissipation is 0.633W or 1.27W for stereo operation.

$$P_{DMAX} = 4 \times (V_{DD})^2 / (2\pi^2 R_1) \text{ Bridge Mode}$$
(3)

The LM4816's power dissipation is twice that given by Equation 2 or Equation 3 when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA}$$
(4)

The LM4816's  $T_{JMAX}$  = 150°C. In the PW (TSSOP) package, the LM4816's  $\theta_{JA}$  is 80°C/W. At any given ambient temperature  $T_{JA}$ , use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 and substituting PDMAX for PDMAX' results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4816's maximum junction temperature.

$$T_{A} = T_{JMAX} - 2 \times P_{DMAX} \theta_{JA}$$
 (5)

For a typical application with a 5V power supply and an  $8\Omega$  load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 48°C.

$$T_{\text{JMAX}} = P_{\text{DMAX}} \theta_{\text{JA}} + T_{\text{A}} \tag{6}$$

Equation 6 gives the maximum junction temperature T<sub>JMAX</sub>. If the result violates the LM4816's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If twice the value given by Equation 3 exceeds the value given by Equation 4, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature.



#### **OUTPUT VOLTAGE LIMITER**

The LM4816's adjustable output voltage limiter can be used to set a maximum and minimum output voltage swing magnitude. The voltage applied to the V<sub>LIM</sub> input (pin 20) controls the amount voltage limit magnitude.

Without the limiter's influence (V<sub>LIM</sub> = 0V), the LM4816's maximum BTL output swing is nominally

$$2 \times V_{DD}$$

When the limiter input voltage is greater than 0V, the BTL output voltage swing is

$$V_{OUT-BTL} = (2 \times V_{DD}) - (4 \times V_{LIM})$$

with a tolerance of ±800 mV.

### **POWER SUPPLY BYPASSING**

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a  $10\mu\text{F}$  in parallel with a  $0.1\mu\text{F}$  filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local  $1.0\mu\text{F}$  tantalum bypass capacitance connected between the LM4816's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation in the output signal. Keep the length of leads and traces that connect capacitors between the LM4816's power supply pin and ground as short as possible. Connecting a  $1\mu\text{F}$  capacitor,  $C_B$ , between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turnon time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially  $C_B$ , depends on desired PSRR requirements, click and pop performance (as explained in the section, SELECTING PROPER EXTERNAL COMPONENTS), system cost, and size constraints.

#### **MICRO-POWER SHUTDOWN**

The voltage applied to the SHUTDOWN pin controls the LM4816's shutdown function. Activate micro-power shutdown by applying  $V_{DD}$  to the SHUTDOWN pin. When active, the LM4816's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically  $V_{DD}/2$ . The low 0.6µA typical shutdown current is achieved by applying a voltage that is as near as  $V_{DD}$  as possible to the SHUTDOWN pin. A voltage thrat is less than  $V_{DD}$  may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external  $10k\Omega$  pull-up resistor between the SHUTDOWN pin and  $V_{DD}$ . Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to  $V_{DD}$  through the pull-up resistor, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Table 1. LOGIC LEVEL TRUTH TABLE FOR SHUTDOWN OPERATION

SHUTDOWN	OPERATIONAL MODE			
Low	Full power, stereo BTL amplifiers			
High	Micro-power Shutdown			

#### SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4816's performance requires properly selecting external components. Though the LM4816 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

Product Folder Links: LM4816



The LM4816 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of  $1V_{RMS}$  (2.83 $V_{P-P}$ ). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

#### **Input Capacitor Value Selection**

Amplifying the lowest audio frequencies requires high value input coupling capacitor ( $C_i$  in Figure 23). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size,  $C_i$  has an affect on the LM4816's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually  $V_{DD}/2$ ) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor,  $R_f$ . Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

A shown in Figure 23, the input resistor ( $R_1$ ) and the input capacitor,  $C_1$  produce a -3dB high pass filter cutoff frequency that is found using Equation 7.

$$f_{-3 dB} = \frac{1}{2\pi R_{IN} C_1}$$
 (7)

As an example when using a speaker with a low frequency limit of 150Hz,  $C_1$ , using Equation 4, is 0.063 $\mu$ F. The 1.0 $\mu$ F  $C_1$  shown in Figure 23 allows the LM4816 to drive high efficiency, full range speaker whose response extends below 30Hz.

### **Bypass Capacitor Value Selection**

Besides minimizing the input capacitor size, careful consideration should be paid to value of  $C_B$ , the capacitor connected to the BYPASS pin. Since  $C_B$  determines how fast the LM4816 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4816's outputs ramp to their quiescent DC voltage (nominally  $1/2 \ V_{DD}$ ), the smaller the turn-on pop. Choosing  $C_B$  equal to  $1.0 \mu F$  along with a small value of  $C_i$  (in the range of  $0.1 \mu F$  to  $0.39 \mu F$ ), produces a click-less and pop-less shutdown function. As discussed above, choosing  $C_i$  no larger than necessary for the desired bandwidth helps minimize clicks and pops.

### OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4816 contains circuitry to minimize turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4816's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches  $1/2\ V_{DD}$ . As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the bypass pin current cannot be modified, changing the size of  $C_B$  alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of  $C_B$  reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of  $C_B$  increases, the turn-on time increases. There is a linear relationship between the size of  $C_B$  and the turn-on time. Here are some typical turn-on times for various values of  $C_B$ :

Product Folder Links: LM4816



Св	T <sub>ON</sub>
0.01µF	20 ms
0.1µF	200 ms
0.22µF	440 ms
0.47µF	940 ms
1.0µF	2 Sec

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching  $V_{DD}$  may not allow the capacitors to fully discharge, which may cause "clicks and pops".

#### NO LOAD STABILITY

The LM4816 may exhibit low level oscillation when the load resistance is greater than  $10k\Omega$ . This oscillation only occurs as the output signal swings near the supply voltages. Prevent this oscillation by connecting a  $5k\Omega$  between the output pins and ground.

#### **AUDIO POWER AMPLIFIER DESIGN**

#### Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:  $1W_{RMS}$  Load Impedance:  $8\Omega$  Input Level:  $1V_{RMS}$  Input Impedance:  $20k\Omega$  Bandwidth:  $100Hz-20 \text{ kHz} \pm 0.25 \text{ dB}$ 

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation 4, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation 8. The result in Equation 9.

$$V_{\text{opeak}} = \sqrt{(2R_{\text{L}}P_{\text{O}})}$$
 (8)

$$V_{DD} \ge (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \tag{9}$$

The Output Power vs Supply Voltage graph for an  $8\Omega$  load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4816 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the POWER DISSIPATION section.

After satisfying the LM4816's power dissipation requirements, the minimum differential gain is found using Equation 10.

$$A_{VD} \ge \sqrt{(P_O R_I)} / (V_{IN}) = V_{orms} / V_{inrms}$$
(10)

Thus, a minimum gain of 2.83 allows the LM4816's to reach full output swing and maintain low noise and THD+N performance. For this example, let  $A_{VD} = 3$ .

The amplifier's overall gain is set using the input  $(R_i)$  and feedback  $(R_f)$  resistors. With the desired input impedance set at  $20k\Omega$ , the feedback resistor is found using Equation 11.

$$R_i/R_i = A_{VD}/2 \tag{11}$$

The value of  $R_f$  is  $30k\Omega$ .



The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_1 = 100Hz/5 = 20Hz$$
 (12)

and an

$$F_{H} = 20kHz \times 5 = 100kHz \tag{13}$$

As mentioned in the External Components Description section, R<sub>i</sub> and C<sub>i</sub> create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation 14.

$$C_{i} \ge \frac{1}{2\pi R_{i} f_{C}} \tag{14}$$

the result is

$$1/(2\pi^*20k\Omega^*20Hz) = 0.398\mu F$$
 (15)

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain,  $A_{VD}$ , determines the upper passband response limit. With  $A_{VD}=3$  and  $f_H=100kHz$ , the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4816's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.



# **REVISION HISTORY**

Cł	nanges from Revision A (May 2013) to Revision B	Pa	ıge
•	Changed layout of National Data Sheet to TI format		13



# PACKAGE OPTION ADDENDUM

2-May-2013

#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Diawing		u.,	(2)		(3)		(4)	
LM4816MTX/NOPB	ACTIVE	TSSOP	PW	20	2500	Green (RoHS	CU SN	Level-1-260C-UNLIM		LM4816	Samples
						& no Sb/Br)				MT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





_		
		Dimension designed to accommodate the component width
	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
ı	P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4816MTX/NOPB	TSSOP	PW	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

www.ti.com 8-May-2013



#### \*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4816MTX/NOPB	TSSOP	PW	20	2500	367.0	367.0	35.0

PW (R-PDSO-G20)

# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



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