LM3503 Dual-Display Constant Current LED Driver with Analog Brightness Control

Check for Samples: LM3503

FEATURES

- **Drives up to 4, 6, 8 or 10 White LEDs for Dual Display Backlighting**
- **>80% Peak Efficiency**
- **Output Voltage Protection Options: 16V, 25V, 35V & 44V**
- **Input Under-Voltage Protection**
- **Internal Soft Start Eliminates Inrush Current**
- **1 MHz Constant Switching Frequency**
- **Analog Brightness Control**
- **Wide Input Voltage Range: 2.5V to 5.5V**
- **Low Profile Packages: <1 mm Height**
  - **10 Bump DSBGA**
  - **16 Pin WQFN**

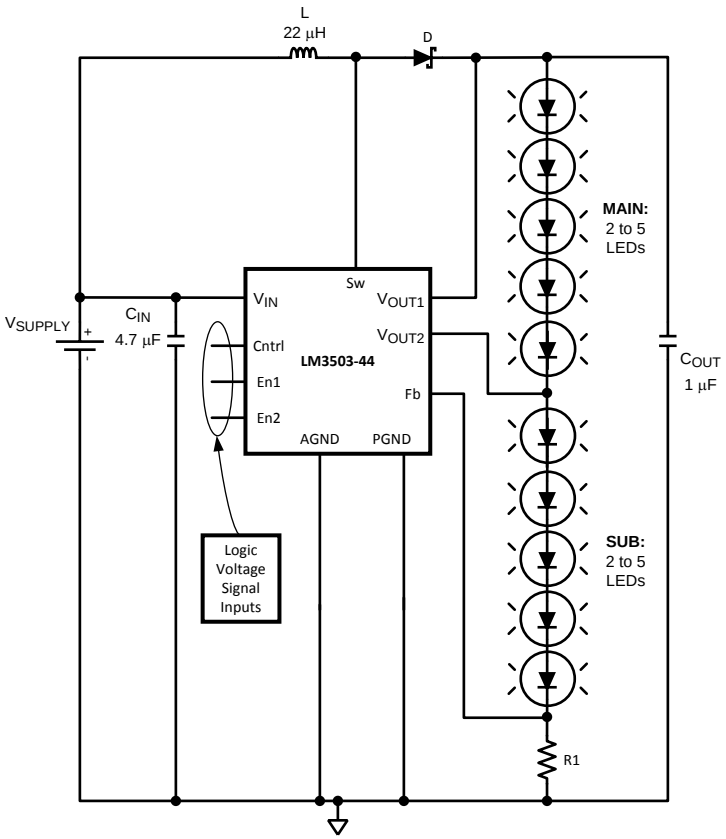
APPLICATIONS

- **Dual Display Backlighting in Portable devices**
- **Cellular Phones and PDAs**

DESCRIPTION

The LM3503 is a white LED driver for lighting applications. For dual display backlighting applications, the LM3503 provides a complete solution. The LM3503 contains two internal white LED current bypass FET (Field Effect Transistor) switches. The white LED current can be adjusted with a DC voltage from a digital to analog converter or RC filtered PWM (pulse-width-modulated) signal at the Cntrl pin.

Typical Application



DESCRIPTION (CONTINUED)

With no external compensation, cycle-by-cycle current limit, output over-voltage protection, input under-voltage protection, and dynamic white LED current control capability, the LM3503 offers superior performance over other step-up white LED drivers.

Connection Diagram

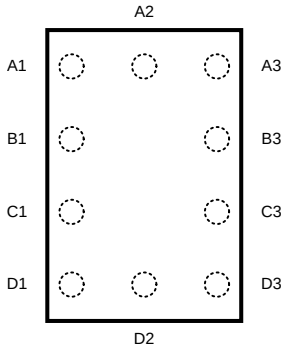


Figure 1. 10-Bump Thin DSBGA Package (YPA0010) (Top View)

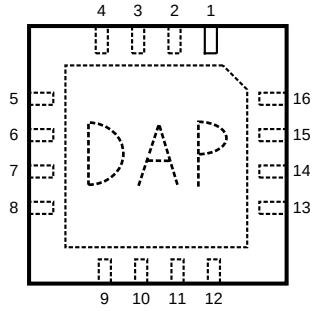


Figure 2. 16-Lead Thin WQFN Package (RGH0016A) (Top View)

PIN DESCRIPTIONS

Bump #	Pin #	Name	Description
A1	9	Cntrl	White LED Current Control Connection
B1	7	Fb	Feedback Voltage Connection
C1	6	V_{OUT2}	Drain Connections of the NMOS and PMOS Field Effect Transistor (FET) Switches (Figure 3: N2 and P1). Connect 100nF at V_{OUT2} node if V_{OUT2} is not used
D1	4	V_{OUT1}	Over-Voltage Protection (OVP) and Source Connection of the PMOS FET Switch (Figure 3: P1)
D2	2 and 3	Sw	Drain Connection of the Power NMOS Switch (Figure 3: N1)
D3	15 and 16	Pgnd	Power Ground Connection
C3	14	Agnd	Analog Ground Connection
B3	13	V_{IN}	Input Voltage Connection
A3	12	En2	NMOS FET Switch Control Connection
A2	10	En1	PMOS FET Switch Control Connection
	1	NC	No Connection
	5	NC	No Connection
	8	NC	No Connection
	11	NC	No Connection
	DAP	DAP	Die Attach Pad (DAP), to be soldered to the printed circuit board's ground plane for enhanced thermal dissipation.

Cntrl (Bump A1): White LED current control pin. Use this pin to control the feedback voltage with an external DC voltage.

Fb (Bump B1): Output voltage feedback connection.

V_{OUT2} (Bump C1): Drain connections of the internal PMOS and NMOS FET switches (Figure 3: P1 and N2). It is recommended to connect 100nF at V_{OUT2} if V_{OUT2} is not used for LM3503-35V & LM3503-44V versions.

V_{OUT1}(Bump D1):

Source connection of the internal PMOS FET switch (Figure 3: P1) and OVP sensing node. The output capacitor must be connected as close to the device as possible, between the V_{OUT1} pin and ground plane. Also connect the Schottky diode as close as possible to the V_{OUT1} pin to minimize trace resistance and EMI radiation.

Sw (Bump D2):

Drain connection of the internal power NMOS FET switch (Figure 3: N1). Minimize the metal trace length and maximize the metal trace width connected to this pin to reduce EMI radiation and trace resistance.

Pgnd (Bump D3): Power ground pin. Connect directly to the ground plane.

Agnd (Bump C3): Analog ground pin. Connect the analog ground pin directly to the Pgnd pin.

V_{IN} (Bump B3): Input voltage connection pin. The C_{IN} capacitor should be as close to the device as possible, between the V_{IN} pin and ground plane.

En2 (Bump A3): Enable pin for the internal NMOS FET switch (Figure 3: N2) during device operation. When V_{En2} is ≥ 1.4V, the internal NMOS FET switch turns off and the SUB display is turned on. The En2 pin has an internal pull down circuit, thus the internal NMOS FET switch is normally in the on state of operation with the SUB display turned off. When V_{En2} is ≤ 0.3V, the internal NMOS FET switch turns on and the SUB display is turned off. If both V_{En1} and V_{En2} are ≤ 0.3V the LM3503 will shutdown. If V_{OUT2} is not used, En2 must be floating or grounded and En1 used to enable the device.

En1 (Bump A2): Enable pin for the internal PMOS FET switch (Figure 3: P1) during device operation. When V_{En1} is ≤ 0.3V, the internal PMOS FET switch turns on and the MAIN display is turned off. When V_{En1} is ≥ 1.4V, the internal PMOS FET switch turns off and the MAIN display is turned on. If both V_{En1} and V_{En2} are ≤ 0.3V the LM3503 will shutdown. The En1 pin has an internal pull down circuit, thus the internal PMOS FET switch is normally in the on state of operation with the MAIN display turned off. If V_{OUT2} is not used, En2 must be grounded and En1 use to enable the device.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{IN} Pin		−0.3V to +5.5V
Sw Pin		−0.3V to +48V
Fb Pin		−0.3V to +5.5V
Cntrl Pin		−0.3V to +5.5V
V_{OUT1}Pin		−0.3V to +48V
V_{OUT2} Pin		−0.3V to V_{OUT1}
En1		−0.3V to +5.5V
En2		−0.3V to +5.5V
Continuous Power Dissipation		Internally Limited
Maximum Junction Temperature (T_{J-MAX})		+150°C
Storage Temperature Range		−65°C to +150°C
ESD Rating(3)	Human Body Model	2 kV
	Machine Model	200V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical characteristic specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Conditions(1)(2)

Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range	−40°C to +85°C
Supply Voltage, V_{IN} Pin	2.5V to 5.5V
En1 and En2 Pins	0V to 5.5V
Cntrl Pin	0V to 3.5V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical characteristic specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the GND pin.

Thermal Properties(3)

Junction-to-Ambient Thermal Resistance (θ_{JA})	
DSBGA Package	65°C/W
WQFN Package	49°C/W

(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See Thermal Properties for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{J(MAX)}–T_A)/ \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature. For more information on this topic, please refer to Application Note 1187(An1187): Leadless Leadframe Package (LLP) and Application Note 1112(AN1112) for DSBGA chip scale package.

Electrical Characteristics(1)(2)

Limits in standard typeface are for T_J = +25°C. Limits in **bold typeface** apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise specified, V_{IN} = 2.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.5		5.5	V
I_Q	Non-Switching Switching Shutdown	Cntrl = 1.6V Fb = 0V, Sw Is Floating En1 = En2 = 0V		0.5 1.9 0.1	**1** **3** **3**	mA mA µA
V_{Fb}	Feedback Voltage	Cntrl = 3.5V	**0.5**	0.55	**0.6**	V
I_{CL}	NMOS Power Switch Current Limit	16, Fb = 0V 25, Fb = 0V 35, Fb = 0V 44,FB = 0V	**250** **400** **450** **450**	400 600 750 750	**650** **800** **1050** **1050**	mA
I_{Fb}	Feedback Pin Output Bias Current	Fb = 0.25V, Cntrl = 1.6V		64	**500**	nA
F_S	Switching Frequency		**0.8**	1	**1.2**	MHz
$R_{DS(ON)}$	NMOS Power Switch ON Resistance (Figure 3: N1)	I_{Sw} = 500 mA(3)		0.55	**1.1**	Ω
$R_{PDS(ON)}$	PMOS ON Resistance Of V_{OUT1}/V_{OUT2} Switch (Figure 3: P1)	I_{PMOS} = 20 mA, En1 = 0V, En2 = 1.5V		5	**10**	Ω
$R_{NDS(ON)}$	NMOS ON Resistance Of V_{OUT2}/Fb Switch (Figure 3: N2)	I_{NMOS} = 20 mA, En1 = 1.5V, En2 = 0V		2.5	**5**	Ω
D_{MAX}	Maximum Duty Cycle	Fb = 0V	**90**	95		%
I_{Sw}	Sw Pin Leakage Current(4)	Sw = 42V, En1 = En2 =0V		0.01	**5**	µA
$I_{VOUT1(OFF)}$	V_{OUT1} Pin Leakage Current(4)	V_{OUT1} = 14V, En1 = En2 = 0V (16) V_{OUT1} = 23V, En1 = En2 = 0V (25) V_{OUT1} = 32V, En1 = En2 = 0V (35) V_{OUT1} = 42V, En1 = En2 = 0V (44)		0.1 0.1 0.1 0.1	**3** **3** **3** **3**	µA
$I_{VOUT1(ON)}$	V_{OUT1} Pin Bias Current(4)	V_{OUT1} = 14V, En1 = En1 = 1.5V (16) V_{OUT1} = 23V, En1 = En2 = 1.5V (25) V_{OUT1} = 32V, En1 = En2 = 1.5V (35) V_{OUT1} = 42V, En1 = En2 = 1.5V (44)		40 50 50 85	**80** **100** **100** **140**	µA
I_{VOUT2}	V_{OUT2}Pin Leakage Current(4)	Fb = En1 = En2 = 0V, V_{OUT2} = V_{OUT1} = 42V		0.1	**3**	µA
UVP	Under-Voltage Protection	On Threshold Off Threshold	 **2.2**	2.4 2.3	**2.5**	V

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not specified, but do represent the most likely norm.
(3) NMOS Power On Resistance measured at I_{SW}= 250mA for sixteen voltage version.
(4) Current flows into the pin.

Electrical Characteristics[1][2] (continued)

Limits in standard typeface are for T_J = +25°C. Limits in **bold typeface** apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise specified, V_{IN} = 2.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OVP	Over-Voltage Protection[5]	On Threshold (16) Off Threshold (16) On Threshold (25) F Off Threshold (25) On Threshold (35) Off Threshold (35) On Threshold (44) Off Threshold (44)	**14.5** **14.0** **22.5** **21.5** **32.0** **31.0** **40.5** **39.0**	15.5 15 24 23 34 33 42 41	**16.5** **16.0** **25.5** **24.5** **35.0** **34.0** **43.5** **42.0**	V
V_{En1}	PMOS FET Switch and Device Enabling Threshold (Figure 3: P1)	Off Threshold		0.8	**0.3**	V
		On Threshold	**1.4**	0.8		
V_{En2}	NMOS FET Switch and Device Enabling Threshold (Figure 3: N2)	Off Threshold		0.8	**0.3**	V
		On Threshold	**1.4**	0.8		
V_{Cntrl}	V_{Cntrl} Range	V_{IN} = 3.6V	0.2		3.5	V
I_{En1}	En1 Pin Bias Current[6]	En1 = 2.5V En1 = 0V		7 0.1	**14**	µA
I_{En2}	En2 Pin Bias Current[6]	En2 = 2.5V En2 = 0V		7 0.1	**14**	µA
I_{CNTRL}	Cntrl Pin Bias Current[6]	Cntrl = 2.5V		8	**14**	µA

(5) The on threshold indicates that the LM3503 is no longer switching or regulating LED current, while the off threshold indicates normal operation.
(6) Current flows into the pin.

Block Diagram

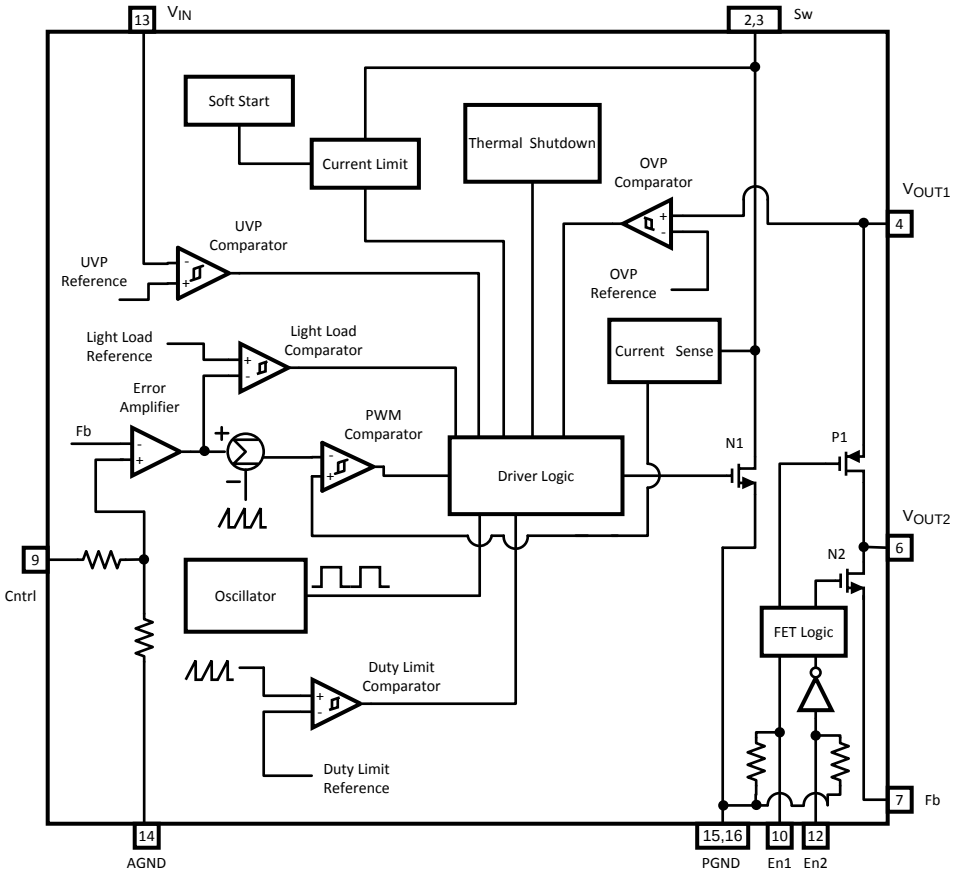


Figure 3. Block Diagram

Detailed Description of Operation

The LM3503 utilizes an asynchronous current mode pulse-width-modulation (PWM) control scheme to regulate the feedback voltage over specified load conditions. The DC/DC converter behaves as a controlled current source for white LED applications. The operation can best be understood by referring to the block diagram in Figure 3 for the following operational explanation. At the start of each cycle, the oscillator sets the driver logic and turns on the internal NMOS power device, N1, conducting current through the inductor and reverse biasing the external diode. The white LED current is supplied by the output capacitor when the internal NMOS power device, N1, is turned on. The sum of the error amplifier's output voltage and an internal voltage ramp are compared with the sensed power NMOS, N1, switch voltage. Once these voltages are equal, the PWM comparator will then reset the driver logic, thus turning off the internal NMOS power device, N1, and forward biasing the external diode. The inductor current then flows through the diode to the white LED load and output capacitor. The inductor current recharges the output capacitor and supplies the current for the white LED load. The oscillator then sets the driver logic again repeating the process. The output voltage of the error amplifier controls the current through the inductor. This voltage will increase for larger loads and decrease for smaller loads limiting the peak current in the inductor and minimizing EMI radiation. The duty limit comparator is always operational, it prevents the internal NMOS power switch, N1, from being on for more than one oscillator cycle and conducting large amounts of current. The light load comparator allows the LM3503 to properly regulate light/small white LED load currents, where regulation becomes difficult for the LM3503's primary control loop. Under light load conditions, the LM3503 will enter into a pulse skipping pulse-frequency-mode (PFM) of operation where the operational frequency will vary with the load. As a result of PFM mode operation, the output voltage ripple magnitude will significantly increase.

The LM3503 has two control pins, En1 and En2, used for selecting which segment of a single white LED string network is active for dual display applications. En1 controls the main display (MAIN) segment of the single string white LED network between pins V_{OUT1} and V_{OUT2}. En2 controls the sub display (SUB) segment of the single string white LED network between the V_{OUT2} and Fb. If both V_{En1} and V_{En2} are ≤ 0.3V, the LM3503 will shutdown, for further description of the En1 and En2 operation, see Figure 33. During shutdown the output capacitor discharges through the string of white LEDs and feedback resistor to ground. The LED current can be dynamically controlled by a DC voltage on the Cntrl pin. When V_{Cntrl} = 0V the white LED current may not be equal to zero because of offsets within the LM3503 internal circuitry. To ensure zero white LED current the LM3503 must be in shutdown mode operation.

The LM3503 has dedicated protection circuitry active during normal operation to protect the integrated circuit (IC) and external components. Soft start circuitry is present in the LM3503 to allow for slowly increasing the current limit to its steady-state value to prevent undesired high inrush current during start up. Thermal shutdown circuitry turns off the internal NMOS power device, N1, when the internal semiconductor junction temperature reaches excessive levels. The LM3503 has a under-voltage protection (UVP) comparator that disables the internal NMOS power device when battery voltages are too low, thus preventing an on state where the internal NMOS power device conducts large amounts of current. The over-voltage protection (OVP) comparator prevents the output voltage from increasing beyond the protection limit when the white LED string network is removed or if there is a white LED failure. OVP allows for the use of low profile ceramic capacitors at the output. The current through the internal NMOS power device, N1, is monitored to prevent peak inductor currents from damaging the IC. If during a cycle (cycle=1/switching frequency) the peak inductor current exceeds the current limit for the LM3503, the internal NMOS power device will be turned off for the remaining duration of that cycle.

En1	En2	**Result** (See **Figure 1** and **Figure 2**)	Shutdown
0.3V	0.3V	**[**P1→OFF N2→OFF N1→OFF**] or [**MAIN→OFF SUB→OFF N1→OFF**]**	X
1.4V	0.3V	**[**P1→OFF N2→ON N1→Switching**] or [**MAIN→ON SUB→OFF N1→Switching**]**	
0.3V	1.4V	**[**P1→ON N2→OFF N1→Switching**] or [**MAIN→OFF SUB→ON N1→Switching**]**	
1.4V	1.4V	**[**P1→OFF N2→OFF N1→Switching**] or [**MAIN→ON SUB→ON N1→Switching**]**	

Figure 4. Operational Characteristics Table

Typical Performance Characteristics

(See Typical Application Circuit : L=DO1608C-223 and D=B150-13. Efficiency: $\eta = P_{OUT}/ P_{IN} = [(V_{OUT} – V_{Fb}) * I_{OUT}] / [V_{IN} * I_{IN}]$. T_A = +25°C, unless otherwise stated.)

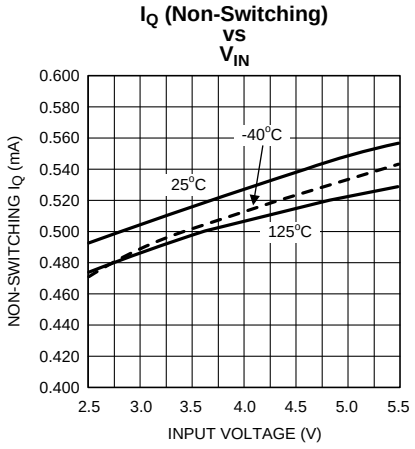


Figure 5.

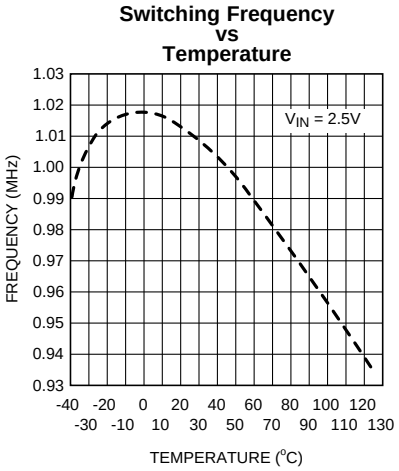


Figure 6.

Typical Performance Characteristics (continued)

(See Typical Application Circuit : L=DO1608C-223 and D=B150-13. Efficiency: $\eta = P_{OUT} / P_{IN} = [(V_{OUT} - V_{Fb}) * I_{OUT}] / [V_{IN} * I_{IN}]$. T_A = +25°C, unless otherwise stated.)

I_Q (Switching) vs V_{IN}

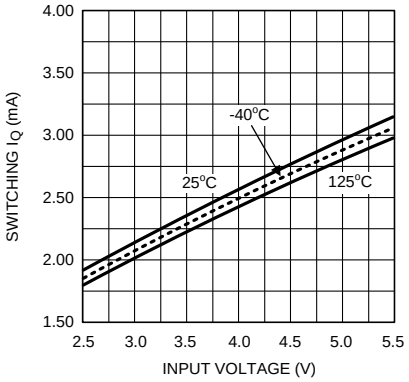


Figure 7.

I_Q (Switching) vs Temperature

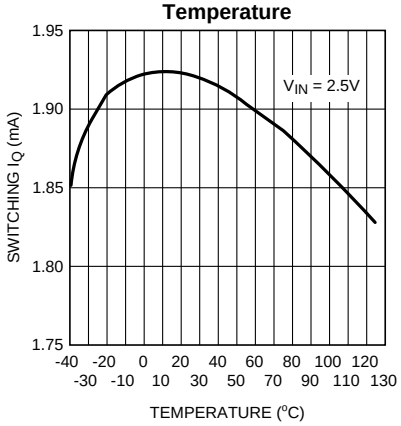


Figure 8.

10 LED Efficiency vs LED Current

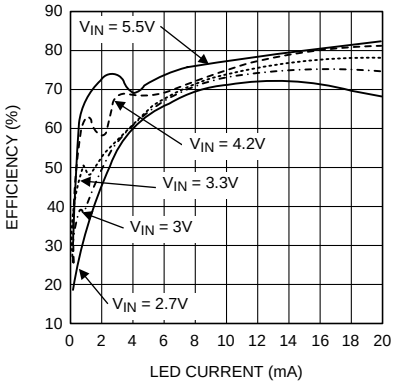


Figure 9.

8 LED Efficiency vs LED Current

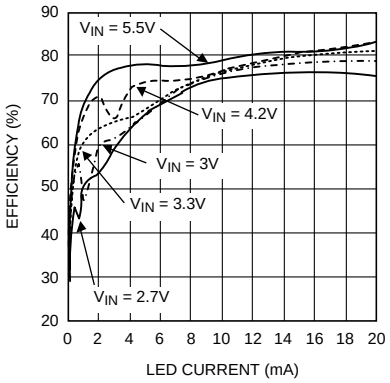


Figure 10.

6 LED Efficiency vs LED Current

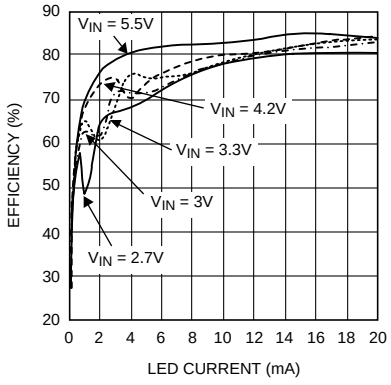


Figure 11.

4 LED Efficiency vs LED Current

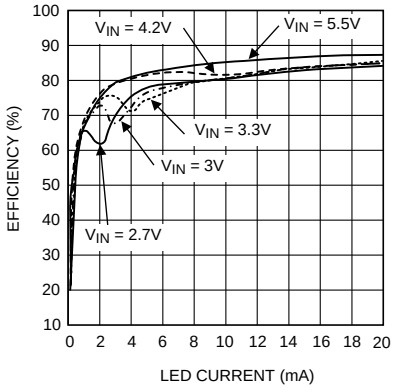


Figure 12.

Typical Performance Characteristics (continued)

(See Typical Application Circuit : L=DO1608C-223 and D=B150-13. Efficiency: η = P_{OUT}/ P_{IN} = [(V_{OUT} – V_{Fb}) * I_{OUT}] / [V_{IN} * I_{IN}]. T_A = +25°C, unless otherwise stated.)

Cntrl Pin Current vs Cntrl Pin Voltage

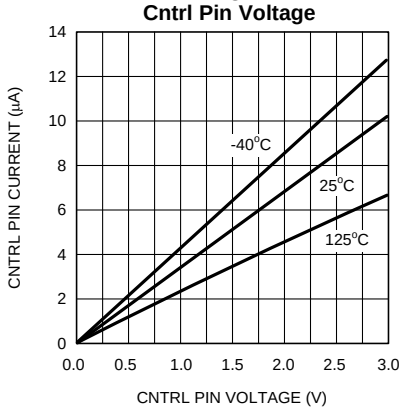


Figure 13.

Maximum Duty Cycle vs Temperature

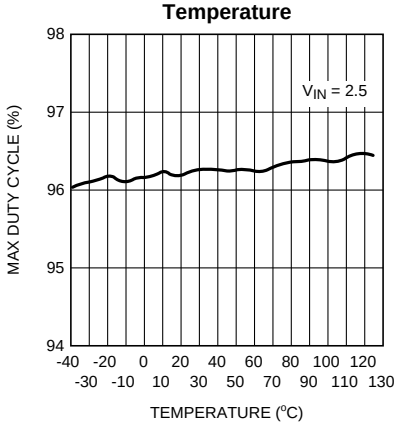


Figure 14.

En1 Pin Current vs En1 Pin Voltage

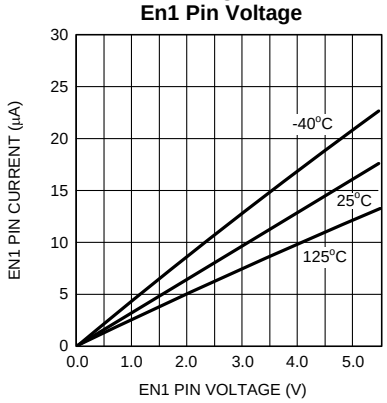


Figure 15.

En2 Pin Current vs En2 Pin Voltage

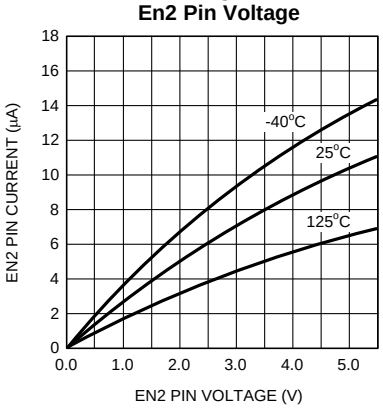


Figure 16.

V_{OUT1} Pin Current vs V_{OUT1}Pin Voltage

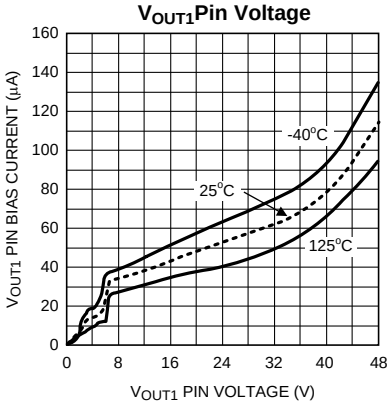


Figure 17.

Power NMOS $R_{DS(ON)}$ (Figure 3: N1) vs V_{IN}

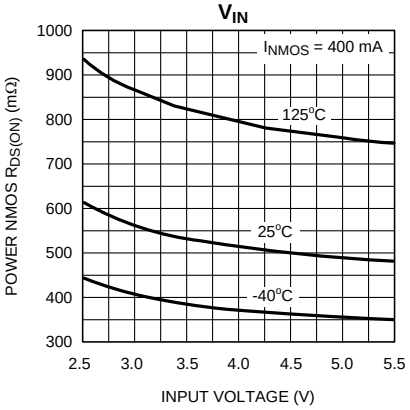


Figure 18.

Typical Performance Characteristics (continued)

(See Typical Application Circuit : L=DO1608C-223 and D=B150-13. Efficiency: η = P_{OUT}/ P_{IN} = [(V_{OUT} – V_{Fb}) * I_{OUT}] / [V_{IN} * I_{IN}]. T_A = +25°C, unless otherwise stated.)

NMOS $R_{DS(ON)}$ (Figure 3: N2) vs V_{IN}

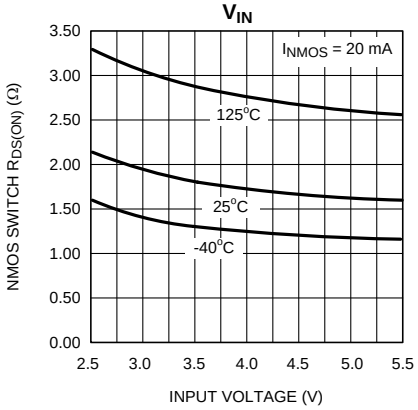


Figure 19.

PMOS $R_{DS(ON)}$ (Figure 3: P1) vs V_{IN}

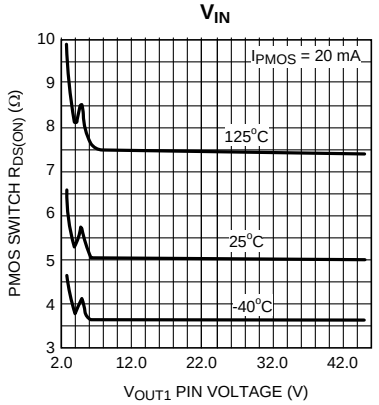


Figure 20.

Feedback Voltage vs Cntrl Pin Voltage

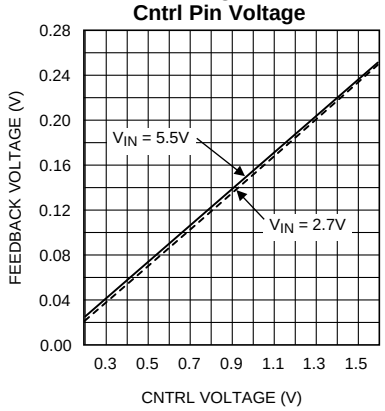


Figure 21.

Current Limit (LM3503-16) vs Temperature

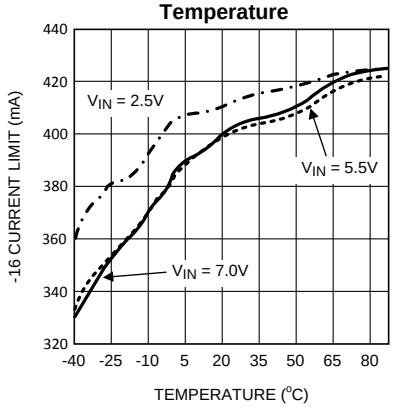


Figure 22.

Current Limit (LM3503-16) vs V_{IN}

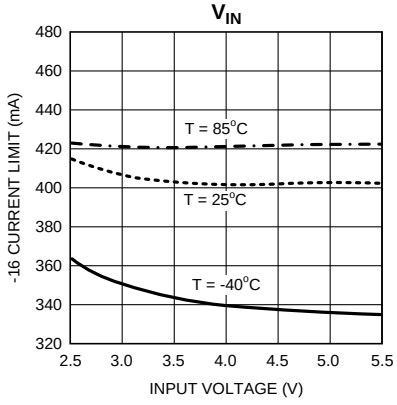


Figure 23.

Current Limit (LM3503-25) vs Temperature

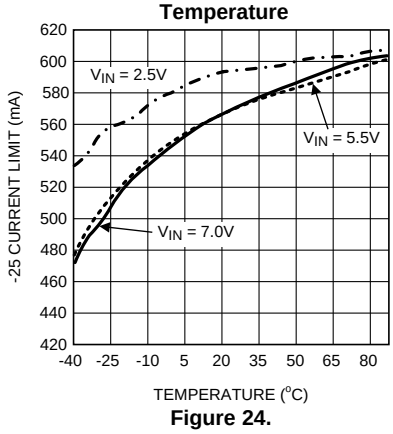


Figure 24.

Typical Performance Characteristics (continued)

(See Typical Application Circuit : L=DO1608C-223 and D=B150-13. Efficiency: η = P_{OUT}/ P_{IN} = [(V_{OUT} – V_{Fb}) * I_{OUT}] / [V_{IN} * I_{IN}]. T_A = +25°C, unless otherwise stated.)

Current Limit (LM3503-25) vs V_{IN}

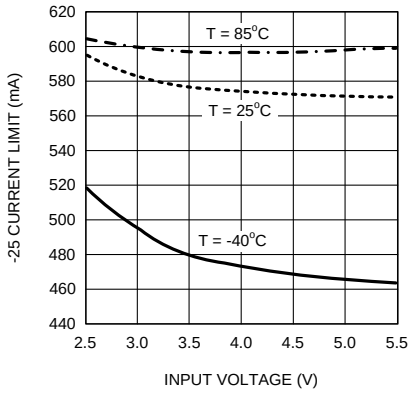


Figure 25.

Current Limit (LM3503-35/44) vs Temperature

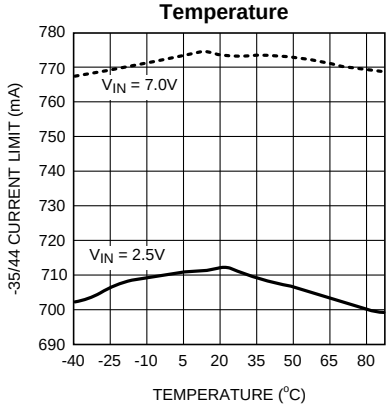


Figure 26.

Current Limit (LM3503-35/44) vs V_{IN}

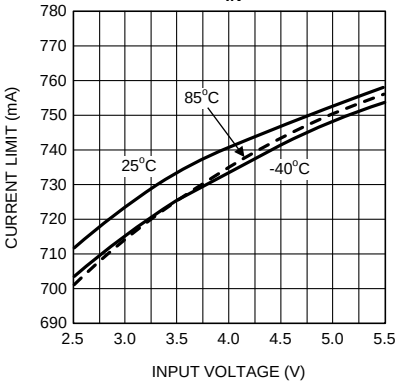


Figure 27.

Feedback Voltage (V_{Cntrl} = 0.8V) vs Temp

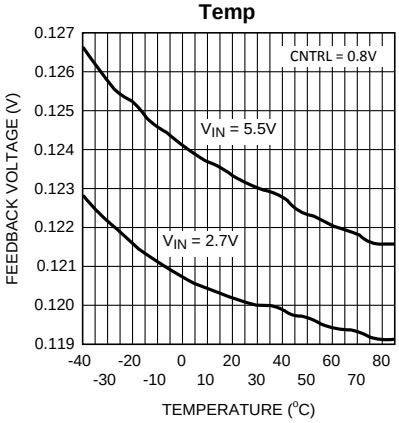


Figure 28.

Feedback Voltage (V_{Cntrl} = 1.6V) vs Temp

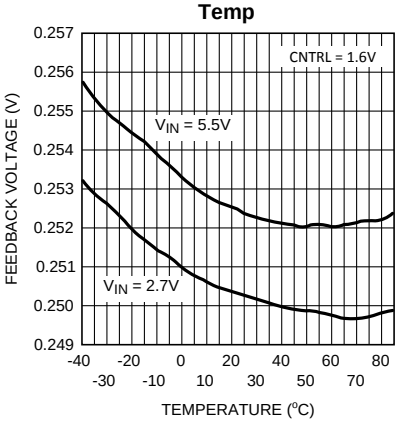


Figure 29.

V_{IN} = 3.6V at 15mA & 4 Leds

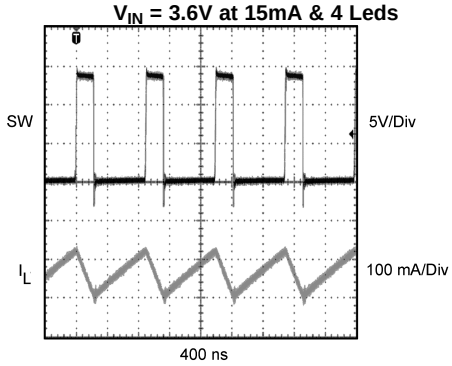


Figure 30.

Typical Performance Characteristics (continued)

(See Typical Application Circuit : L=DO1608C-223 and D=B150-13. Efficiency: $\eta = P_{OUT} / P_{IN} = [(V_{OUT} - V_{Fb}) * I_{OUT}] / [V_{IN} * I_{IN}]$. T_A = +25°C, unless otherwise stated.)

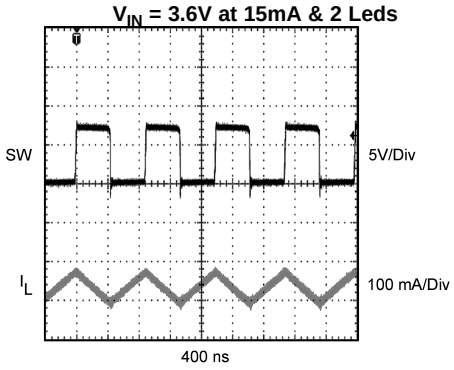


Figure 31.

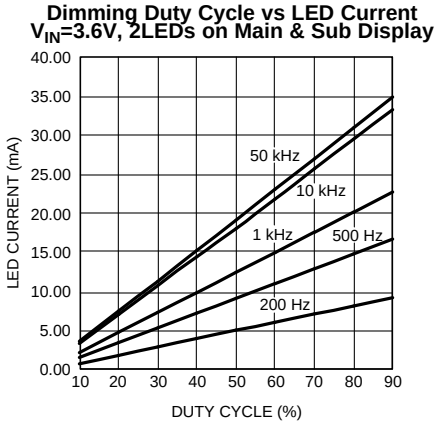


Figure 32.

APPLICATION INFORMATION

WHITE LED CURRENT SETTING

The white LED current is controlled by a DC voltage at the Cntrl pin.

The relationship between the Cntrl pin voltage and Fb pin voltage can be computed with the following:

$V_{FB} = (0.156) \times (V_{Cntrl})$

- V_{Cntrl}: Cntrl Pin Voltage. Voltage Range: $0.2V \le V_{Cntrl} \le 3.5V$.
- V_{Fb}: Feedback Pin Voltage. (1)

LED CURRENT

The LED current is set using the following equation:

$$I_{LED} = \frac{V_{Fb}}{R1} \quad (2)$$

To determine the maximum output current capability of the device, it is best to estimate using equations on page 16 and the minimum peak current limit of the device (see electrical table). Note the current capability will be higher with less LEDs in the application.

WHITE LED DIMMING

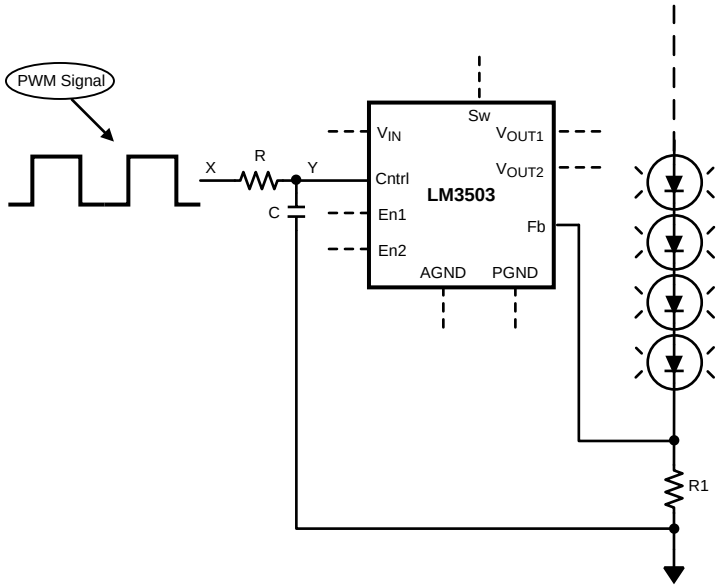


Figure 33. If V_{OUT2} is not used, En2 must be grounded

Aside from varying the DC voltage at the Cntrl pin, white LED dimming can be accomplished through the RC filtering of a PWM signal. The PWM signal frequency should be at least a decade greater than the RC filter bandwidth. WHITE LED DIMMING is how the LM3503 should be wired for PWM filtered white LED dimming functionality. When using PWM dimming, it is recommended to add 1-2ms delay between the Cntrl signal and the main Enable sginal (En1) to allow time for the output to discharge. This will prevent potential flickering especially if the Sub display is compose of 2 LEDs or less.

The equations below are guidelines for choosing the correct RC filter values in relation to the PWM signal frequency.

Equation:

$$F_{RC} = \frac{1}{2 \times \pi \times R \times C} \quad (3)$$

Equation:

$$F_{PWM} > 10 \times F_{RC} \quad (4)$$

F_{RC}: RC Filter Bandwidth Cutoff Frequency.

F_{PWM}: PWM Signal Frequency.

R: Chosen Filter Resistor.

C: Chosen Filter Capacitor.

For example, using the above equations to determine the proper RC values. Assume the following condition:V_{IN}= 3.6V, C=0.01µF and F_{PWM} = 500Hz, then F_{RC}= 50Hz by relation to equation 2. By rearranging equation 1 to solve for R; R = 318.5K ohms (standard value, R = 316K).

PWM Dimming Duty Cycle vs. LED Current

The results are based on the 2LEDs on Main display and 2LEDs on Sub display

Duty	200Hz	500Hz	1KHz	10KHz	50KHz	100kHz
(%)	R = 787k ohms	R =316k ohms	R = 158kohms	R=16.2k ohms	R=3.16k ohms	R=1.62k ohms
10	0.78mA	1.59mA	2.23mA	3.42mA	3.58mA	3.61mA
20	1.85mA	3.46mA	4.78mA	7.09mA	7.41mA	7.48mA
30	2.88mA	5.35mA	7.33mA	10.77mA	11.25mA	11.34mA
40	3.96mA	7.24mA	9.88mA	14.48mA	15.12mA	15.24mA
50	5.05mA	9.12mA	12.45mA	19.1mA	19.06mA	19.16mA
60	6.08mA	11.03mA	15.03mA	21.86mA	22.98mA	23.10mA
70	7.13mA	12.94mA	17.61mA	25.71mA	26.9mA	27.05mA
80	8.17mA	14.83mA	20.20mA	29.53mA	30.83mA	31.00mA
90	9.24mA	16.73mA	22.79mA	33.32mA	34.78mA	35.00mA

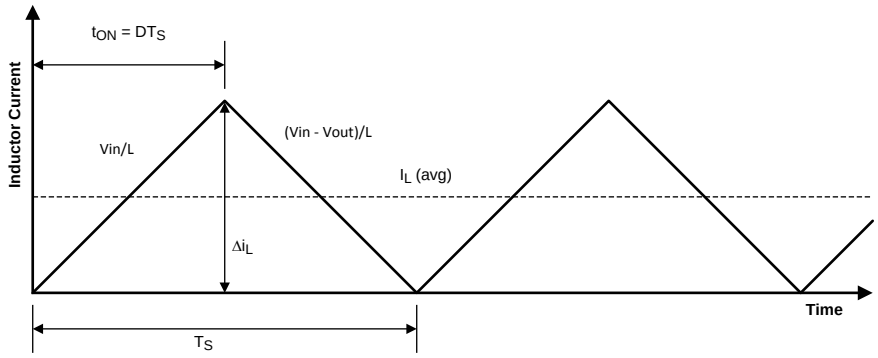


Figure 34. Inductor Current Waveform

CONTINUOUS AND DISCONTINUOUS MODES OF OPERATION

Since the LM3503 is a constant frequency pulse-width-modulated step-up regulator, care must be taken to make sure the maximum duty cycle specification is not violated. The duty cycle equation depends on which mode of operation the LM3503 is in. The two operational modes of the LM3503 are continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Continuous conduction mode refers to the mode of operation where during the switching cycle, the inductor current never goes to and stays at zero for any significant amount of time during the switching cycle. Discontinuous conduction mode refers to the mode of operation where during the switching cycle, the inductor current goes to and stays at zero for a significant amount of time during the switching cycle. Figure 34 illustrates the threshold between CCM and DCM operation. In Figure 34 the inductor current is right on the CCM/DCM operational threshold. Using this as a reference, a factor can be introduced to calculate when a particular application is in CCM or DCM operation. R is a CCM/DCM factor we can use to compute which mode of operation a particular application is in. If R is ≥ 1, then the application is operating in CCM. Conversely, if R is < 1, the application is operating in DCM. The R factor inequalities are a result of the components that make up the R factor. From Figure 34, the R factor is equal to the average inductor current, I_L(avg), divided by half the inductor ripple current, Δi_L. Using Figure 34, the following equation can be used to compute R factor:

$$R = \frac{2 * I_L (avg)}{\Delta i_L} \quad (5)$$

$$I_L (avg) = \frac{[I_{OUT}]}{[(1-D) * Eff]} \quad (6)$$

$$\Delta i_L = \frac{[V_{IN} * D]}{[L * Fs]} \quad (7)$$

$$R = \frac{[2 * I_{OUT} * L * Fs * (V_{OUT})^2]}{[(V_{IN})^2 * Eff * (V_{OUT} - V_{IN})]} \quad (8)$$

V_{IN}: Input Voltage.

V_{OUT}: Output Voltage.

Eff: Efficiency of the LM3503.

Fs: Switching Frequency.

I_{OUT}: White LED Current/Load Current.

L: Inductance Magnitude/Inductor Value.

D: Duty Cycle for CCM operation.

Δi_L: Inductor Ripple Current.

I_L(avg): Average Inductor Current.

For CCM operation, the duty cycle can be computed with:

$$D = \frac{t_{ON}}{T_S} \quad (9)$$

$$D = \frac{[V_{OUT} - V_{IN}]}{[V_{OUT}]} \quad (10)$$

D: Duty Cycle for CCM Operation.

V_{OUT}: Output Voltage.

V_{IN} : Input Voltage.

For DCM operation, the duty cycle can be computed with:

$$D = \frac{t_{ON}}{T_S} \quad (11)$$

$$D = \sqrt{\frac{[2 * I_{OUT} * L * (V_{OUT} - V_{IN}) * Fs]}{[(V_{IN})^2 * Eff]}} \quad (12)$$

D: Duty Cycle for DCM Operation.

V_{OUT}: Output Voltage.

V_{IN} : Input Voltage.

I_{OUT}: White LED Current/Load Current.

Fs: Switching Frequency.

L: Inductor Value/Inductance Magnitude.

INDUCTOR SELECTION

In order to maintain inductance, an inductor used with the LM3503 should have a saturation current rating larger than the peak inductor current of the particular application. Inductors with low DCR values contribute decreased power losses and increased efficiency. The peak inductor current can be computed for both modes of operation: CCM and DCM.

The cycle-by-cycle peak inductor current for CCM operation can be computed with:

$$I_{Peak} \approx I_L\,(avg) + \frac{\Delta i_L}{2} \quad (13)$$

$$I_{Peak} \approx \frac{[I_{OUT}]}{[(1 - D) * Eff]} + \frac{[V_{IN} * D]}{[2 * L * Fs]} \quad (14)$$

V_{IN}: Input Voltage.

Eff: Efficiency of the LM3503.

Fs: Switching Frequency.

I_{OUT}: White LED Current/Load Current.

L: Inductance Magnitude/Inductor Value.

D: Duty Cycle for CCM Operation.

I_{PEAK}: Peak Inductor Current.

Δi_L: Inductor Ripple Current.

I_L(avg): Average Inductor Current.

The cycle-by-cycle peak inductor current for DCM operation can be computed with:

$$I_{Peak} \approx \frac{[V_{IN} * D]}{[L * Fs]} \quad (15)$$

V_{IN}: Input Voltage.

Fs: Switching Frequency.

L: Inductance Magnitude/Inductor Value.

D: Duty Cycle for DCM Operation.

I_{PEAK}: Peak Inductor Current.

The minimum inductance magnitude/inductor value for the LM3503 can be calculated using the following, which is only valid when the duty cycle is > 0.5:

$$L > \frac{[V_{IN} * R_{DS(ON)} * ((D/D') - 1)]}{[1.562 * Fs]} \quad (16)$$

D: Duty Cycle.

D': 1-D.

$R_{DS(ON)}$: NMOS Power Switch ON Resistance.

Fs: Switching Frequency.

V_{IN}: Input Voltage.

L: Inductance Magnitude/Inductor Value.

This equation gives the value required to prevent subharmonic oscillations. The result of this equation and the inductor ripple currents should be accounted for when choosing an inductor value.

Some recommended Inductor manufactures included but are not limited to:

Coilcraft	DO1608C-223	www.coilcraft.com
	DT1608C-223	

CAPACITOR SELECTION

Multilayer ceramic capacitors are the best choice for use with the LM3503. Multilayer ceramic capacitors have the lowest equivalent series resistance (ESR). Applied voltage or DC bias, temperature, dielectric material type (X7R, X5R, Y5V, etc), and manufacturer component tolerance have an affect on the true or effective capacitance of a ceramic capacitor. Be aware of how your application will affect a particular ceramic capacitor by analyzing the aforementioned factors of your application. Before selecting a capacitor always consult the capacitor manufacturer's data curves to verify the effective or true capacitance of the capacitor in your application.

INPUT CAPACITOR SELECTION

The input capacitor serves as an energy reservoir for the inductor. In addition to acting as an energy reservoir for the inductor the input capacitor is necessary for the reduction in input voltage ripple and noise experienced by the LM3503. The reduction in input voltage ripple and noise helps ensure the LM3503's proper operation, and reduces the effect of the LM3503 on other devices sharing the same supply voltage. To ensure low input voltage ripple, the input capacitor must have an extremely low ESR. As a result of the low input voltage ripple requirement multilayer ceramic capacitors are the best choice. A minimum capacitance of 2.0 µF is required for normal operation, so consult the capacitor manufacturer's data curves to verify whether the minimum capacitance requirement is going to be achieved for a particular application.

OUTPUT CAPACITOR SELECTION

The output capacitor serves as an energy reservoir for the white LED load when the internal power FET switch (Figure 3: N1) is on or conducting current. The requirements for the output capacitor must include worst case operation such as when the load opens up and the LM3503 operates in over-voltage protection (OVP) mode operation. A minimum capacitance of 0.5 µF is required to ensure normal operation. Consult the capacitor manufacturer's data curves to verify whether the minimum capacitance requirement is going to be achieved for a particular application.

Some recommended capacitor manufacturers included but are not limited to:

Taiyo-Yuden	GMK212BJ105MD (0805/35V)	www.t-yuden.com
muRata	GRM40-035X7R105K (0805/50V)	www.murata.com
TDK	C3216X7R1H105KT (1206/50V)	www.tdktca.com
	C3216X7R1C475K (1206/16V)	
AVX	08053D105MAT (0805/25V)	www.avxcorp.com
	08056D475KAT (0805/6.3V)	
	1206ZD475MAT (1206/10V)	

DIODE SELECTION

To maintain high efficiency it is recommended that the average current rating (I_F or I_O) of the selected diode should be larger than the peak inductor current (I_{Lpeak}). At the minimum the average current rating of the diode should be larger than the maximum LED current. To maintain diode integrity the peak repetitive forward current (I_{FRM}) must be greater than or equal to the peak inductor current (I_{Lpeak}). Diodes with low forward voltage ratings (V_F) and low junction capacitance magnitudes (C_J or C_T or C_D) are conducive to high efficiency. The chosen diode must have a reverse breakdown voltage rating (V_R and/or V_{RRM}) that is larger than the output voltage (V_{OUT}). No matter what type of diode is chosen, Schottky or not, certain selection criteria must be followed:

1. V_R and $V_{RRM} > V_{OUT}$
2. I_F or $I_O \geq I_{LOAD}$ or I_{OUT}
3. $I_{FRM} \geq I_{Lpeak}$

Some recommended diode manufacturers included but are not limited to:

Vishay	SS12(1A/20V)	www.vishay.com
	SS14(1A/40V)	
	SS16(1A/60V)	

On Semiconductor	MBRM120E (1A/20V)	www.onsemi.com
	MBRS1540T3 (1.5A/40V)	
	MBR240LT (2A/40V)	
Central Semiconductor	CMSH1-40M (1A/40V)	www.centralsemi.com

SHUTDOWN AND START-UP

On startup, the LM3503 contains special circuitry that limits the peak inductor current which prevents large current spikes from loading the battery or power supply. The LM3503 is shutdown when both En1 and En2 signals are less than 0.3V. During shutdown the output voltage is a diode drop below the supply voltage. When shutdown, the softstart is reset to prevent inrush current at the next startup.

THERMAL SHUTDOWN

The LM3503 stops regulating when the internal semiconductor junction temperature reaches approximately 140°C. The internal thermal shutdown has approximately 20°C of hysteresis which results in the LM3503 turning back on when the internal semiconductor junction temperature reaches 120°C. When the thermal shutdown temperature is reached, the softstart is reset to prevent inrush current when the die temperature cools.

UNDER VOLTAGE PROTECTION

The LM3503 contains protection circuitry to prevent operation for low input supply voltages. When Vin drops below 2.3V, typically, the LM3503 will no longer regulate. In this mode, the output voltage will be one diode drop below Vin and the softstart will be reset. When Vin increases above 2.4V, typically, the device will begin regulating again.

OVER VOLTAGE PROTECTION

The LM3503 contains dedicated ciruitry for monitoring the output voltage. In the event that the LED network is disconnected from the LM3503, the output voltage will increase and be limited to 15.5V(typ.) for the 16V version, 24V(typ.) for the 25V version, 34V(typ.) for 35V version and 42V(typ.) for the 44V version. (see electrical table for more details). In the event that the network is reconnected regulation will resume at the appropriate output voltage.

LAYOUT CONSIDERATIONS

All components, except for the white LEDs, must be placed as close as possible to the LM3503. The die attach pad (DAP) must be soldered to the ground plane.

The input bypass capacitor C_{IN}, as shown in the Typical Application Circuit, must be placed close to the IC and connect between the V_{IN} and Pgnd pins. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100 nF bypass capacitor can be placed in parallel with C_{IN} to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, must be placed close to the IC and be connected between the V_{OUT1} and Pgnd pins. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple and efficiency. The current setting resistor, R1, should be kept close to the Fb pin to minimize copper trace connections that can inject noise into the system. The ground connection for the current setting resistor network should connect directly to the Pgnd pin. The Agnd pin should be tied directly to the Pgnd pin. Trace connections made to the inductor should be minimized to reduce power dissipation and increase overall efficiency while reducing EMI radiation. For more details regarding layout guidelines for switching regulators, refer to Applications Note AN-1149.

REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3503ITL-25/NOPB	OBSOLETE	DSBGA	YPA	10		TBD	Call TI	Call TI	-40 to 85	SBJB	
LM3503ITL-35/NOPB	OBSOLETE	DSBGA	YPA	10		TBD	Call TI	Call TI	-40 to 85	SBKB	
LM3503ITL-44/NOPB	OBSOLETE	DSBGA	YPA	10		TBD	Call TI	Call TI	-40 to 85	SDNB	
LM3503SQ-16/NOPB	OBSOLETE	WQFN	RGH	16		TBD	Call TI	Call TI	-40 to 85	L00045B	
LM3503SQ-25/NOPB	OBSOLETE	WQFN	RGH	16		TBD	Call TI	Call TI	-40 to 85	L00046B	
LM3503SQ-35	OBSOLETE	WQFN	RGH	16		TBD	Call TI	Call TI	-40 to 85	L00047B	
LM3503SQ-35/NOPB	OBSOLETE	WQFN	RGH	16		TBD	Call TI	Call TI	-40 to 85	L00047B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

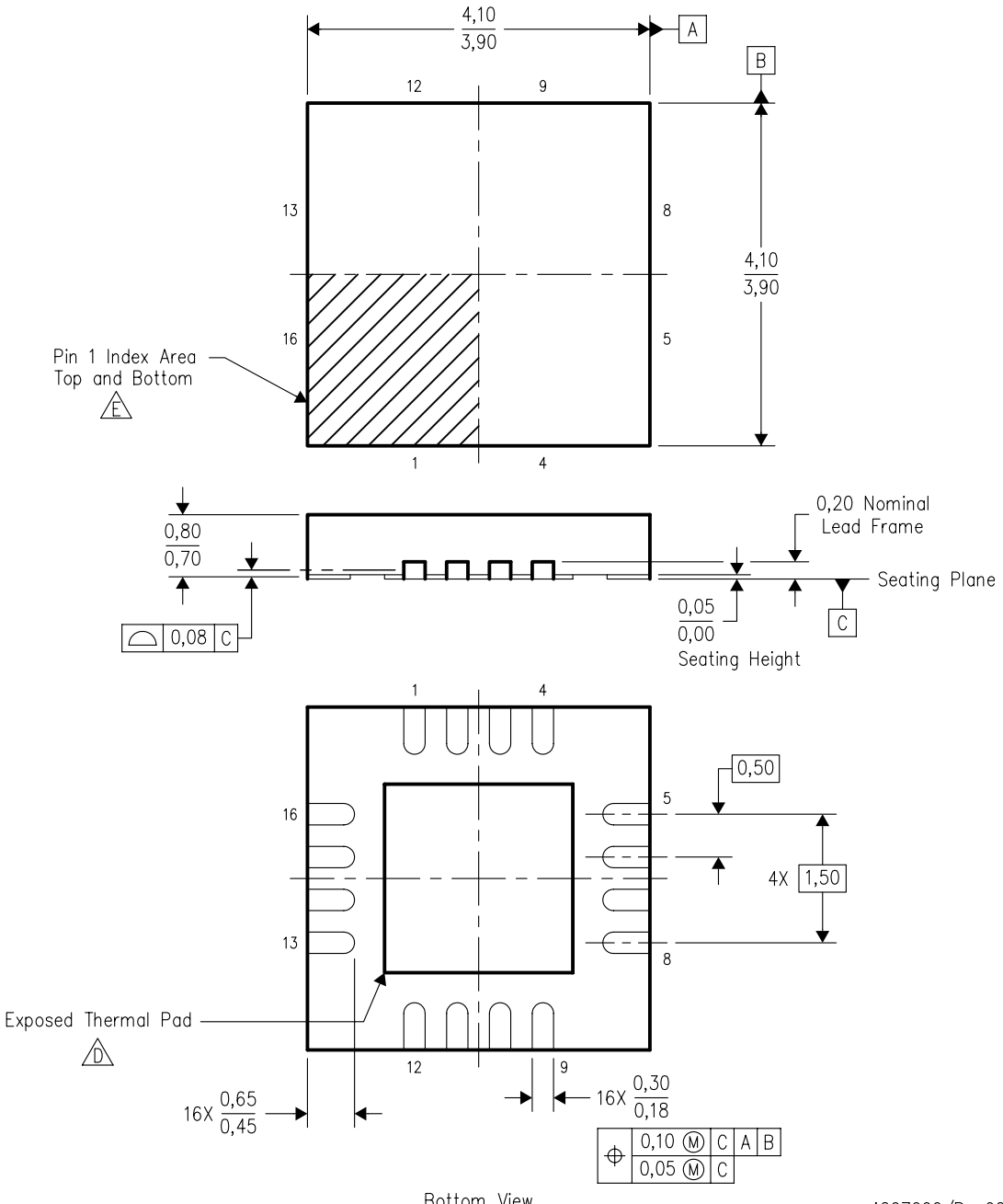
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

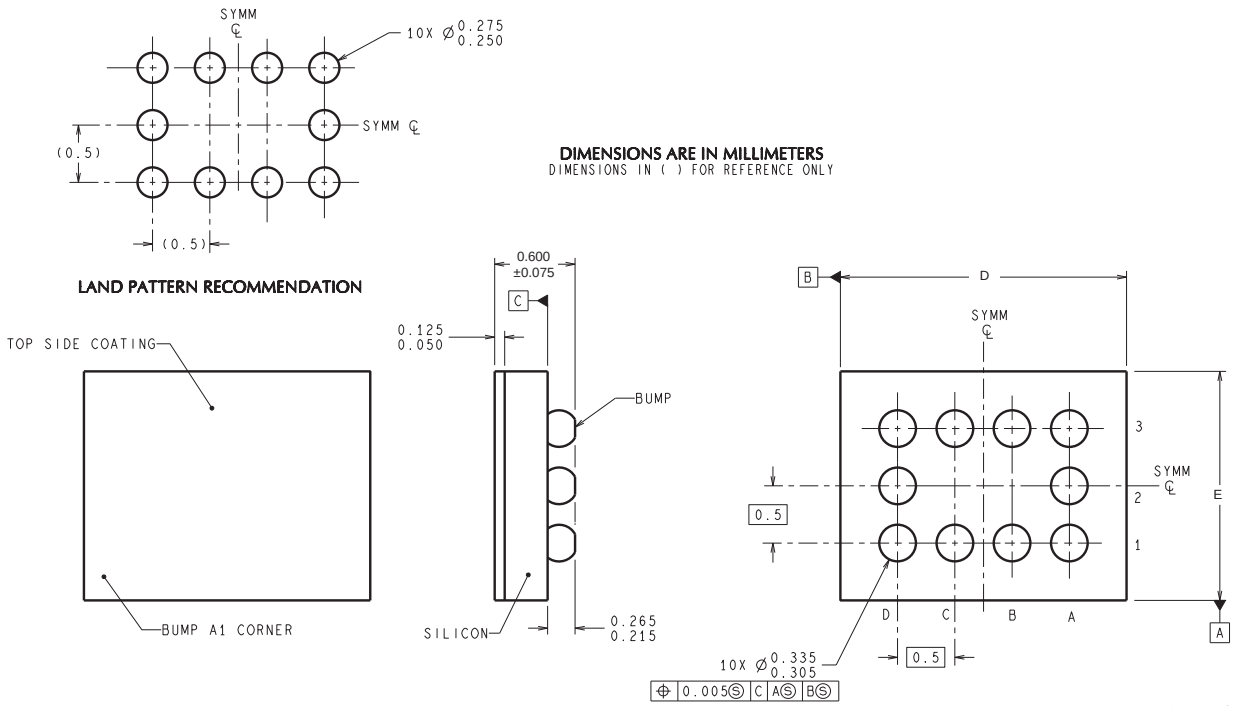
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RGH (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Complies to JEDEC MO–220 variation WGGD–4.

YPA0010



TLP10XXX (Rev D)

4215069/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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