International
IOR Rectifier

PD-95727A

IRF8915PbF

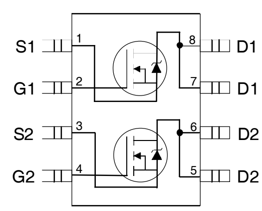
HEXFET® Power MOSFET

Applications

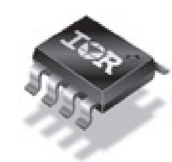
Dual SO-8 MOSFET for POL converters in desktop, servers, graphics cards, game consoles and set-top box

- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	I_D
20V	18.3mΩ@V_{GS} = 10V	8.9A



Top View



SO-8

Benefits

- Ultra-Low Gate Impedance
- Very Low $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	8.9	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	7.1	
I_{DM}	Pulsed Drain Current ①	71	
P_D @T_A = 25°C	Power Dissipation	2.0	W
P_D @T_A = 70°C	Power Dissipation	1.3	
	Linear Derating Factor	0.016	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	——	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④	——	62.5	

Notes ① through ⑤ are on page 10

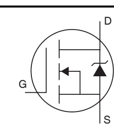
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.015	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	14.6	18.3	mΩ	V_{GS} = 10V, I_D = 8.9A ③
		—	21.6	27		V_{GS} = 4.5V, I_D = 7.1A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.7	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.8	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V_{DS} = 16V, V_{GS} = 0V
		—	—	150		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	12	—	—	S	V_{DS} = 10V, I_D = 7.1A
Q_g	Total Gate Charge	—	4.9	7.4		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	1.8	—		V_{DS} = 10V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	0.61	—	nC	V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	1.7	—		I_D = 7.1A
Q_{godr}	Gate Charge Overdrive	—	0.79	—		See Fig. 6
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	2.3	—		
Q_{oss}	Output Charge	—	2.7	—	nC	V_{DS} = 10V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	—	6.0	—		V_{DD} = 4.5V, V_{GS} = 4.5V
t_r	Rise Time	—	12	—	ns	I_D = 7.1A
$t_{d(off)}$	Turn-Off Delay Time	—	7.1	—		Clamped Inductive Load
t_f	Fall Time	—	3.6	—		
C_{iss}	Input Capacitance	—	540	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	180	—	pF	V_{DS} = 10V
C_{rss}	Reverse Transfer Capacitance	—	91	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	15	mJ
I_{AR}	Avalanche Current ①	—	7.1	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	71		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 7.1A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	13	19	ns	T_J = 25°C, I_F = 7.1A, V_{DD} = 10V
Q_{rr}	Reverse Recovery Charge	—	3.5	5.2	nC	di/dt = 100A/μs ③

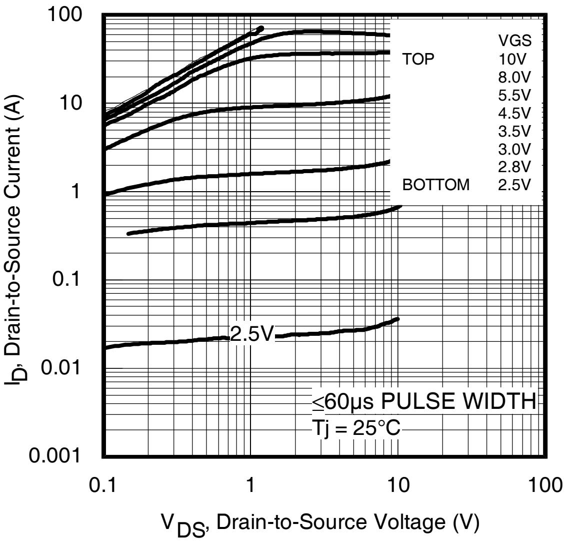


Fig 1. Typical Output Characteristics

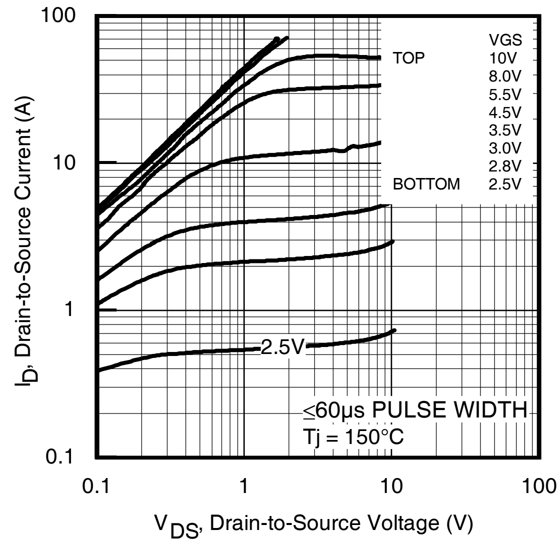


Fig 2. Typical Output Characteristics

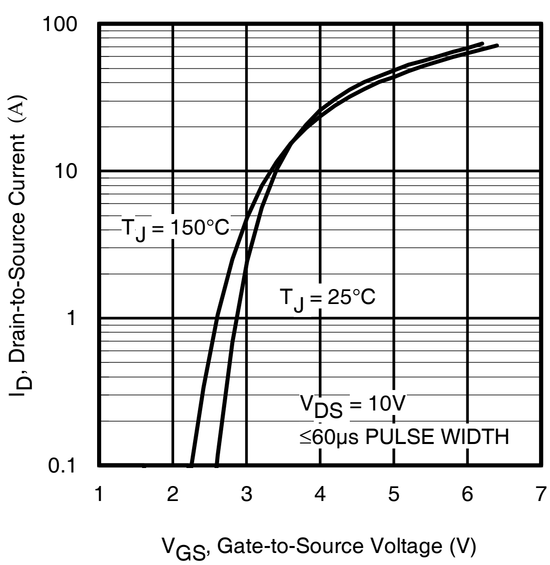


Fig 3. Typical Transfer Characteristics

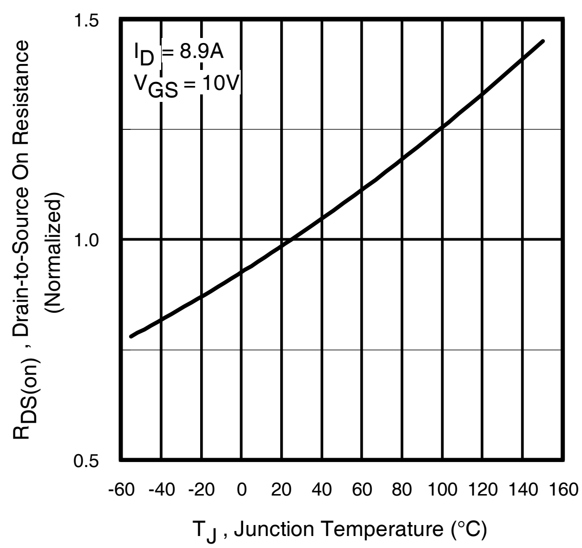


Fig 4. Normalized On-Resistance vs. Temperature

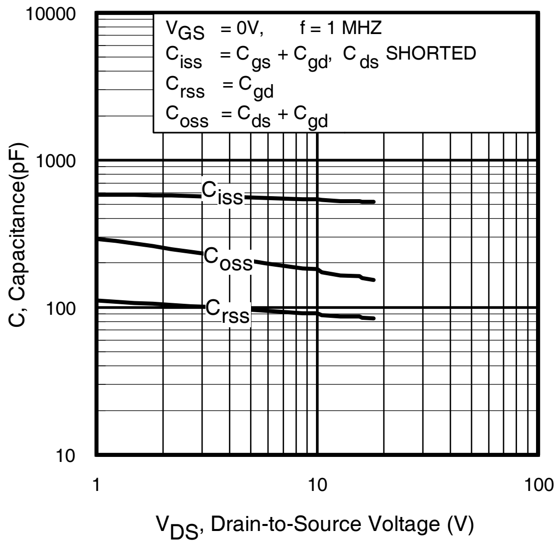


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

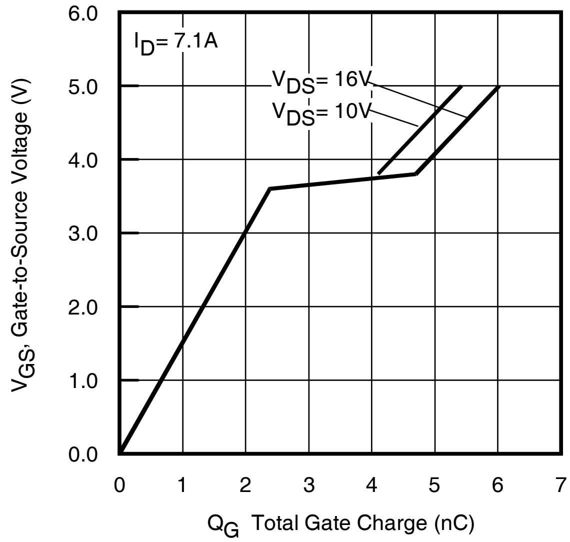


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

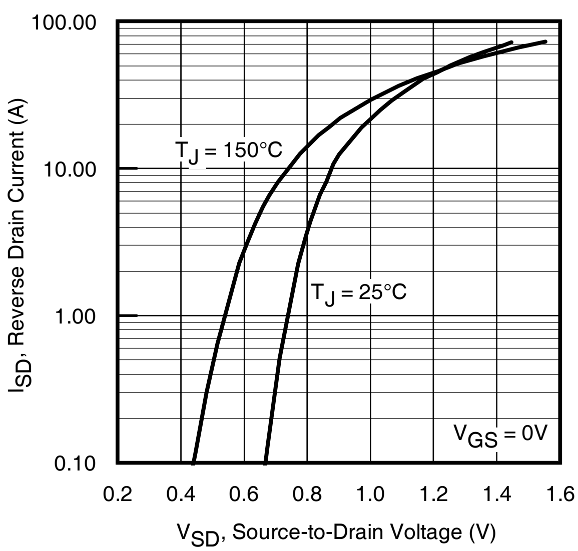


Fig 7. Typical Source-Drain Diode Forward Voltage

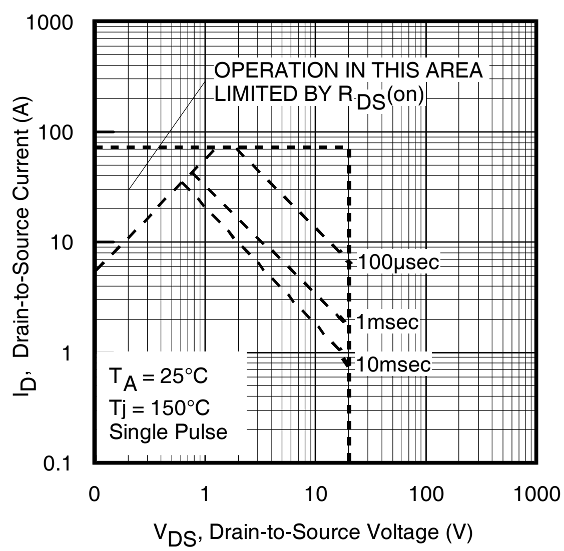
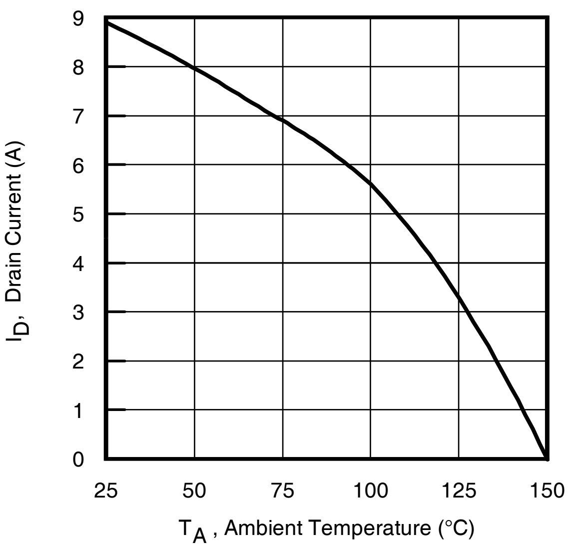


Fig 8. Maximum Safe Operating Area



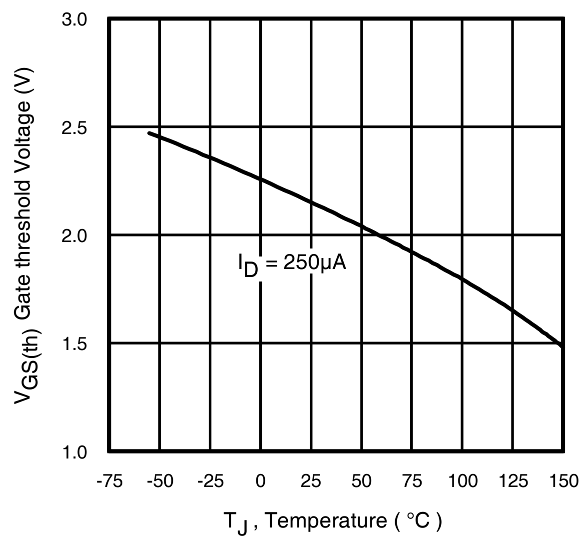
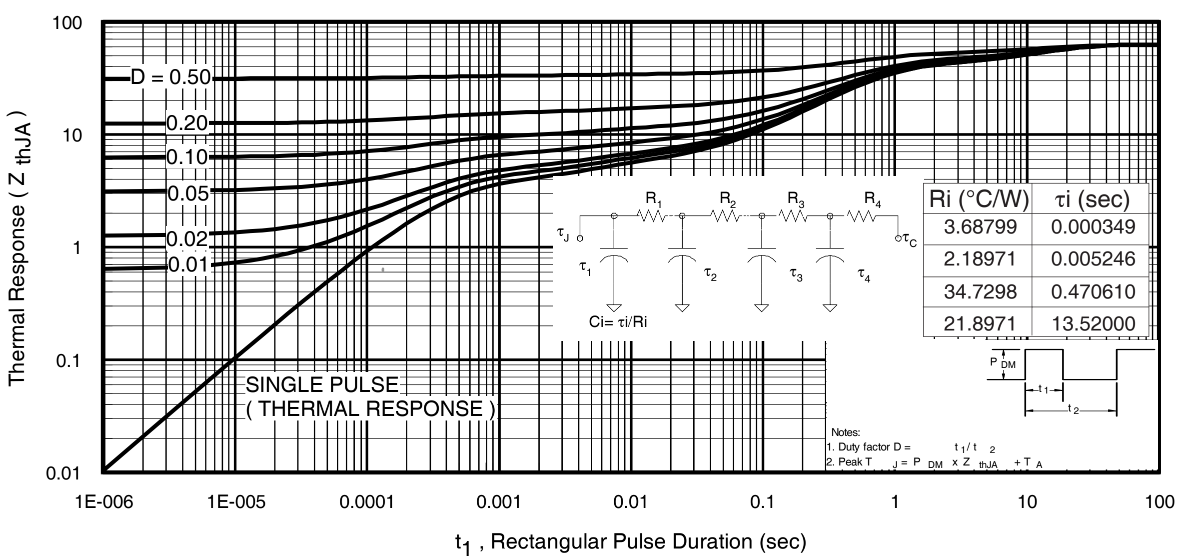


Fig 9. Maximum Drain Current vs. Ambient Temperature

Fig 10. Threshold Voltage vs. Temperature



Ri (°C/W)	τi (sec)
3.68799	0.000349
2.18971	0.005246
34.7298	0.470610
21.8971	13.52000

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

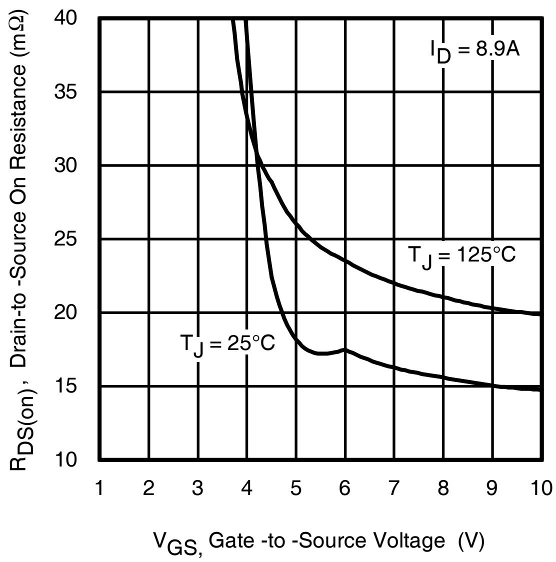


Fig 12. On-Resistance vs. Gate Voltage

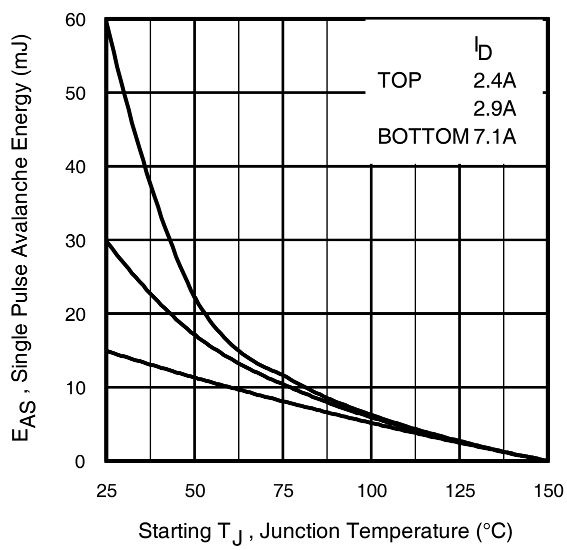


Fig 13. Maximum Avalanche Energy vs. Drain Current

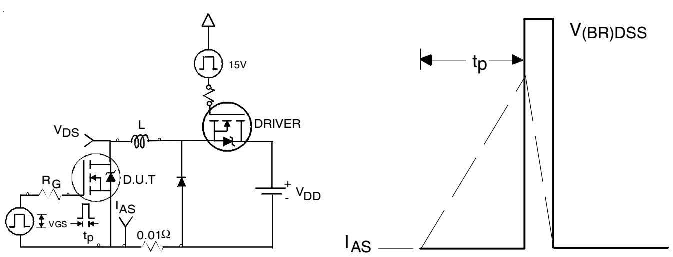


Fig 14. Unclamped Inductive Test Circuit and Waveform

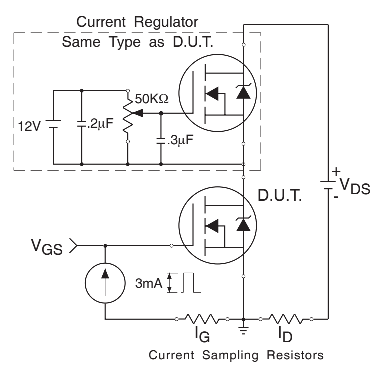


Fig 15. Gate Charge Test Circuit

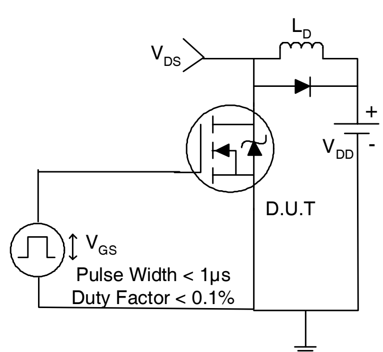


Fig 16. Switching Time Test Circuit

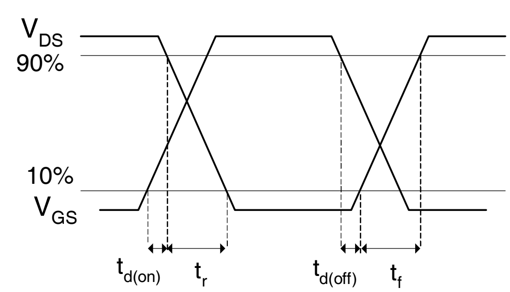


Fig 17. Switching Time Waveforms

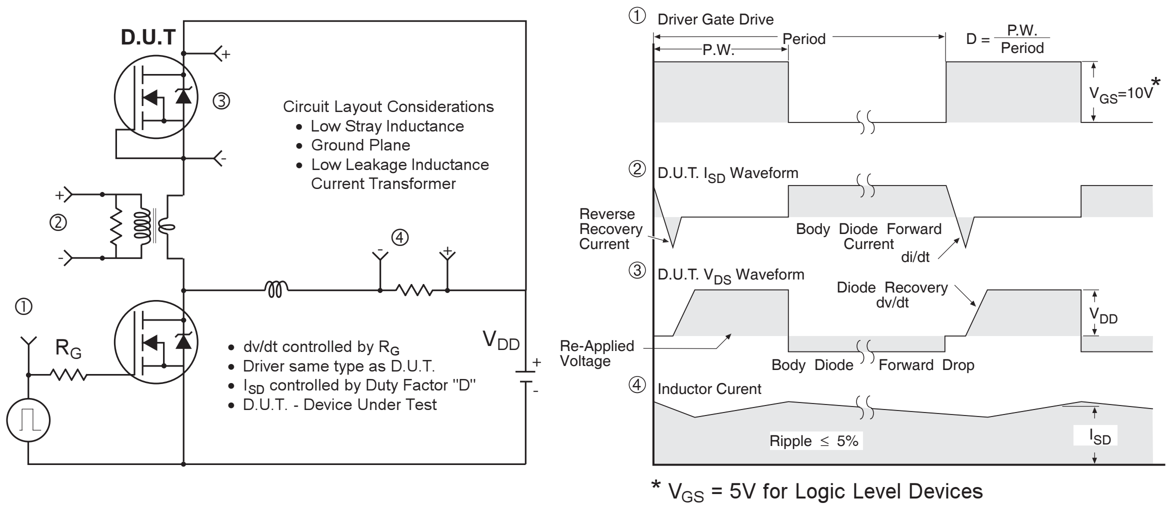


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

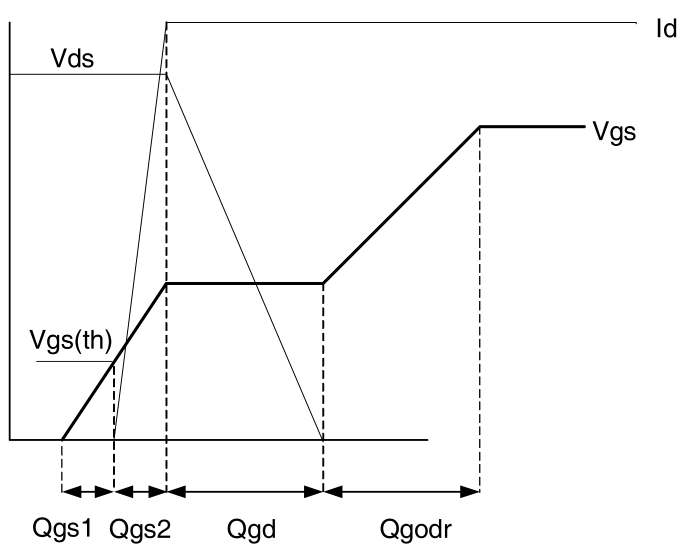


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

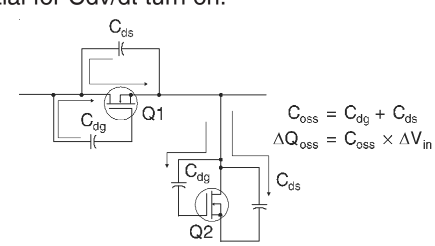
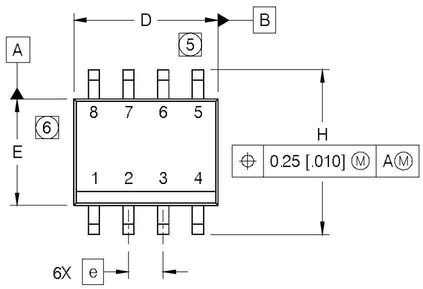


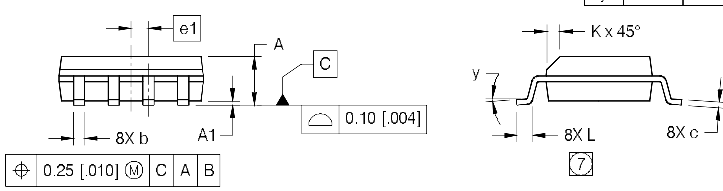
Figure A: Q_{oss} Characteristic

SO-8 Package Outline(Mosfet & Fetky)

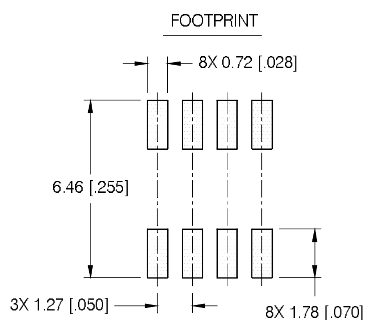
Dimensions are shown in milimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

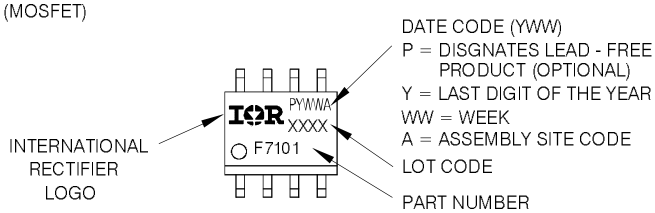


NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



SO-8 Part Marking Information

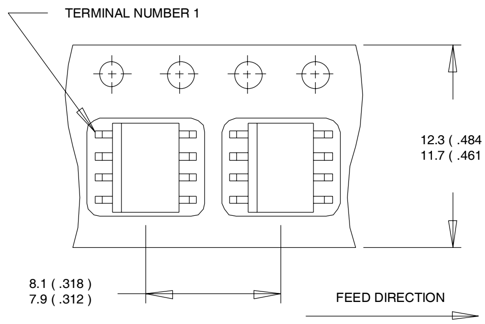
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



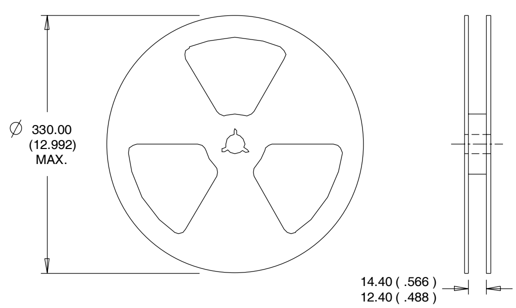
Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.59mH, R_G = 25Ω, I_{AS} = 7.1A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ R_θ is measured at T_J of approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

International
IOR Rectifier

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