IRF520

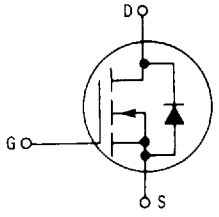
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

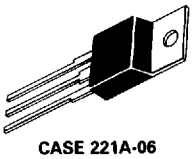
TMOS POWER FET
8 AMPERES
$R_{DS(on)}$ = 0.27 OHM
100 VOLTS

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS®





CASE 221A-06
(TO-220AB)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 8 5 32	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	°C

See the MTP10N10E Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$R_{DS(on)}$	—	0.27	Ohm
On-State Drain Current (V_{GS} = 10 V) ($V_{DS} \geq$ 2.4 Vdc)		$I_{D(on)}$	8	—	Adc
Forward Transconductance ($V_{DS} \geq$ 2.4 V, I_D = 4 A)		g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	($V_{DD} \approx$ 0.5 V_{DSS}, I_D = 4 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	70	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	70	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	13 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.4 (Typ)	2.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	280 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)		L_s	7.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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