TEXAS INSTRUMENTS

SCCS054C - August 1994 - Revised October 2003

CY74FCT16373T
CY74FCT162373T

16-Bit Latches

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **$V_{CC} = 5V \pm 10\%$**

CY74FCT16373T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at $V_{CC} = 5V$, $T_A = 25˚C$**

CY74FCT162373T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at $V_{CC} = 5V$, $T_A = 25˚C$**

Functional Description

CY74FCT16373T and CY74FCT162373T are 16-bit D-type latches designed for use in bus applications requiring high speed and low power. These devices can be used as two independent 8-bit latches or as a single 16-bit latch by connecting the Output Enable ($\overline{OE}$) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16373T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162373T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162373T is ideal for driving transmission lines.

Logic Block Diagrams

TO 7 OTHER CHANNELS

FCT162373-1

TO 7 OTHER CHANNELS

FCT162373-2
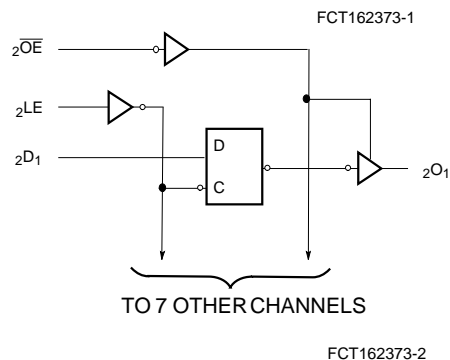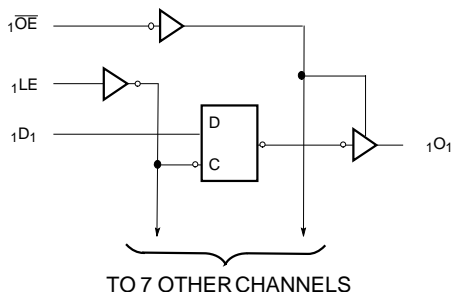
Pin Configuration

SSOP/TSSOP/TVSOP
Top View

Pin		Pin
$_1\overline{OE}$	1	48	$_1$LE
$_1O_1$	2	47	$_1D_1$
$_1O_2$	3	46	$_1D_2$
GND	4	45	GND
$_1O_3$	5	44	$_1D_3$
$_1O_4$	6	43	$_1D_4$
V_{CC}	7	42	V_{CC}
$_1O_5$	8	41	$_1D_5$
$_1O_6$	9	40	$_1D_6$
GND	10	39	GND
$_1O_7$	11	38	$_1D_7$
$_1O_8$	12	37	$_1D_8$
$_2O_1$	13	36	$_2D_1$
$_2O_2$	14	35	$_2D_2$
GND	15	34	GND
$_2O_3$	16	33	$_2D_3$
$_2O_4$	17	32	$_2D_4$
V_{CC}	18	31	V_{CC}
$_2O_5$	19	30	$_2D_5$
$_2O_6$	20	29	$_2D_6$
GND	21	28	GND
$_2O_7$	22	27	$_2D_7$
$_2O_8$	23	26	$_2D_8$
$_2\overline{OE}$	24	25	$_2$LE

FCT162373-3

TEXAS INSTRUMENTS

Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Inputs (Active HIGH)
$\overline{OE}$	Output Enable Inputs (Active LOW)
O	Three-State Outputs

Function Table[1]

Inputs			Outputs
D	**LE**	**$\overline{OE}$**	**O**
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... Com'l −55°C to +125°C

Ambient Temperature with
Power Applied.................................. Com'l −55°C to +125°C

DC Input Voltage ....−0.5V to +7.0V

DC Output Voltage ....−0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) ....−60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage...>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[7]			±1	µA

Output Drive Characteristics for CY74FCT16373T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Notes:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance. Q_0=Previous state of flip-flop.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A= +25°C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Tested at +25°C.

Output Drive Characteristics for CY74FCT162373T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V, V_{IN}≥V_{CC}−0.2V	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[8]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	60	100	µA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND, LE=V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND, LE=V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	2.4	4.5[11]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[11]	mA

Notes:
8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C= $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC}D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input(V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	CY74FCT16373AT CY74FCT162373AT		Unit	Fig. No.[13]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	5.2	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	6.7	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.1	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.5	ns	1, 7, 8
t_{SU}	Set-Up Time HIGH or LOW, D to LE	2.0		ns	9
t_H	Hold Time HIGH or LOW, D to LE	1.5		ns	9
t_W	LE Pulse Width HIGH	3.3		ns	5
$t_{SK(O)}$	Output Skew[14]		0.5	ns	—

Parameter	Description	CY74FCT16373CT CY74FCT162373CT		Unit	Fig. No.[13]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	4.2	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	5.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.0	ns	1, 7, 8
t_{SU}	Set-Up Time HIGH or LOW, D to LE	2.0		ns	9
t_H	Hold Time HIGH or LOW, D to LE	1.5		ns	9
t_W	LE Pulse Width HIGH	3.3		ns	5
$t_{SK(O)}$	Output Skew[14]		0.5	ns	—

Notes:
12. Minimum limits are specified but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.
14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.
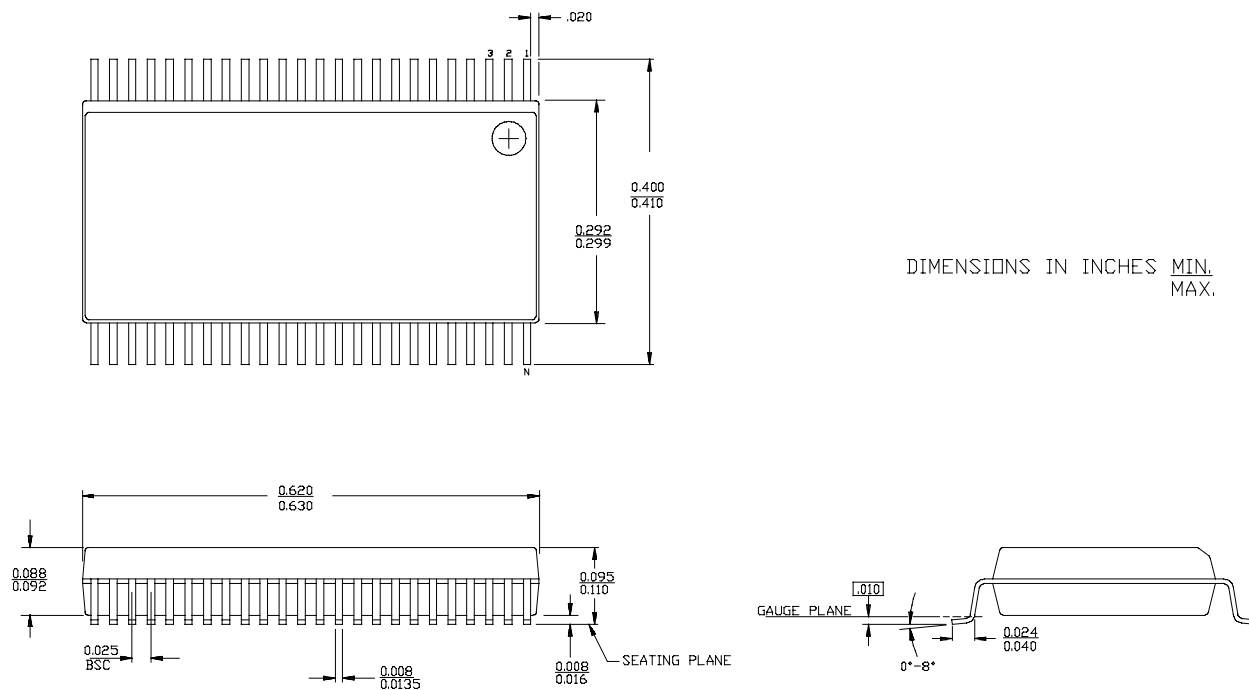
Ordering Information CY74FCT16373

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16373CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16373CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
	CY74FCT16373CTVR	-	48-Lead (173-Mil) TVSOP	
5.2	CY74FCT16373ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16373ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
	CY74FCT16373ATVR	-	48-Lead (173-Mil) TVSOP	

Ordering Information CY74FCT162373

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	74FCT162373CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162373CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162373CTPVCT	O48	48-Lead (300-Mil) SSOP	
5.2	74FCT162373ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162373ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162373ATPVCT	O48	48-Lead (300-Mil) SSOP	

TEXAS INSTRUMENTS

Package Diagrams

48-Lead Shrunk Small Outline Package O48

DIMENSIONS IN INCHES MIN.
MAX.

48-Lead Thin Shrunk Small Outline Package Z48

DIMENSIONS IN INCHES MIN.
MAX.
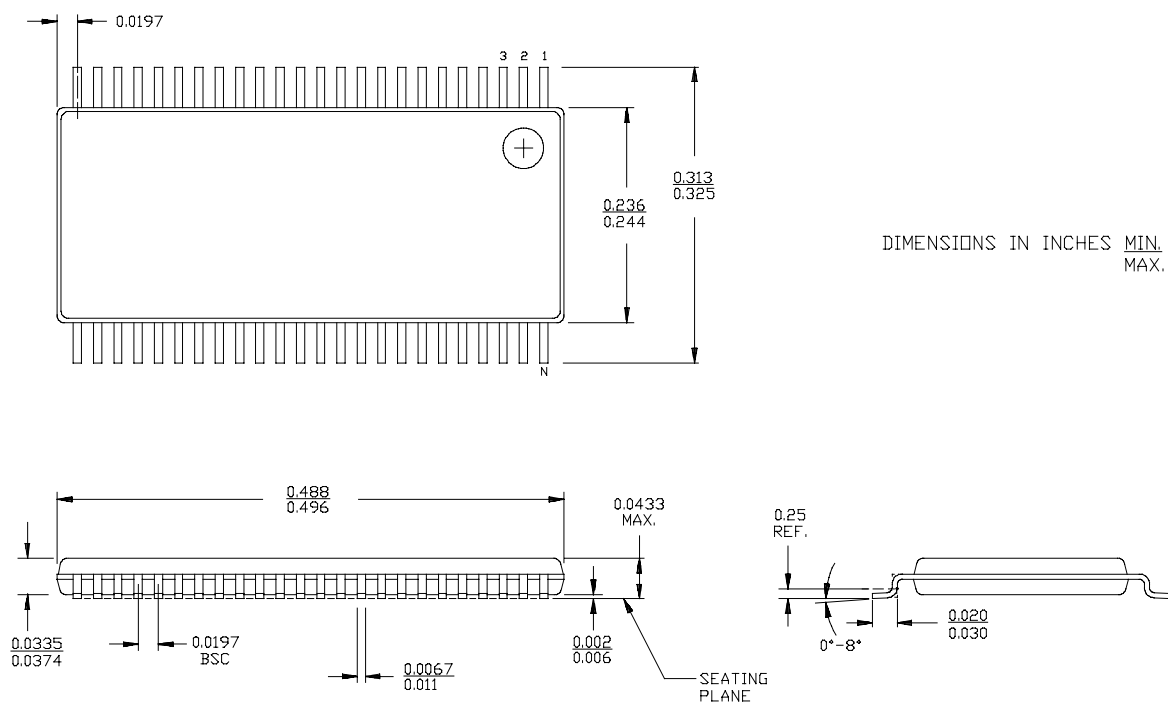
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162373ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	Samples
74FCT162373ATPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	Samples
74FCT162373ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	Samples
74FCT162373CTPACT	ACTIVE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	FCT162373C	Samples
74FCT162373CTPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373C	Samples
74FCT162373ETPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
74FCT162373ETPVCT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
74FCT16373ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	Samples
74FCT16373ATPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	Samples
74FCT16373ATPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	Samples
74FCT16373ATPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	Samples
74FCT16373CTPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373C	Samples
74FCT16373CTPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373C	Samples
74FCT16373CTPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373C	Samples
CY74FCT162373ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	Samples
CY74FCT162373CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373C	Samples
CY74FCT162373ETPAC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT162373ETPVC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16373ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	Samples

9-Aug-2013

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT16373ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	Samples
CY74FCT16373ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	Samples
CY74FCT16373CTPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373C	Samples
CY74FCT16373CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373C	Samples
CY74FCT16373CTVR	ACTIVE	TVSOP	DGV	48		TBD	Call TI	Call TI	-40 to 85	FD373C	Samples
CY74FCT16373CTVRE4	ACTIVE	TVSOP	DGV	48		TBD	Call TI	Call TI	-40 to 85	FD373C	Samples
CY74FCT16373CTVRG4	ACTIVE	TVSOP	DGV	48		TBD	Call TI	Call TI	-40 to 85	FD373C	Samples
CY74FCT16373ETPAC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16373ETPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16373ETPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16373ETPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
FCT162373ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	Samples
FCT162373ATPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	Samples
FCT162373ATPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	Samples
FCT162373CTPACTE4	ACTIVE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	FCT162373C	Samples
FCT162373CTPACTG4	ACTIVE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	FCT162373C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162373ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
74FCT162373ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16373ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
CY74FCT16373ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16373CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL BOX DIMENSIONS
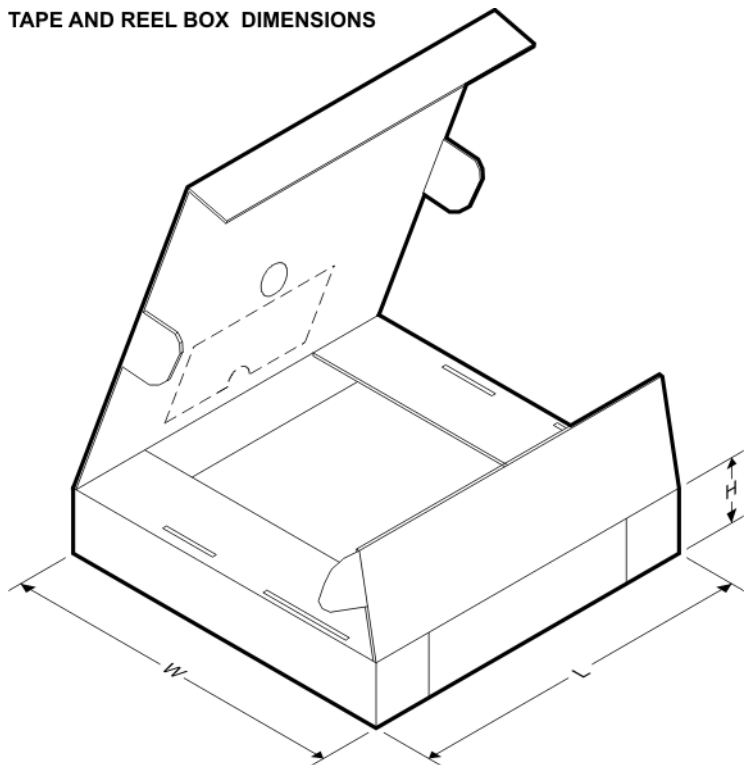
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162373ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
74FCT162373ATPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16373ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT16373ATPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16373CTPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
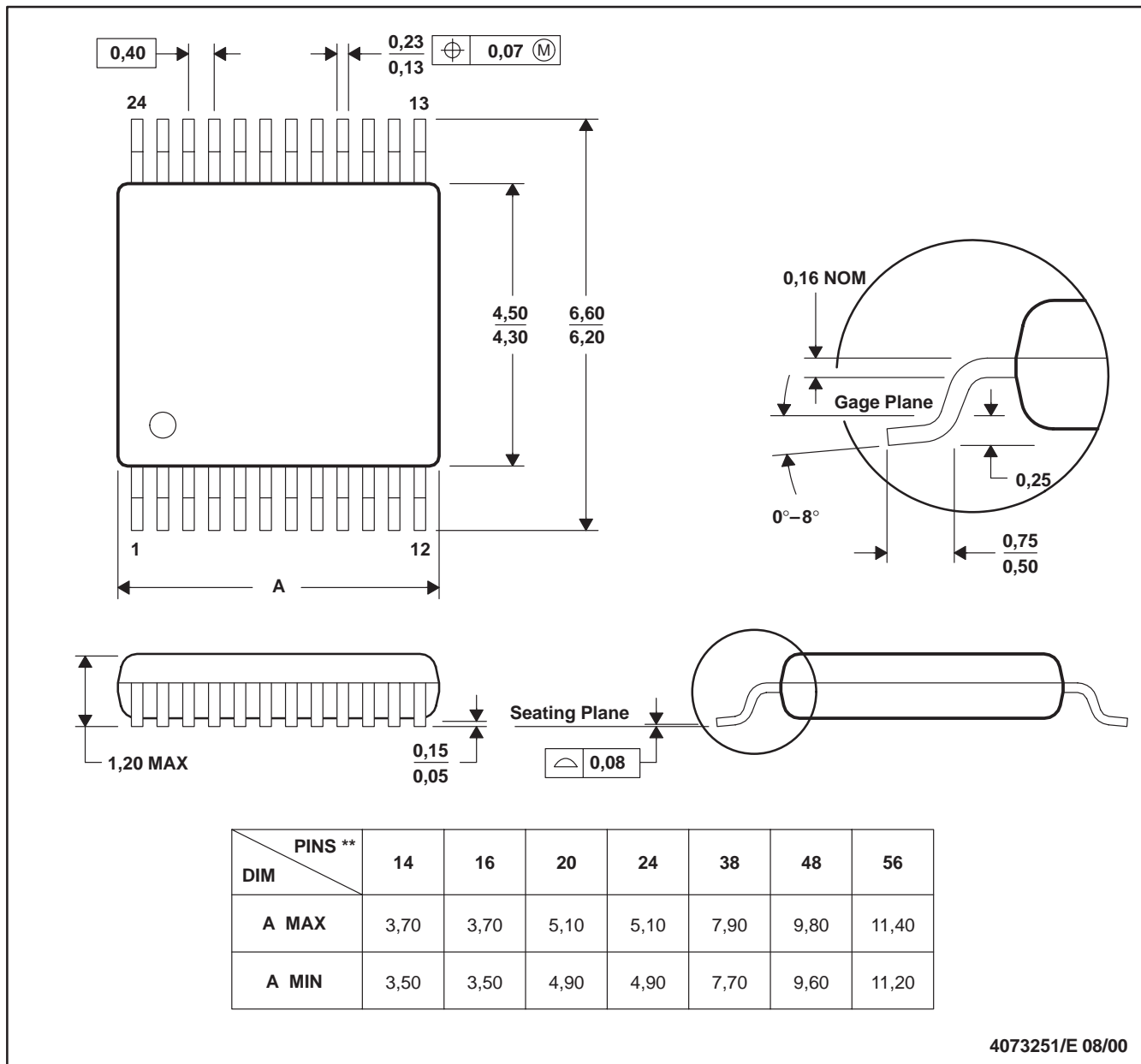
PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
            D. Falls within JEDEC: 24/48 Pins – MO-153
                                14/16/20/56 Pins – MO-194

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

$\frac{0.0135\ (0,343)}{0.008\ (0,203)}$

⊕ 0.005 (0,13) Ⓜ

48   25

$\frac{0.420\ (10,67)}{0.395\ (10,03)}$

$\frac{0.299\ (7,59)}{0.291\ (7,39)}$

1   24

$\frac{0.630\ (16,00)}{0.620\ (15,75)}$

$\frac{0.010\ (0,25)}{0.005\ (0,13)}$

Gage Plane

0.010 (0,25)

0°−8°

$\frac{0.040\ (1,02)}{0.020\ (0,51)}$

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−3/F   05/13
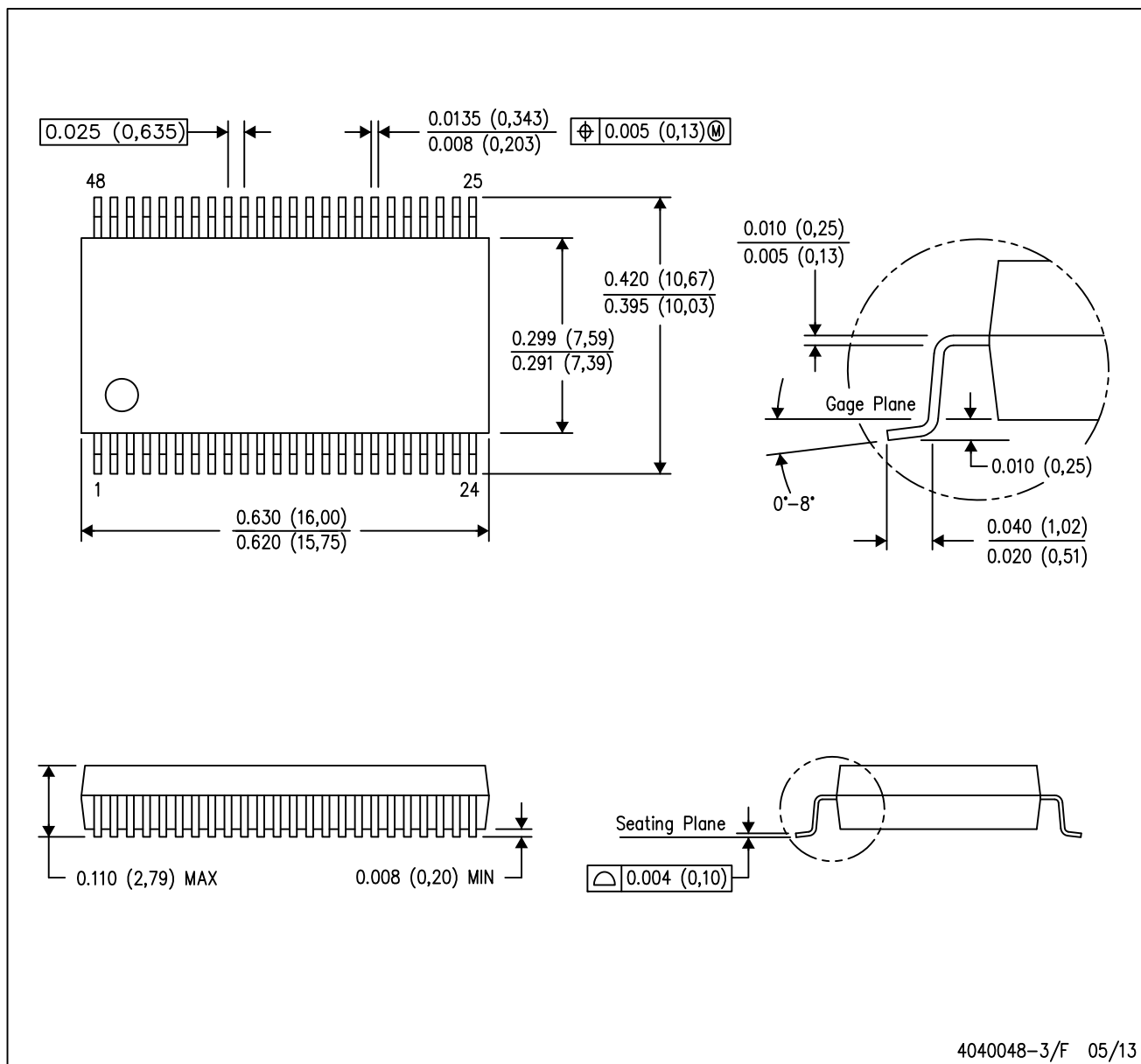
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO−118

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DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN
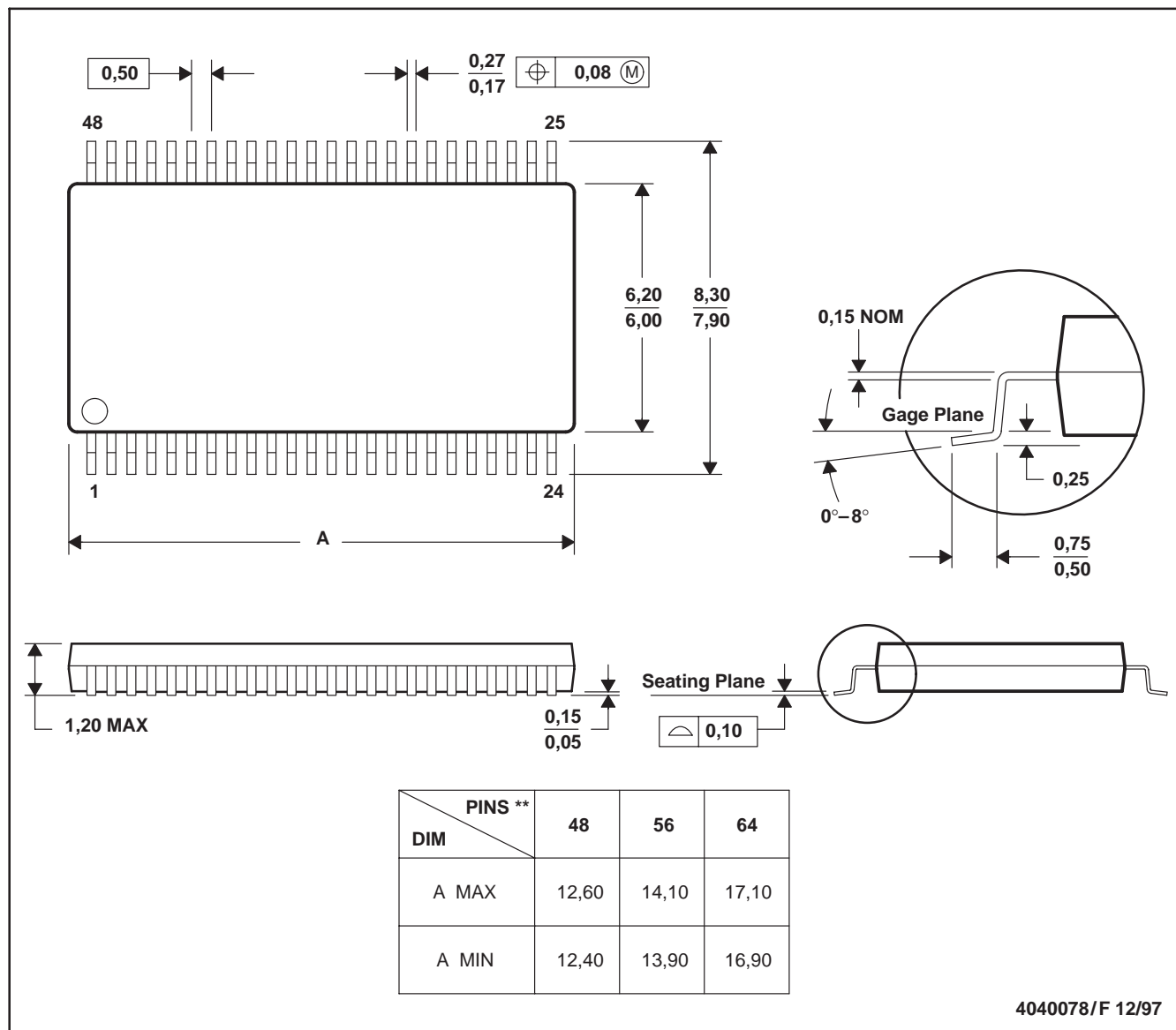
PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold protrusion not to exceed 0,15.
          D. Falls within JEDEC MO-153

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