133-MHz CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS WITH 3-STATE OUTPU

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 Supports Pentium III™ Class Motherboards Uses a 14.318-MHz Crystal Input to 	DL PAC (TOP	CKAGE VIEW)
Generate Multiple Output Frequencies	GND 1	56 V _{DD} 2.5V
 Includes Spread Spectrum Clocking (SSC), 	REF0	55 APIC2
0.5% Downspread for Reduced EMI	REF1] 3	54 APIC1
Performance	V _{DD} 3.3V [4	53 APIC0
 Power Management Control Terminals 	XIN 🛮 5	52] GND
 Low Output Skew and Jitter for Clock 	XOUT [6	51 V _{DD} 2.5V
Distribution	GND 🛛 7	50 CPU_DIV2(1)
2.5-V and 3.3-V Supplies	PCI_F [] 8	49 CPU_DIV2(0)
Generates the Following Clocks:	PCI1 9	48 GND
- 4 CPU (2.5 V, 100/133 MHz)	V _{DD} 3.3V 1 10	47 V _{DD} 2.5V
- 7 PCI (3.3 V, 33.3 MHz)	PCI2 11	46 CPU3
 1 PCI_F (Free Running, 3.3 V, 33.3 MHz) 	PCl3	45] CPU2 44] GND
- 2 CPU/2 (2.5 V, 50/66 MHz)	PCI4 14	43 V _{DD} 2.5V
- 3 APIC (2.5 V, 16.67 MHz)	PCI5 15	42 VDD2.3V 42 CPU1
- 4 3V66 (3.3 V, 66 MHz)	V _{DD} 3.3V 16	41 CPU0
2 REF (3.3 V, 14.318 MHz)1 48MHz (3.3 V, 48 MHz)	PCI6 17	40 GND
	PCI7 18	39 V _{DD} 3.3V
Packaged in 56-Pin SSOP Package	GND 19	38 GND
 Designed for Use with TI's Direct Rambus™ 	GND 1 20	37 PCI_STOP
Clock Generators (CDCR81, CDCR82,	3V66(0) [21	36 CPU_STOP
CDCR83)	3V66(1) [22	35 PWR_DWN
description	V _{DD} 3.3V [23	34 SPREAD
accomplian	GND [24	33 SEL1
The CDC924 is a clock synthesizer/driver that	3V66(2) 25	32 SEL0
generates system clocks necessary to support	3V66(3) 26	31 🛛 V _{DD} 3.3V

3V66, PCI, APIC, 48MHz, and REF clock signals. All output frequencies are generated from a

Intel Pentium III systems on CPU, CPU_DIV2,

14.318-MHz crystal input. A reference clock input instead of a crystal can be provided at the XIN input. Two phase-locked loops (PLLs) are used, one to generate the host frequencies and the other to generate the 48-MHz clock frequency. On-chip loop filters and internal feedback loops eliminate the need for external components.

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 $V_{DD}3.3V$

SEL133/100

The host and PCI clock outputs provide low-skew and low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected via control inputs SEL0, SEL1, and SEL133/100.

The outputs are either 3.3-V or 2.5-V single-ended CMOS buffers. With a logic high-level on the PWR_DWN terminal, the device operates normally, but when a logical low-level input is applied, the device powers down completely, with the outputs in a low-level output state. When a high-level is applied to the PCI STOP or CPU STOP, the outputs operate normally. With a low-level applied to the PCI STOP or CPU STOP terminals, the PCI or CPU and 3V66 outputs, respectively, are held in a low-level state.

The CPU bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with corresponding setting for SEL133/ $\overline{100}$ control input. The PCI bus frequency is fixed to 33MHz.



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¶ 48MHz

GND

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description (continued)

Since the CDC924 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL. This stabilization time is required after power up or after changes to the SEL inputs are made. With use of an external reference clock, this signal must be fixed-frequency and fixed-phase before the stabilization time starts.

function tables

SELECT FUNCTIONS

I	NPUTS					OUTPUT	5			
SEL133/ 100	SEL1	SEL0	CPU	CPU_DIV2	3V66	PCI, PCI_F	48MHz	REF	APIC	FUNCTION
L	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	3-state
L	L	Н	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
L	Н	L	100 MHz	50 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
L	Н	Н	100 MHz	50 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on
Н	L	L	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	Test
Н	L	Н	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
Н	Н	L	133 MHz	66 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
Н	Н	Н	133 MHz	66 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on

ENABLE FUNCTIONS

	INPUTS			OUTPUTS						INTERNAL	
CPU_STOP	PWR_DWN	PCI_STOP	CPU	CPU_DIV2	APIC	3V66	PCI	PCI_F	REF, 48MHz	Crystal	VCOs
Х	L	Χ	L	L	L	L	L	L	L	Off	Off
L	Н	L	L	On	On	L	L	On	On	On	On
L	Н	Н	L	On	On	L	On	On	On	On	On
Н	Н	L	On	On	On	On	L	On	On	On	On
Н	Н	Н	On	On	On	On	On	On	On	On	On

OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V _{DD} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
CPU, CPU_DIV2, APIC	2.375 – 2.625	13.5 – 45	TYPE 1
48MHz, REF	3.135 – 3.465	20 – 60	TYPE 3
PCI, PCI_F, 3V66	3.135 - 3.465	12 – 55	TYPE 5



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Terminal Functions

TERMI	NAL		
NAME	NO.	I/O	DESCRIPTION
3V66 [0-3]	21, 22, 25, 26	0	3.3 V, Type 5, 66-MHz clock outputs
48MHz	30	0	3.3 V, Type 3, 48-MHz clock output
APIC [0-2]	53, 54, 55	0	2.5 V, Type 1, APIC clock outputs
CPU [0-3]	41, 42, 45, 46	0	2.5 V, Type 1, CPU clock outputs
CPU_DIV2 [0-1]	49, 50	0	2.5 V, Type 1, CPU_DIV2 clock outputs
CPU_STOP	36	I	Disables CPU clock to low state
GND	1, 7, 13, 19, 20, 24, 29, 38, 40, 44, 48, 52		Ground
PCI [1-7]	9, 11, 12, 14, 15, 17, 18	0	3.3 V, Type 5, 33-MHz PCI clock outputs
PCI_F	8	0	Free-running 3.3-V, Type 5, 33-MHz PCI clock output
PCI_STOP	37	I	Disables PCI clock to low state
PWR_DWN	35	I	Power down for complete device with outputs forced low
REF0, REF1	2, 3	0	3.3 V, Type 3, 14.318-MHz reference clock output
SEL0, SEL1	32, 33	I	LVTTL level logic select terminals for function selection
SEL133/100	28	I	LVTTL level logic select pins for enabling 100/133 MHz
SPREAD	34	I	Disables SSC function
V _{DD} 3.3V	4, 10, 16, 23, 27, 31, 39		Power for the 3V66, 48MHz, PCI, REF outputs and CORE logic
V _{DD} 2.5V	43, 47, 51, 56		Power for CPU and APIC outputs
XIN	5	I	Crystal input – 14.318 MHz
XOUT	6	0	Crystal output – 14.318 MHz



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spread spectrum clock (SSC) implementation for CDC924

Simultaneously switching at fixed frequency generates a significant power peak at the selected frequency, which in turn will cause EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU-PLL allows to distribute the energy to many different frequencies which reduces the power peak. A typical characteristic for a single frequency spectrum and a frequency modulated spectrum is shown in Figure 1.

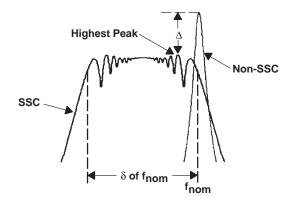


Figure 1. Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution left hand to the single frequency spectrum which indicates a "down-spread modulation".

The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation was driven to keep the average clock frequency closed to its upper specification limit. The modulation amount was set to approximately –0.5%.

In order to allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC induced tracking skew jitter. The ideal modulation profile used for CDC924 is shown in Figure 2.

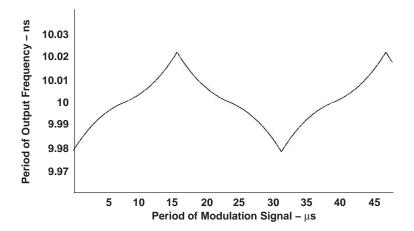
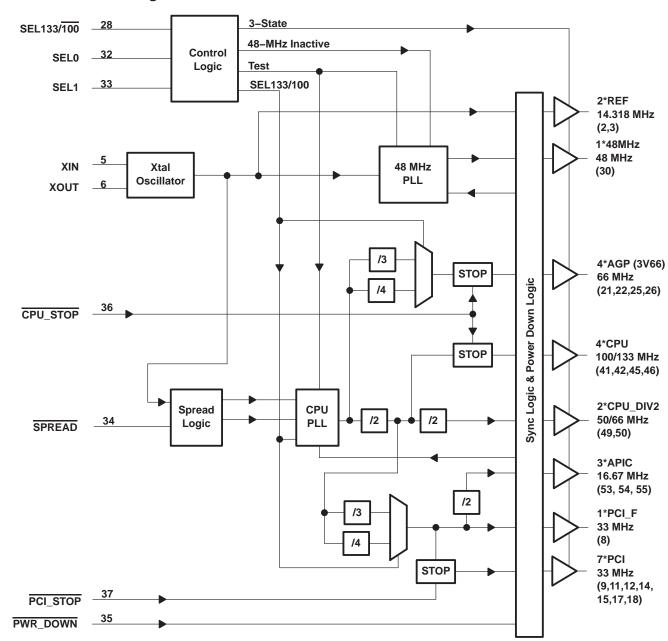


Figure 2. SSC Modulation Profile



functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATNG	DERATING FACTOR [†] ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DL	1558.6 mW	12.468 mW/°C	997.5 mW	810.52 mW

[†] This is the inverse of the traditional junction-to-case thermal resistance (R_{θJA}) and uses a board-mounted device at 80.2°C/W.

recommended operating conditions (see Note 2)

		MIN	иом†	MAX	UNIT
	3.3 V	3.135		3.465	.,
Supply voltage, V _{DD}	2.5 V	2.375		2.625	V
High-level input voltage, V _{IH}		2		V _{DD} + 0.3 V	V
Low-level input voltage, V _{IL}		GND – 0.3 V		0.8	V
Input voltage, V _I		0		V_{DD}	V
	CPUx, CPU_DIV2x			-12	
High lavel autout aumont I	APICx			-12	A
High-level output current, IOH	48MHz, REFx			-14	mA
	PCIx, PCI_F, 3V66x			-18	
	CPUx, CPU_DIV2x			12	
Law book outside comment to	APICx			12	4
Low-level output current, IOL	48MHz, REFx			9	mA
	PCIx, PCI_F, 3V66x			12	
Reference frequency, f(XIN) [‡]	Test mode		130		MHz
Crystal frequency, f(XTAL)§	Normal mode	13.8	14.318	14.8	MHz
Operating free-air temperature, T _A		0		85	°C

NOTE 2: Unused inputs must be held high or low to prevent them from floating.



[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[†] All nominal values are measured at their respective nominal VDD values.

[‡] Reference frequency is a test clock driven on the XIN input during the device test mode and normal mode. In test mode, XIN can be driven externally up to f(XIN) = 130 MHz. If XIN is driven externally, XOUT is floating.

[§] This is a series fundamental crystal with $f_O = 14.31818$ MHz.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CO	ONDITIONS	MIN	TYP†	MAX	UNIT	
٧ıK	Input clamp voltage		$V_{DD} = 3.135 \text{ V},$	I _I = -18 mA			-1.2	V	
R _I	Input resistance	XIN-XOUT	V _{DD} = 3.465 V,	$V_I = V_{DD} - 0.5 V$	80		350	kΩ	
		XOUT	$V_{DD} = 3.135 \text{ V},$	$V_I = V_{DD} - 0.5 V$		20	50	mA	
ΙΗ	High-level input current	SEL0, SEL1, CPU_STOP, PCI_STOP, SPREAD	V _{DD} = 3.465 V,	$V_I = V_{DD}$		<10	10	μΑ	
		PWR_DWN	$V_{DD} = 3.465 \text{ V},$	$V_I = V_{DD}$		<10	10	μΑ	
		SEL133/100	V _{DD} = 3.465 V,	$V_I = V_{DD}$		<10	10	μΑ	
		XOUT	$V_{DD} = 3.135 \text{ V},$	V _O = 0 V		-2	-5	mA	
IIL	Low-level input current	SEL0, SEL1, CPU_STOP, PCI_STOP, SPREAD	V _{DD} = 3.465 V,	V _I = GND		<10	-10	μΑ	
		PWR_DWN	V _{DD} = 3.465 V,	V _I = GND		<10	-10	μΑ	
		SEL133/100	$V_{DD} = 3.465 \text{ V},$	$V_I = GND$		<10	-10	μΑ	
loz	High-impedance-state output cu	rrent	$ V_{DD} = \max,$	$V_O = V_{DD}$ or GND			±10	μΑ	
			V _{DD} = 2.625 V, All outputs = low	$\overline{PWR_DWN} = low,$		<20	100	0	
lDD	Supply current		$V_{DD} = 2.625 \text{ V},$ All outputs = high	$V_{DD}x = 2.5 V,$		<20	100	μΑ	
			V _{DD} = 3.465 V, All outputs = low	$\overline{PWR_DWN} = low,$		<50	200		
			V _{DD} = 3.465 V,	All outputs = high		12	35	mA	
	High impodence state surely so		V _{DD} = 2.625 V				1.4	A	
I _{DD} (Z)	High-impedance-state supply current		V _{DD} = 3.465 V				28	mA	
	Dynamic supply current		C _L = 20 pF,	V _{DD} = 3.465 V		114	146	mA	
	Бупанію зарріў санені		CPU = 133 MHz	V _{DD} = 2.625 V		52	70	ША	
Cl	Input capacitance		$V_{DD} = 3.3 V,$	$V_I = V_{DD}$ or GND	3.3		5.8	pF	
	Crystal terminal capacitance		$V_{DD} = 3.3 \text{ V},$	V _I = 0.3 V	18	18.5	22.5	pF	

[†] All typical values are measured at their respective nominal V_{DD} values.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

CPUx, CPU_DIV2x, APICx (Type 1)

	PARAMETER		TEST CO	NDITIONS	MIN	TYP [†]	MAX	UNIT
VOH	V _{OH} High-level output voltage		V _{DD} = min to max,	I _{OH} = -1 mA	VDD – 0.1 V			V
			V _{DD} = 2.375 V,	$I_{OH} = -12 \text{ mA}$	2			
\/ - ·	Laurianal autaut valtana		V _{DD} = min to max,	I _{OL} = 1 mA			0.1	٧
VOL	Low-level output voltage		V _{DD} = 2.375 V,	I _{OL} = 12 mA		0.18	0.4	V
			V _{DD} = 2.375 V,	V _O = 1 V	-26	-42		
lOH	IOH High-level output current		$V_{DD} = 2.5 V,$	V _O = 1.25 V		-46		mA
			$V_{DD} = 2.625 V$,	V _O = 2.375 V		-16	-27	
			$V_{DD} = 2.375 V$,	V _O = 1.2 V	27	57		
loL	Low-level output current		$V_{DD} = 2.5 V,$	V _O = 1.25 V		63		mA
			$V_{DD} = 2.625 V$,	V _O = 0.3 V		23	43	
CO	Output capacitance		$V_{DD} = 3.3 V,$	$V_O = V_{DD}$ or GND	6		8.5	pF
70	Output impedance	High state	$V_{O} = 0.5 V_{DD}$	Vo/IoH	13.5	27	45	
ZO		Low state	$V_{O} = 0.5 V_{DD}$	V _O /I _{OL}	13.5	20	45	Ω

[†] All typical values are measured at their respective nominal V_{DD} values.

48MHz, REFx (Type 3)

	PARAMETER		TEST CO	NDITIONS	MIN	TYP [†]	MAX	UNIT
Vон	High-level output voltage		V _{DD} = min to max,	I _{OH} = -1 mA	VDD – 0.1 V			V
			V _{DD} = 3.135 V,	I _{OH} = -14 mA	2.4			
\/-·	Laurianal andmitticaltana		V _{DD} = min to max,	I _{OL} = 1 mA			0.1	V
VOL	Low-level output voltage		$V_{DD} = 3.135 V,$	$I_{OL} = 9 \text{ mA}$		0.18	0.4	V
			V _{DD} = 3.135 V,	V _O = 1 V	-27	-41		
IOH	IOH High-level output current		$V_{DD} = 3.3 \text{ V},$	V _O = 1.65 V		-41		mA
			V _{DD} = 3.465 V,	V _O = 3.135 V		-12	-23	
			$V_{DD} = 3.135 V,$	V _O = 1.95 V	29	50		
lOL	Low-level output current		$V_{DD} = 3.3 \text{ V},$	V _O = 1.65 V		53		mA
			V _{DD} = 3.465 V,	V _O = 0.4 V		20	37	
CO	CO Output capacitance		$V_{DD} = 3.3 \text{ V},$	$V_O = V_{DD}$ or GND	4.5		7	pF
7 -	Output impedance	High state	$V_{O} = 0.5 V_{DD}$	V _O /I _{OH}	20	40	60	0
ZO	Output impedance	Low state	$V_{O} = 0.5 V_{DD}$	V _O /I _{OL}	20	31	60	Ω

 $[\]dagger$ All typical values are measured at their respective nominal V_{DD} values.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PCIx, PCI_F, 3V66x (Type 5)

	PARAMETER		TEST CO	NDITIONS	MIN	TYP [†]	MAX	UNIT
VOH	High-level output voltage		V _{DD} = min to max,	I _{OH} = -1 mA	VDD – 0.1 V			V
			V _{DD} = 3.135 V,	$I_{OH} = -18 \text{ mA}$	2.4			
V	Laurianal antonit nalta aa		V _{DD} = min to max,	I _{OL} = 1 mA			0.1	.,
VOL	Low-level output voltage		V _{DD} = 3.135 V,	I _{OL} = 12 mA		0.15	0.4	V
			V _{DD} = 3.135 V,	V _O = 1 V	-33	-53		
ІОН	IOH High-level output current		$V_{DD} = 3.3 V,$	V _O = 1.65 V		-53		mA
			V _{DD} = 3.465 V,	V _O = 3.135 V		-16	-33	
			$V_{DD} = 3.135 V,$	V _O = 1.95 V	30	67		
lOL	Low-level output current		$V_{DD} = 3.3 V,$	V _O = 1.65 V		70		mA
			V _{DD} = 3.465 V,	V _O = 0.4 V		27	49	
CO	Output capacitance		$V_{DD} = 3.3 \text{ V},$	$V_O = V_{DD}$ or GND	4.5		7.5	pF
70	Output impedance	High state	$V_{O} = 0.5 V_{DD}$	Vo/IoH	12	31	55	Ω
ZO	Output impedance	Low state	$V_{O} = 0.5 V_{DD}$	V _O /I _{OL}	12	24	55	52

[†] All typical values are measured at their respective nominal V_{DD} values.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Overshoot/undershoot		GND - 0.7 V		V _{DD} + 0.7 V	V
	Ring back		V _{IL} – 0.1 V		V _{IH} + 0.1 V	V
	Stabilization time, PWR_DWN to PCIx	f(CPU) = 133 MHz		0.05	3	ms
t _{dis3}	Disable time, PWR_DWN to PCIx	f _(CPU) = 133 MHz		50		ns
	Stabilization time, PWR_DWN to CPUx	f _(CPU) = 133 MHz		0.03	3	ms
t _{dis4}	Disable time, PWR_DWN to CPUx	f _(CPU) = 133 MHz		50		ns
	0.131.0.0.1	After SEL1, SEL0			3	
	Stabilization time†	After power up			3	ms

The Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time from when VDD achieves its nominal operating level until the output frequency is stable and operating within specification.



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switching characteristics, V_{DD} = 2.375 V to 2.625 V, T_A = 0°C to 85°C (continued)

CPUx

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{en1}	Output enable time	SEL133/100	CPUx	f _(CPU) = 100 or 133MHz		6	10	ns
tdis1	Output disable time	SEL133/100	CPUx	f _(CPU) = 100 or 133MHz		8	10	ns
	c CPU clock period [†]			f _(CPU) = 100 MHz	10	10.04	10.2	ns
t _C	СРО сюск репост			f _(CPU) = 133 MHz	7.5	7.53	7.7	ns
	Cycle to cycle jitter			f _(CPU) = 100 or 133MHz			300	ps
	Duty cycle			f _(CPU) = 100 or 133MHz	45%		55%	
t _{sk(o)}	CPU bus skew	CPUx	CPUx	f _(CPU) = 100 or 133MHz		50	175	ps
t _{sk(p)}	CPU pulse skew	CPUn	CPUn	f _(CPU) = 100 or 133MHz			2.2	ns
t(off)	CPU clock to APIC clock offset, rising edge	е			1.5	2.8	4	ns
t(off)	CPU clock to 3V66 clock offset, rising edge	е			0	0.75	1.5	ns
	Dulas dimetica midth high			f _(CPU) = 100 MHz	2.6	4.3		
t _{w1}	Pulse duration width, high			f _(CPU) = 133 MHz	1.4	3.7		ns
	Dulas dimetias midth land			f _(CPU) = 100 MHz	2.8	4.3		
t _{w2}	Pulse duration width, low			f(CPU) = 133 MHz	1.7	4		ns
t _r	Rise time			V _O = 0.4 V to 2.0 V	0.4	1.5	2.2	ns
tf	Fall time		_	V _O = 0.4 V to 2.0 V	0.4	1.4	2	ns

[†] The average over any 1-µs period of time is greater than the minimum specified period.

CPU DIV2x

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{en1}	Output enable time	SEL133/100	CPU_DIV2x	f(CPU) = 100 or 133MHz		6	10	ns
tdis1	Output disable time	SEL133/100	CPU_DIV2x	f(CPU) = 100 or 133MHz		8	10	ns
	CDLL DIVO algala navia di			f(CPU) = 100 MHz	20	20.08	20.4	ns
t _C	CPU_DIV2 clock period†			f(CPU) = 133 MHz	15	15.06	15.3	ns
	Cycle to cycle jitter			f(CPU) = 100 or 133MHz			300	ps
	Duty cycle			f(CPU) = 100 or 133MHz	45%		55%	
tsk(o)	CPU_DIV2 bus skew	CPU_DIV2x	CPU_DIV2x	f(CPU) = 100 or 133MHz		50	175	ps
t _{sk(p)}	CPU_DIV2 pulse skew	CPU_DIV2n	CPU_DIV2n	f _(CPU) = 100 or 133MHz			1.6	ns
	B			f(CPU) = 100 MHz	7.1			
tw1	Pulse duration width, high			f(CPU) = 133 MHz	4.7			ns
	Dulan diseast an estable form			f(CPU) = 100 MHz	7.3	8.9		
t _{w2}	Pulse duration width, low			f(CPU) = 133 MHz	5	6.6		ns
t _r	Rise time			V _O = 0.4 V to 2.0 V	0.4	1.4	2	ns
t _f	Fall time			V _O = 0.4 V to 2.0 V	0.4	1.3	1.8	ns

[†] The average over any 1-μs period of time is greater than the minimum specified period.



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switching characteristics, V_{DD} = 2.375 V to 2.625 V, T_{A} = 0°C to 85°C (continued)

APIC

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{en1}	Output enable time	SEL133/100	APICx	f _(APIC) = 16.67 MHz		6	10	ns
tdis1	Output disable time	SEL133/100	APICx	f(APIC) = 16.67 MHz		8	10	ns
t _C	APIC clock period [†]			f(APIC) = 16.67 MHz	60	60.24	60.6	ns
	Cycle to cycle jitter			f(CPU) = 100 or 133 MHz			400	ps
	Duty cycle	f(APIC) = 16.67 MHz	45%		55%			
tsk(o)	APIC bus skew	APICx	APICx	f(APIC) = 16.67 MHz		30	100	ps
t _{sk(p)}	APIC pulse skew	APICn	APICn	f(APIC) = 16.67 MHz			3	ns
t(off)	APIC clock to CPU clock offset, rising edge	APICx	CPUx		-1.5		-4	ns
t _{w1}	Pulse duration width, high			f(APIC) = 16.67 MHz	25.5	28		ns
t _{w2}	Pulse duration width, low			f _(APIC) = 16.67 MHz	25.3	29.2		ns
t _r	Rise time			V _O = 0.4 V to 2 V	0.4	1.6	2.1	ns
t _f	Fall time			V _O = 0.4 V to 2 V	0.4	1.2	1.7	ns

[†] The average over any 1-µs period of time is greater than the minimum specified period.

switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C

3V66

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ten1	Output enable time	SEL133/100	3V66x	f _(3V66) = 66 MHz		6	10	ns
t _{dis1}	Output disable time	SEL133/100	3V66x	f _(3V66) = 66 MHz		8	10	ns
t _C	3V66 clock period [†]			f(3V66) = 66 MHz	15	15.06	15.3	ns
	Cycle to cycle jitter			f(CPU) = 100 or 133 MHz			400	ps
	Duty cycle			f(3V66) = 66 MHz	45%		55%	
t _{sk(o)}	3V66 bus skew	3V66x	3V66x	f(3V66) = 66 MHz		50	150	ps
t _{sk(p)}	3V66 pulse skew	3V66n	3V66n	f _(3V66) = 66 MHz			2.6	ns
t(off)	3V66 clock to CPU clock offset	3V66x	CPUx		0	-0.75	-1.5	ns
t(off)	3V66 clock to PCI clock offset, ris	sing edge			1.2	2.1	3	ns
t _{w1}	Pulse duration width, high			f(3V66) = 66 MHz	5.2			ns
t _{w2}	Pulse duration width, low			f(3V66) = 66 MHz	5			ns
t _r	Rise time			V _O = 0.4 V to 2 V	0.5	1.5	2	ns
t _f	Fall time			V _O = 0.4 V to 2 V	0.5	1.5	2	ns

 $[\]mbox{†}$ The average over any 1- μs period of time is greater than the minimum specified period.

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switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C (continued)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{en1}	Output enable time	SEL133/100	48MHz	f _(48MHz) = 48 MHz		6	10	ns
tdis1	Output disable time	SEL133/100	48MHz	f _(48MHz) = 48 MHz		8	10	ns
t _C	48MHz clock period [†]			f(48MHz) = 48 MHz	20.5	20.83	21.1	ns
	Cycle to cycle jitter			f(CPU) = 100 or 133 MHz			500	ps
	Duty cycle		f _(48MHz) = 48 MHz	45%		55%		
tsk(p)	48MHz pulse skew	48MHz	48MHz	f _(48MHz) = 48 MHz			3	ns
t _{w1}	Pulse duration width, high			f _(48MHz) = 48 MHz	7.8			ns
t _{w2}	Pulse duration width, low			f _(48MHz) = 48 MHz	7.8			ns
t _r	Rise time			$V_0 = 0.4 \text{ V to 2 V}$	1	2.1	2.8	ns
tf	Fall time		_	V _O = 0.4 V to 2 V	1	1.9	2.8	ns

[†] The average over any 1-μs period of time is greater than the minimum specified period.

REF

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ten1	Output enable time	SEL133/100	REFx	f(REF) = 14.318 MHz		6	10	ns
^t dis1	Output disable time	SEL133/100	REFx	f(REF) = 14.318 MHz		8	10	ns
t _C	REF clock period [†]			f(REF) = 14.318 MHz		69.84		ns
	Cycle to cycle jitter			f _(CPU) = 100 or 133 MHz			700	ps
	Duty cycle	f _(REF) = 14.318 MHz	45%		55%			
tsk(o)	REF bus skew	REFx	REFx	f(REF) = 14.318 MHz		150	250	ps
tsk(p)	REF pulse skew	REFn	REFn	f(REF) = 14.318 MHz			2	ns
tw1	Pulse duration width, high			f(REF) = 14.318 MHz	26.2	32.7		ns
t _{w2}	Pulse duration width, low			f(REF) = 14.318 MHz	26.2	31.2		ns
t _r	Rise time			V _O = 0.4 V to 2 V	1	2	2.8	ns
t _f	Fall time			V _O = 0.4 V to 2 V	1	1.9	2.8	ns

[†] The average over any 1-μs period of time is greater than the minimum specified period.



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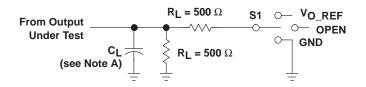
switching characteristics, V_{DD} = 3.135 V to 3.465 V, T_A = 0°C to 85°C (continued)

PCI, PCI_F

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ten1	Output enable time	SEL133/100	PCIx	f _(PCI) = 33 MHz		6	10	ns
tdis1	Output disable time	SEL133/100	PCIx	f _(PCI) = 33 MHz		8	10	ns
t _C	PCIx clock period [†]			f _(PCI) = 33 MHz	30	30.12	30.5	ns
	Cycle to cycle jitter			f _(CPU) = 100 or 133 MHz			300	ps
	Duty cycle	f _(PCI) = 33 MHz	45%		55%			
t _{sk(o)}	PCIx bus skew	PCIx	PCIx	f _(PCI) = 33 MHz		70	300	ps
t _{sk(p)}	PCIx pulse skew	PCIn	PCIn	f _(PCI) = 33 MHz			4	ns
t(off)	PCIx clock to 3V66 clock offset				-1.2		-3	ns
t _{w1}	Pulse duration width, high			f _(PCI) = 33 MHz	12			ns
t _{w2}	Pulse duration width, low			f _(PCI) = 33 MHz	12			ns
t _r	Rise time			V _O = 0.4 V to 2 V	0.5	1.6	2	ns
t _f	Fall time			V _O = 0.4 V to 2 V	0.5	1.5	2	ns

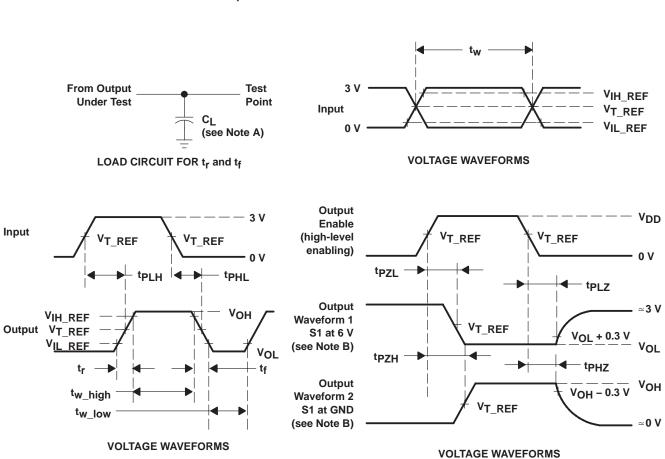
[†] The average over any 1-µs period of time is greater than the minimum specified period.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VO_REF
tPHZ/tPZH	GND

LOAD CIRCUIT for tpd and tsk



NOTES: A. C_I includes probe and jig capacitance. C_I = 20 pF (CPUx, APICx, 48MHz, REF), C_I = 30 pF (PCIx, 3V66)

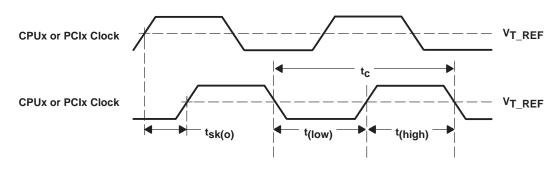
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 14.318 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.

	PARAMETER	3.3-V INTERFACE	2.5-V INTERFACE	UNIT
VIH_REF	High-level reference voltage	2.4	2	V
VIL_REF	Low-level reference voltage	0.4	0.4	V
VT_REF	Input Threshold reference voltage	1.5	1.25	V
VO_REF	Off-state reference voltage	6	4.6	V

Figure 3. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION



$$t_{sk(p)} = |t_{PLH}^{-t}_{PHL}|$$

Duty Cycle =
$$\frac{t(low \ or \ high)}{t_C} \times 100$$

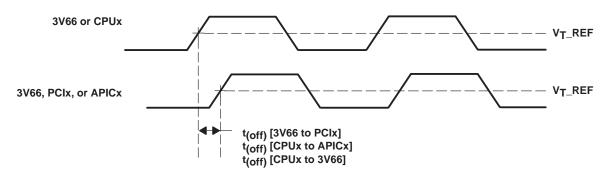


Figure 4. Waveforms for Calculation of Skew, Offset, and Jitter

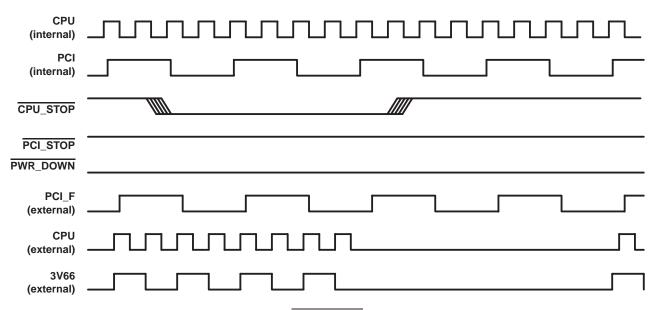
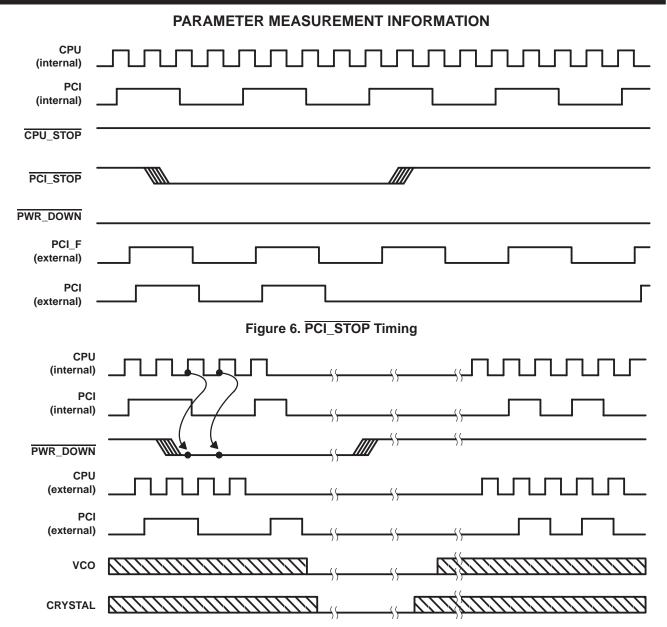


Figure 5. CPU_STOP Timing

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NOTE A: Shaded sections on the VCO and Crystal waveforms indicate that the VCO and crystal oscillators are active and there is a valid clock.

Figure 7. Power-Down Timing



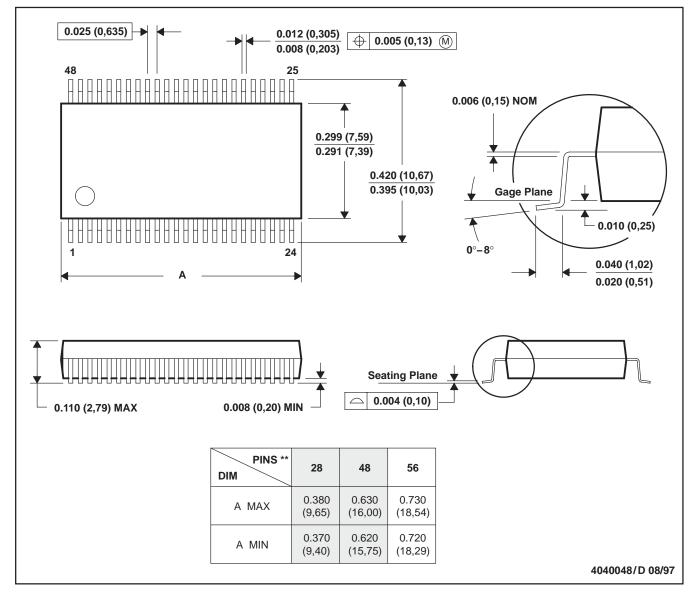
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MECHANICAL DATA

DL (R-PDSO-G**)

48-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: B. All linear dimensions are in inches (millimeters).

- C. This drawing is subject to change without notice.
- D. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- E. Falls within JEDEC MO-118





com 31-Jul-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC924DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDC924DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDC924DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDC924DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

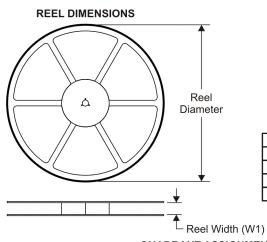
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

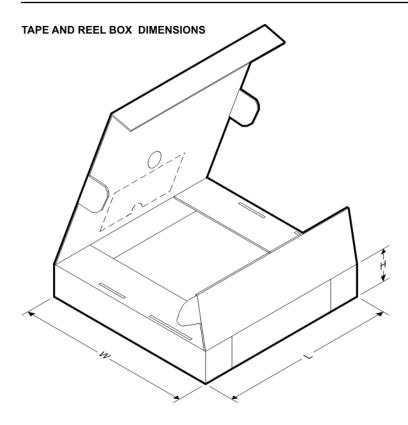
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC924DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC924DLR	SSOP	DL	56	1000	333.2	345.9	41.3

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