

NOT RECOMMENDED FOR NEW DESIGNS

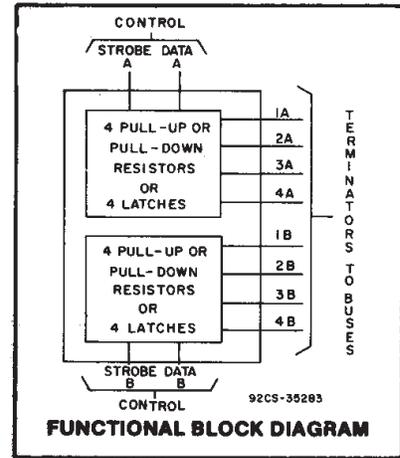
CD40117B Types

Programmable Dual 4-Bit Terminator

High-Voltage Types (20-Volt Rating)

Features:

- One standard "B" output will drive eight terminator circuits.
- Will terminate a CMOS data bus with up to 40 B-series inputs or 3-state outputs connected at V_{DD} of 5 V.
- Input terminals protected by standard "B" series ESD protection network.
- Preserves final logic state.
- Output after switching is closer to V_{DD} or V_{SS} rail than with a resistor.
- Requires only one solder connection.
- Open circuited terminator not used will not affect performance.
- Can be connected to any CMOS I/O line.
- Draws current only when logic state is changing.
- Can be preset.



■ CD40117B is a dual 4-bit terminator that can be programmed by means of STROBE and DATA control bits to function as pull-up or pull-down resistors. The CD40117B can also be programmed to function as latches to terminate any open or unused CMOS logic when used with 3-state logic or during a power-down condition. Considerable savings in power and board space can be realized when this device is used to replace pull-up or pull-down resistors. When the STROBE is in the logic "1" state, the terminator functions as a pull-up resistor if the DATA input is a logic "1" or as a pull-down resistor if the DATA input is a logic "0".

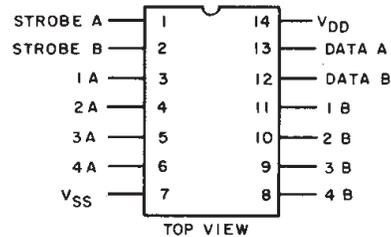
When the STROBE is in the logic "0" state, the terminator performs the latch function, i.e., it follows the changing states of the bus. If the bus goes into the high-Z state or into a power-down condition, the latched terminator retains the data ("1" or "0") that the bus carried before it switched to the high-Z or power-down state. If and when the bus changes from the high-Z state to the state opposite to that which the latch is storing, the bus will override the latch and the terminator will reflect the state on the bus. The small geometries chosen for the inverters in the latch allow this override mode. When checking the data bus whose last state is being preserved by the terminator, a resistor should be used in series with the probe whose input capacitance could trip the small latches. The resistance should be in excess of the output impedance of the latch, i.e., R should be > 30 KΩ at V_{DD} = 10 V.

The STROBE and DATA inputs in each section can be paralleled allowing this device to be used as an 8-bit bus terminator.

The CD40117B types are supplied in 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:

- Error state identification.
- Replaces pull-up or pull-down resistors
- Avoids floating inputs in modular systems
- Sharpens transistors (hysteresis)
- Anti-bounce circuit



TERMINAL DIAGRAM

TRUTH TABLE

STROBE	DATA	1A(B)	2A(B)	3A(B)	4A(B)
1	0	0 Δ	0 Δ	0 Δ	0 Δ
1	1	1 $+$	1 $+$	1 $+$	1 $+$
0	X	*	*	*	*

1 = High, 0 = Low, X = Don't Care

Δ Equivalent to pull-down resistor.

$+$ Equivalent to pull-up resistor.

*Equivalent to a latch.

CD40117B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5V to +20V
Voltages referenced to V_{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10mA$
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -55^\circ C$ to $+100^\circ C$	500mW
For $T_A = +100^\circ C$ to $+125^\circ C$	Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	$-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE (T_{stg})	$-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79mm$) from case for 10s max	$+265^\circ C$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	TYP.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range)	—	3	18	V

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

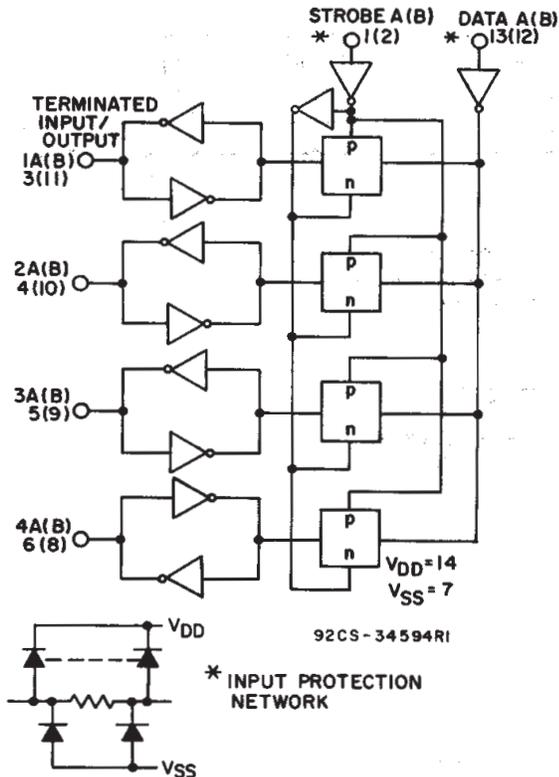
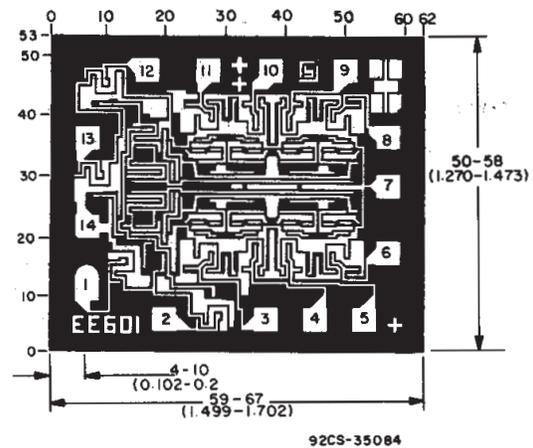


Fig. 1 - Logic diagram (1/2 of CD40117B)



Dimensions and pad layout for CD40117B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CD40117B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current Max. I _{DD}	—	0, 5	5	0.25	0.25	7.5	7.5	—	—	0.25	μA
	—	0, 10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0, 15	15	1	1	30	30	—	0.01	1	
	—	0, 20	20	5	5	150	150	—	0.02	5	
Output Low Sink Current Min. I _{OL}	0.4	0, 5	5	—	—	—	—	—	25	—	μA
	0.5	0, 10	10	—	—	—	—	—	60	—	
	1.5	0, 15	15	—	—	—	—	—	250	—	
Output High (Source) Current Min. I _{OH}	4.6	0, 5	5	—	—	—	—	—	-25	—	μA
	2.5	0, 5	5	—	—	—	—	—	—	—	
	9.5	0, 10	10	—	—	—	—	—	-60	—	
	13.5	0, 15	15	—	—	—	—	—	-250	—	
Output Voltage: Low-Level Max. V _{OL}	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min. V _{OH}	—	0, 5	5	4.95				4.95	5	—	V
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage Max. V _{IL}	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage Min. V _{IH}	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current Max. I _{IN}	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V _{DD} (V)	LIMITS All Packages			UNITS
			MIN.	TYP.	MAX.	
Propagation Delay Time Strobe, Data to Outputs	t _{PHL}	5	—	1.7	—	μs
		10	—	850	—	ns
		15	—	575	—	ns
	t _{PLH}	5	—	1.5	—	μs
		10	—	625	—	ns
		15	—	500	—	ns
Transition Time	t _{THL} , t _{TLH}	5	—	3.3	—	μs
		10	—	1.6	—	μs
		15	—	1.1	—	μs
Minimum Strobe Pulse Width	t _w	5	—	1.5	—	μs
		10	—	600	—	ns
		15	—	475	—	ns
Minimum Data Pulse Width	t _{WH} , t _{WL}	5	—	1.6	—	μs
		10	—	700	—	ns
		15	—	500	—	ns
Minimum Terminator Input/Output Pulse Width	t _w	5	—	10	—	ns
Minimum Data Setup Time Data to Strobe	t _{SU}	5	—	0	—	ns
		10	—	0	—	ns
		15	—	0	—	ns
Input Capacitance	C _{IN}	Any Input	—	5	—	pF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40117BE	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD40117BE	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

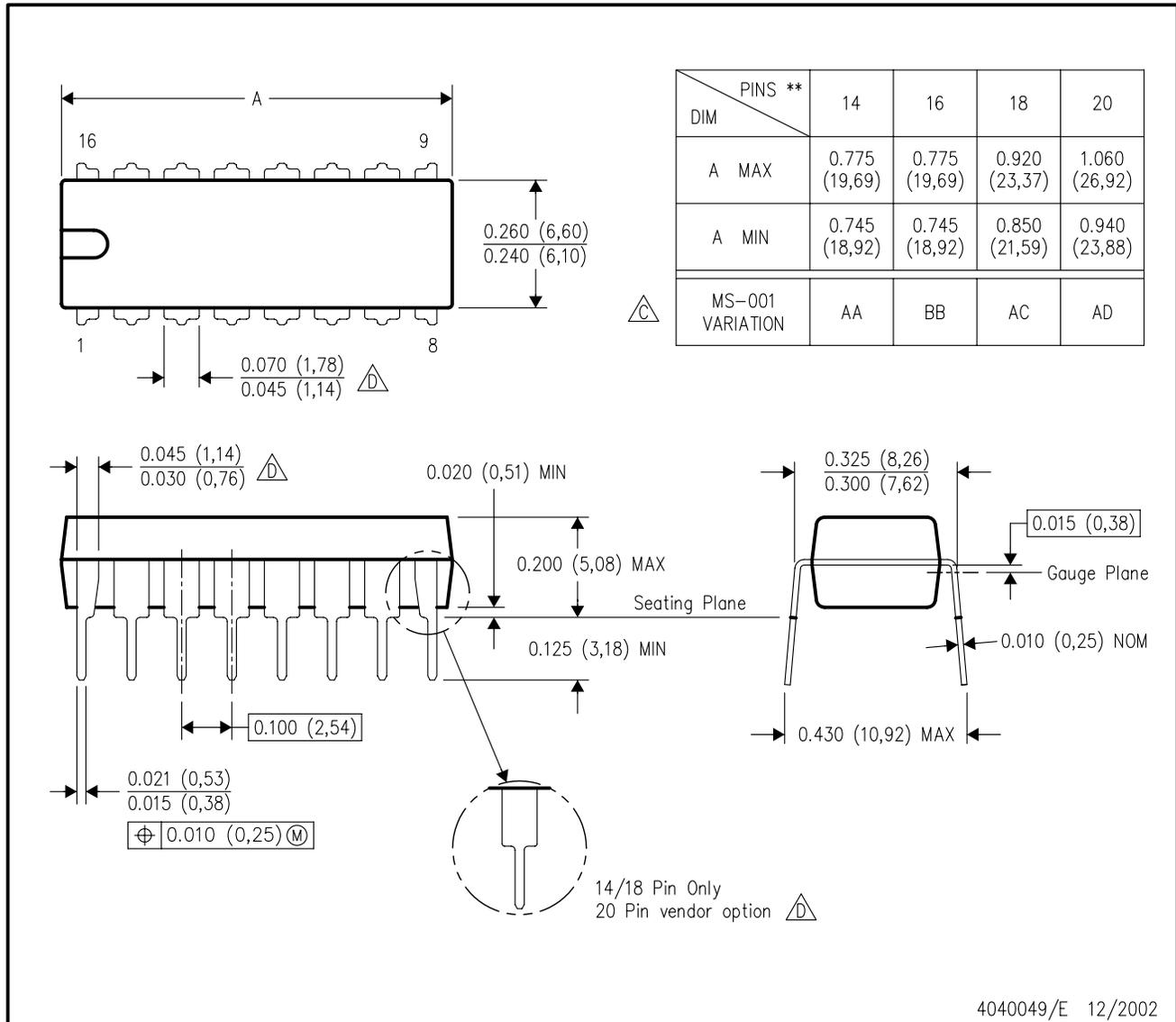
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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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