ASM3P2863A

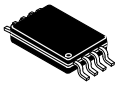
Product Preview

Low Power Peak EMI Reducing Solution

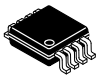
ON Semiconductor®

http://onsemi.com

TSOT−6
O SUFFIX
CASE 419AF



TSSOP−8
T SUFFIX
CASE 948AL



SOIC−8
S SUFFIX
CASE 751BD

Description

The ASM3P2863A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The ASM3P2863A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The ASM3P2863A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding that are traditionally required to pass EMI regulations.

The ASM3P2863A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

The ASM3P2863A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation.'

Applications

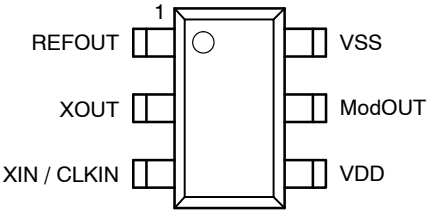
The ASM3P2863A is targeted towards all portable devices with very low power requirements like MP3 players, Notebooks and Digital still cameras.

Features

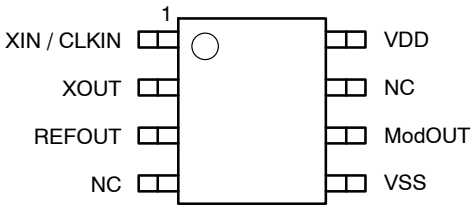
- Generates an EMI Optimized Clock Signal at the Output
- Integrated Loop Filter Components
- Operates with a 3.3 V / 2.5 V Supply
- Operating Current less than 4 mA
- Low Power CMOS Design
- Input Frequency: 12 MHz
- Generates a 1X Low EMI Spread Spectrum Clock of the Input Frequency
- Frequency Deviation: ±0.4% (Typ) @ 12 MHz Input Frequency
- Available in 6−pin TSOT−23, 8−pin SOIC and 8−pin TSSOP Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

PIN CONFIGURATIONS



6−Pin TSOT−23 Package
(Top View)



8−Pin SOIC and TSSOP Packages
(Top View)

KEY SPECIFICATIONS

Description	Specification
Supply Voltages	V_{DD} = 2.5 V / 3.3 V
Cycle−to−Cycle Jitter	200 pS (Typ)
Output Duty Cycle	45/55% (worst case)
Modulation Rate Equation	F_{IN}/256
Frequency Deviation	±0.4% (Typ) @ 12 MHz

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

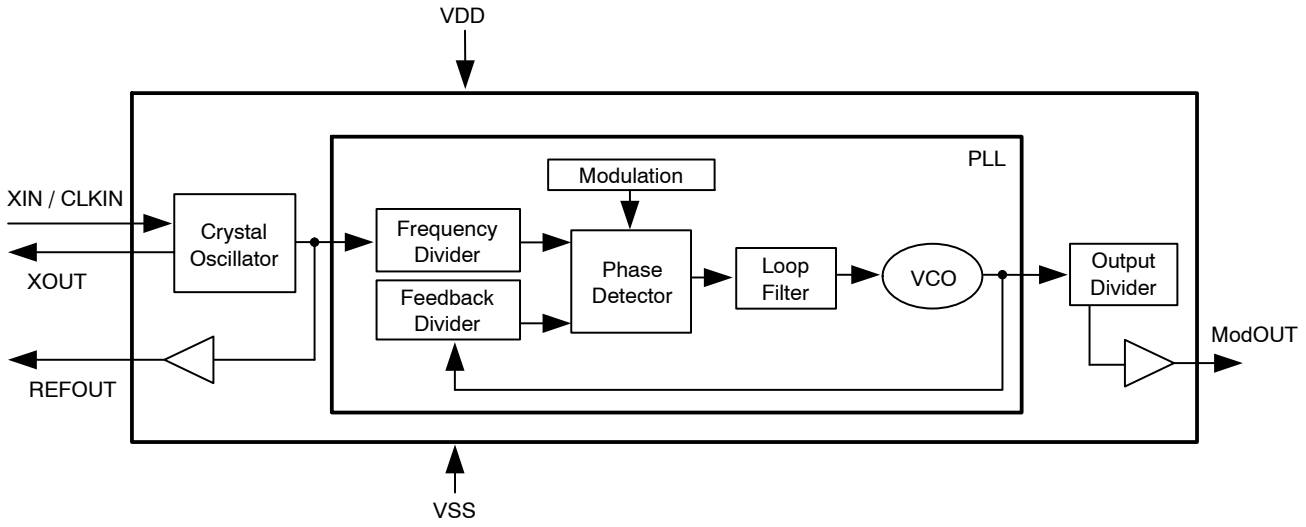


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION (6−Pin TSOT−23 Package)

Pin#	Pin Name	Type	Description
1	REFOUT	O	Buffered output of the input frequency.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	XIN / CLKIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
4	VDD	P	Power supply for the entire chip.
5	ModOUT	O	Spread spectrum clock output.
6	VSS	P	Ground connection.

Table 2. PIN DESCRIPTION (8−Pin SOIC and TSSOP Packages)

Pin#	Pin Name	Type	Description
1	XIN / CLKIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	REFOUT	O	Buffered output of the input frequency.
4	NC	−	No connect.
5	VSS	P	Ground connection.
6	ModOUT	O	Spread spectrum clock output.
7	NC	−	No connect.
8	VDD	P	Power supply for the entire chip.

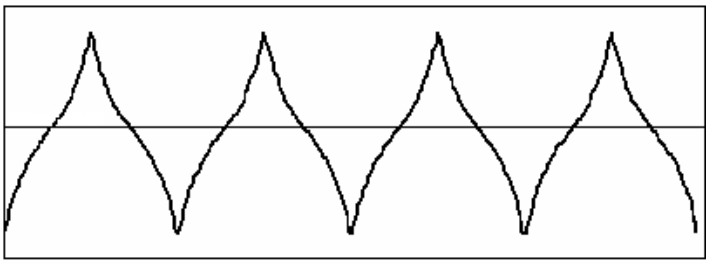


Figure 2. Modulation Profile

Table 3. SPECIFICATIONS

Description	Specification
Input Frequency	12 MHz
Modulation Equation	$F_{IN}/256$
Frequency Deviation	±0.4% (Typ) @ 12 MHz

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated.)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS−0.3	–	0.8	V
V_{IH}	Input high voltage	2.0	–	VDD+0.3	V
I_{IL}	Input low current	–	–	−35	μA
I_{IH}	Input high current	–	–	35	μA
I_{XOL}	XOUT output low current (@ 0.5 V, VDD = 2.5 V)	–	3	–	mA
I_{XOH}	XOUT output high current (@ 1.8 V, VDD = 2.5 V)	–	3	–	mA
V_{OL}	Output low voltage (VDD = 2.5 V, I_{OL} = 8 mA)	–	–	0.6	V
V_{OH}	Output high voltage (VDD = 2.5 V, I_{OH} = 8 mA)	1.8	–	–	V
I_{DD}	Static supply current (Note 1)	–	0.8	–	mA
I_{CC}	Dynamic supply current (2.5 V, 12 MHz and no load)	–	3	–	mA
VDD	Operating voltage	2.375	2.5	2.625	V
t_{ON}	Power−up time (first locked cycle after power−up)	–	–	5	mS
Z_{OUT}	Output impedance	–	50	–	Ω

1. XIN / CLKIN pin is pulled low.

Table 6. AC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input frequency	–	12	–	MHz
ModOUT	Output frequency	–	12	–	MHz
f_d	Frequency Deviation	–	±0.4	–	%
t_{LH} (Note 2)	Output rise time (measured from 0.7 V to 1.7 V)	0.5	1.5	1.7	nS
t_{HL} (Note 2)	Output fall time (measured from 1.7 V to 0.7 V)	0.5	1.0	1.2	nS
t_{JC}	Jitter (Cycle−to−Cycle)	–	200	300	pS
t_D	Output duty cycle	45	50	55	%

2. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

Table 7. DC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated.)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS−0.3	–	0.8	V
V_{IH}	Input high voltage	2.0	–	VDD+0.3	V
I_{IL}	Input low current	–	–	−35	μA
I_{IH}	Input high current	–	–	35	μA
I_{XOL}	XOUT output low current (@ 0.4 V, V_{DD} = 3.3 V)	–	3	–	mA
I_{XOH}	XOUT output high current (@ 2.5 V, V_{DD} = 3.3 V)	–	3	–	mA
V_{OL}	Output low voltage (VDD = 3.3 V, I_{OL} = 8 mA)	–	–	0.4	V
V_{OH}	Output high voltage (VDD = 3.3 V, I_{OH} = 8 mA)	2.5	–	–	V
I_{DD}	Static supply current (Note 3)	–	1	–	mA
I_{CC}	Dynamic supply current (3.3 V, 12 MHz and no load)	–	3.5	–	mA
VDD	Operating Voltage	3.0	3.3	3.6	V
t_{ON}	Power−up time (first locked cycle after power−up)	–	–	5	mS
Z_{OUT}	Output impedance	–	45	–	Ω

3. XIN / CLKIN pin is pulled low.

Table 8. AC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

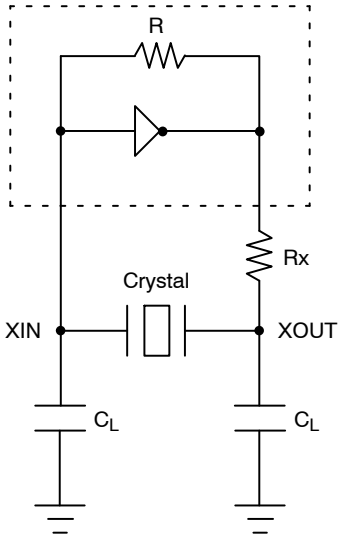
Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input frequency	–	12	–	MHz
ModOUT	Output frequency	–	12	–	MHz
f_d	Frequency Deviation	–	±0.4	–	%
t_{LH} (Note 4)	Output rise time (measured from 0.8 V to 2.0 V)	0.5	1.4	1.6	nS
t_{HL} (Note 4)	Output fall time (measured at 2.0 V to 0.8 V)	0.4	1.0	1.2	nS
t_{JC}	Jitter (Cycle−to−Cycle)	–	200	300	pS
t_D	Output duty cycle	45	50	55	%

4. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

Table 9. CRYSTAL SPECIFICATIONS

Fundamental AT Cut Parallel Resonant Crystal	
Nominal frequency	12 MHz
Frequency tolerance	±50 ppm or better at 25°C
Operating temperature range	−25°C to +85°C
Storage temperature	−40°C to +85°C
Load capacitance (C_P)	18 pF
Shunt capacitance	7 pF maximum
ESR	25 Ω

NOTE: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

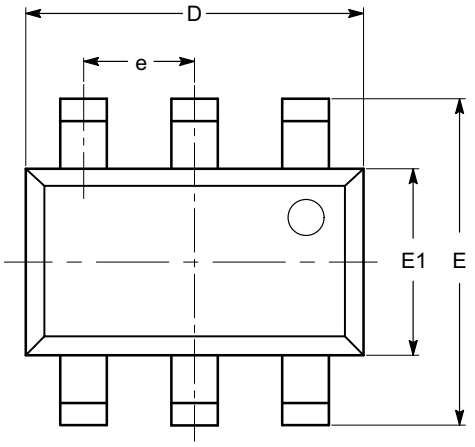


$C_L = 2^*(C_P - C_S)$,
Where C_P = Load capacitance of crystal from crystal vendor datasheet.
C_S = Stray capacitance due to C_{IN}, PCB, Trace, etc.

Figure 3. Typical Crystal Interface Circuit

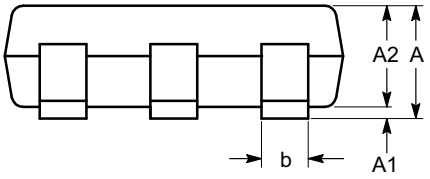
PACKAGE DIMENSIONS

TSOT−23, 6 LEAD
CASE 419AF−01
ISSUE O

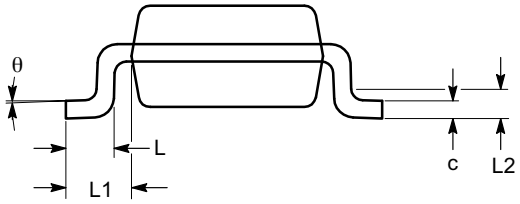


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 TYP	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	
θ	0°		8°



SIDE VIEW

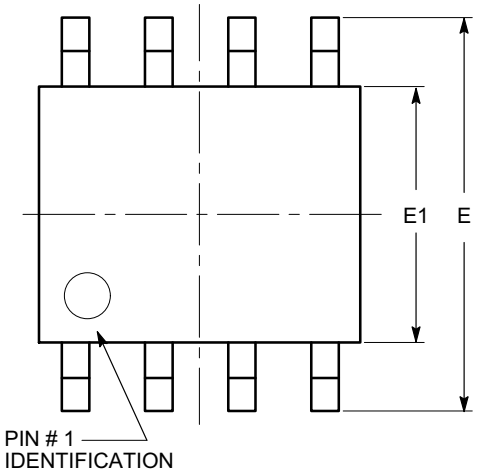


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

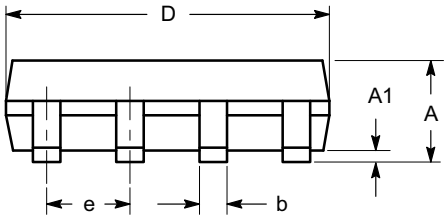
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

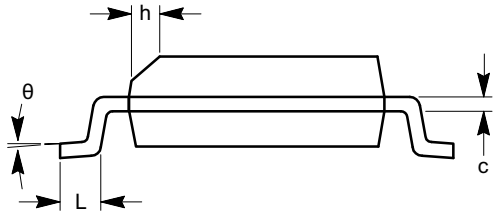


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

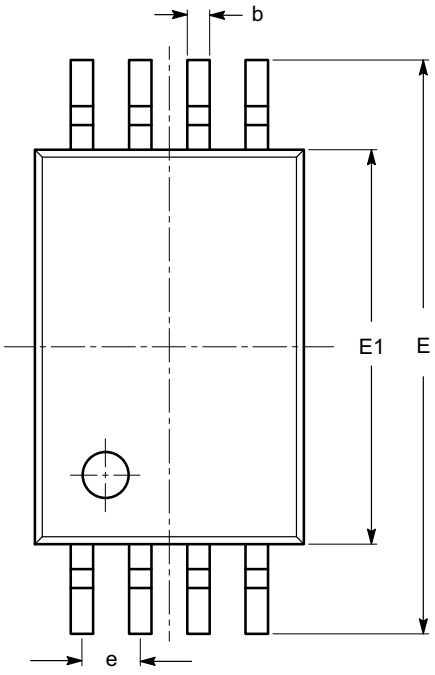


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

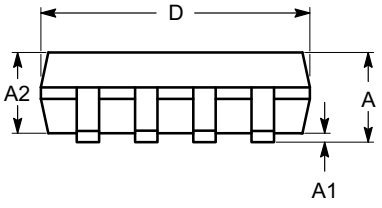
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O



TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



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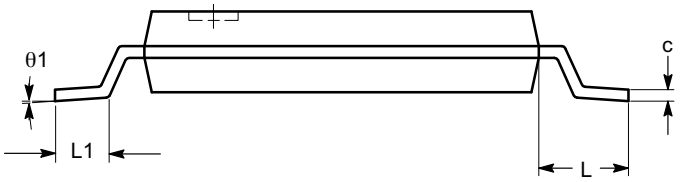

END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Table 10. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
ASM3P2863AF−06OR	V4LL	6−Pin TSOT−23, TAPE & REEL, Pb Free	Commercial
ASM3P2863AF−08TT	3P2863AF	8−Pin TSSOP, TUBE, Pb Free	Commercial
ASM3P2863AF−08TR	3P2863AF	8−Pin TSSOP, TAPE & REEL, Pb Free	Commercial
ASM3P2863AF−08ST	3P2863AF	8−Pin SOIC, TUBE, Pb Free	Commercial
ASM3P2863AF−08SR	3P2863AF	8−Pin SOIC, TAPE & REEL, Pb Free	Commercial
ASM3P2863AG−06OR	V3LL	6−Pin TSOT−23, TAPE & REEL, Green	Commercial
ASM3P2863AG−08TT	3P2863AG	8−Pin TSSOP, TUBE, Green	Commercial
ASM3P2863AG−08TR	3P2863AG	8−Pin TSSOP, TAPE & REEL, Green	Commercial
ASM3P2863AG−08ST	3P2863AG	8−Pin SOIC, TUBE, Green	Commercial
ASM3P2863AG−08SR	3P2863AG	8−Pin SOIC, TAPE & REEL, Green	Commercial

PUBLICATION ORDERING INFORMATION

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