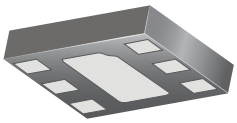
Low Voltage Voice Coil Motor Driver

Features and Benefits

- Fixed I²C logic thresholds
- 8-bit D-to-A converter
- 500 µA resolution
- Low voltage I²C serial interface
- Low current-draw sleep mode
- 2.4 to 5.5 V operation
- 2 mm × 1.5 mm, 0.38 mm nominal overall height DFN
- 1.1 mm × 0.7 mm, 0.5 mm maximum overall height WLCSP

Packages:



1.5 mm × 2 mm DFN
(EW package)

1.1 mm × 0.7 mm WLCSP
(CG package)

Not to scale

Description

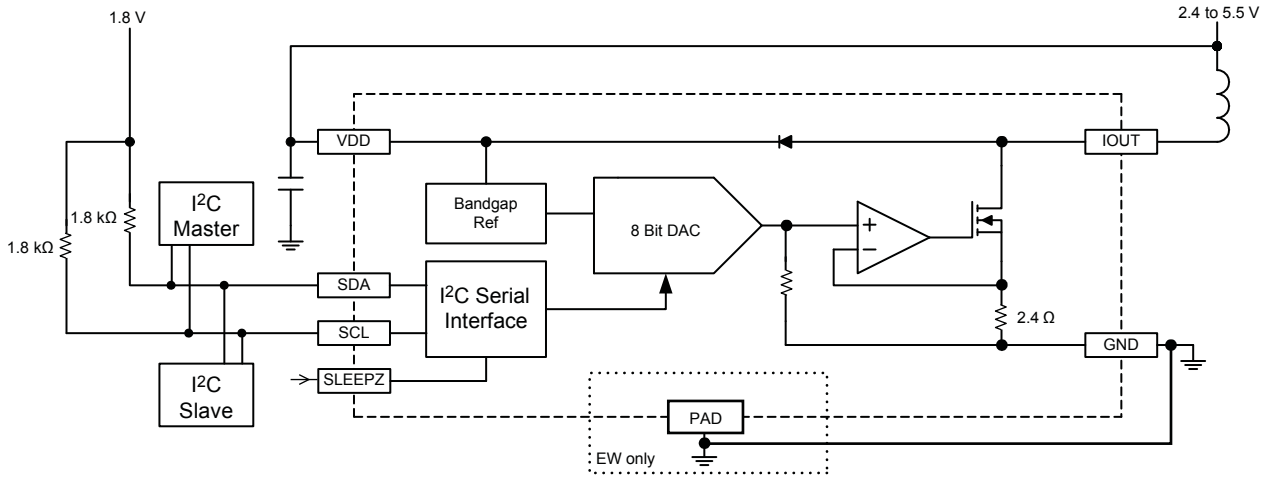
The A3904 is a voice coil motor (VCM) driver, with an I²C-compatible serial interface. Designed for camera autofocus and zoom applications, this high accuracy digital IC is provided in small packages ideal for portable devices. Its operating voltage range is 2.4 to 5.5 V, and its maximum output current is 127 mA.

Output current is programmed via the I²C interface, in 500 uA increments, with clock rates up to 400 kHz. I²C inputs set the internal D-to-A converter output voltage that is the reference for linear current control via a MOSFET output sink transistor. To conserve battery power, a logic low signal on the SLEEPZ input disables the output MOSFET and reduces the supply current to <0.5 µA.

A3904 internal protection features include thermal shutdown and undervoltage lockout. Logic input levels are independent of the supply voltage. The operating temperature range is –40°C to 85°C.

The A3904 is available at two packaging levels: bumped wafer level chip scale package (WLCSP) (suffix CG); and complete thin profile (0.38 mm nominal overall height) DFN package, with NiAuPd leadframe plating and an exposed tab for enhanced thermal dissipation (suffix EW).

Functional Block Diagram



Selection Guide

Part Number	Packing	Package	Pb-Free
A3904ECGTR	4000 pieces per reel	Bumped wafer-level chip-scale package (WLCSP)	Pb-free chip with high-temperature solder balls (RoHS compliant)
A3904EEWTR-P	3000 pieces per reel	Leadless package (DFN)	Yes; NiAuPd leadframe plating

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{DD}		6	V
Logic Input Voltage Range	V_{IN}		–0.3 to V_{DD}+0.3	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

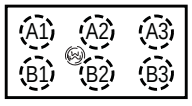
Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	EW package, 4-layer PCB based on JEDEC standard	64	ºC/W

*For additional information, refer to the Allegro website.

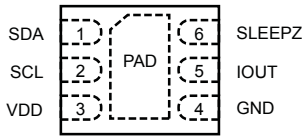
Pin-out Diagrams

CG Package



Orientation mark on bump side

EW Package



Terminal List

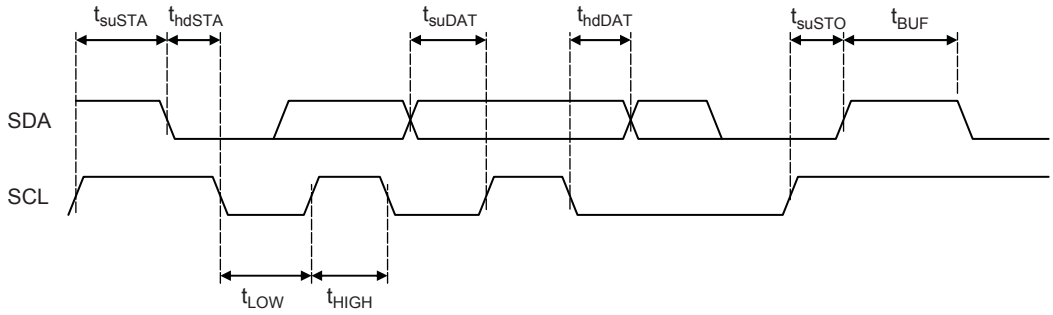
Number		Name	Description
EW	CG		
1	A1	SDA	I^2C data input/output
2	A2	SCL	I^2C clock
3	A3	VDD	Power supply
4	B3	GND	Ground
5	B2	IOUT	Sink drive output
6	B1	SLEEPZ	Standby mode control
PAD	–	–	Exposed thermal pad (tie to GND)

ELECTRICAL CHARACTERISTICS Valid at T_A= 25°C, V_{DD} = 2.4 to 5.5 V, unless otherwise noted

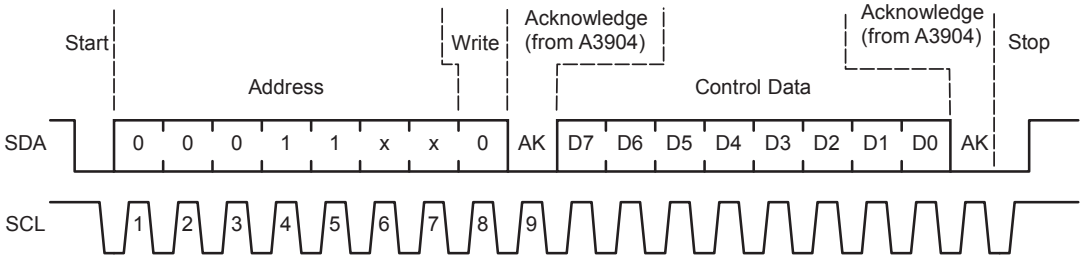
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
General						
Supply Current	I_{DD}		–	0.5	2	mA
		Sleep mode (SLEEPZ = Low)	–	<100	500	nA
UVLO Enable Threshold	$V_{UV(th)}$	V_{DD} rising	–	2.1	2.395	V
UVLO Hysteresis	$V_{UV(hys)}$		100	–	–	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$.T_{JTSD(hys)}$	$T_{JTSD(hys)} = T_{JTSD} – T_{J(recover)}$	–	15	–	°C
Power-Up Delay	$t_{d(on)}$		–	10	–	µs
D-to-A Converter						
Resolution	Res	Target = 500 µA / LSB	–	8	–	bit
LSB Relative Accuracy	INL	Code = 16 to 255, Endpoint method	–	±4	–	LSB
LSB Differential Nonlinearity	DNL	Guaranteed monotonic	–	–	±1	LSB
Maximum Output Current	I_{max}	Code = 255	–	127.5	–	mA
Gain Error	err_A	T_J = 25°C, Code 16 to 255, V_{DD} = 2.6 to 3.0 V	–10	<3	10	%FS
Gain Error Drift*	Δerr_A	T_J = –40°C to 125°C	–	0.2	–	LSB/°C
Offset Error	I_{errOS}	Code = 1	0	1	5	mA
		Code = 16	0.5	–	–	mA
Output						
Output Voltage Range	V_{OUT}		0.500	–	V_{DD}–0.1	V
Output On Resistance	$R_{DS(on)}$	$R_{SENSE} + R_{SINK}$, I_{OUT} = 127.5 mA	–	3	–	Ω
I²C Interface						
Bus Free Time Between Stop and Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	t_{hdSTA}		0.6	–	–	µs
Setup Time for Repeated Start Condition	t_{suSTA}		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	t_{suDAT}		100	–	–	ns
Data Hold Time	t_{hdDAT}		0		900	ns
Setup Time for Stop Condition	t_{suSTO}		0.6	–	–	µs
Logic Input Low Level (SDA, SCL pins)	V_{IL}		–	–	0.84	V
Logic Input High Level (SDA, SCL pins)	V_{IH}		1.26	–	–	V
Input Hysteresis (SDA, SCL pins)	V_{hys}		–	100	–	mV
SLEEPZ Input Low Level	V_{inSLP}		–	–	0.7	V
SLEEPZ Input High Level	V_{inSLP}		1.5	–	–	V
Logic Input Current	I_{IN}	V_{IN} = 0 V to V_{DD}	–1	0	1	µA
Output Voltage (SDA pin)	V_{OL}	I_{LOAD} = 1.5 mA	–	–	0.36	V
Clock Frequency (SCL pin)	f_{CLK}		–	–	400	kHz
Output Fall Time (SDA pin)	t_{fO}	V_{IH} to V_{IL}	–	–	250	ns

*Guaranteed by design and characterization, not production tested

I²C Interface Timing Diagram



Write Register Bit Definition and Timing Diagram



I²C Control Register Bit Definition

Bit	Name	Function
0	D0	DAC LSB
1	D1	
2	D2	
3	D3	
4	D4	
5	D5	
6	D6	
7	D7	DAC MSB

A3904 Slave Address Bit Definition

Bit								Operation
0	1	2	3	4	5	6	7	
0	0	0	1	1	x	X	1	Read
							0	Write

Functional Description

The A3904 output current is controlled by programming the D-to-A converter value via the I²C serial port. The target output current can be calculated by:

$$I_{OUT} = \text{DAC} \times 500\ \mu\text{A}\ ,$$

where DAC = 1 to 255. Code = 0 is a disable state for the output sink drive. The DAC will be set to code = 0 upon power-up or a fault condition on V_{DD}.

SLEEPZ A logic low input disables all of the internal circuitry and prevents the IC from draining battery power.

Output Range The voltage on the IOUT pin should be greater than 500 mV to guarantee the accuracy and linearity of the programmed current. The output voltage is a function of the battery voltage, motor resistance, and the programmed load current.

Clamp Diode When the output is turned off, the load inductance causes the output voltage to rise. A clamp diode, from IOUT to VDD, is integrated in the IC to ensure that the output voltage remains at a safe level.

I²C Interface This is a serial interface that uses two bus lines, SCL and SDA, to access the internal Control registers. Data is exchanged between a microcontroller (master) and the A3904 (slave). The clock input to SCL is generated by the master, while the SDA line functions as either an input or an open drain output, depending on the direction of the data. The I²C input thresholds do not depend on the V_{DD} voltage of the A3904. The levels are fixed at approximately 1 V. The fixed levels allow the SDA and SCL lines to be pulled-up to a different logic level than the V_{DD} supply of the 3904.

Timing Considerations The control sequence of the communication through the I²C interface is composed of several steps in the following sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.
2. Address Cycle. 7 bits of address, plus 1 bit to indicate write (0) or read (1), and an acknowledge bit. The address setting is 0x18, 0x1A, 0x1C or 0x1E.
3. Data Cycles. Write 8 bits of data that address the internal Control register, followed by an acknowledge bit.
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low. It is possible for the Start or Stop condition to occur at any time during a data transfer. The A3904 always responds by resetting the data transfer sequence.

The Read/Write bit is set low to indicate a write cycle. Multiple writes are allowed before issuing a Stop condition. There are no readback functions incorporated into the A3904.

The master monitors for an acknowledge pulse to determine if the slave device is responding to the address byte sent to the A3904. When the A3904 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A3904 pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the master device must release the SDA line before the ninth clock cycle, in order to allow this handshaking to occur.

Application Information

Headroom The current may not reach the programmed level if there is not adequate headroom in the output circuit. The IC output voltage must be over 500 mV to guarantee normal linear operation. V_{DD}, I_{LOAD}, and R_{LOAD} can be adjusted to ensure that the device operates in the linear range.

If the equation shown below is not satisfied, the load current will be limited by the series impedance, and may not reach the programmed level

$$V_{DD}(\text{min}) - R_{LOAD}(\text{max}) \times I_{OUT}(\text{max}) \geq 500\ \text{mV} \quad .$$

I_{OUT} Errors

Relative accuracy (INL) This error is calculated by measuring the worse case deviation from a straight line, defined from end points. The straight line end points are defined by the actual measured values at Code = 16 and Code = 255. See figure 1.

Differential nonlinearity (DNL) A measure of the monotonicity of the D-to-A converter. The slope of the line must always be positive for each incremental step, according to the following formula:

$$\text{DNL} = (I_{OUT(n+1)} - I_{OUT(n)}) / \text{LSB} - 1 \ \text{(LSB)} \quad .$$

where *n* is in the range 16 to 255.

Offset error The measured output current at input Code = 16, compared to the ideal value according to the transfer function (8 mA).

Gain Error The difference in the slopes of the ideal transfer function and the actual transfer function. The gain error is calculated by subtracting out the offset error, at Code = 16, from the actual transfer function. This calculated value is compared to the ideal transfer function and reported as a percentage of the ideal full scale value (127.5 mA). See figure 2.

Gain Error Drift The change in slope of the transfer function due to temperature, expressed as LSB/°C.

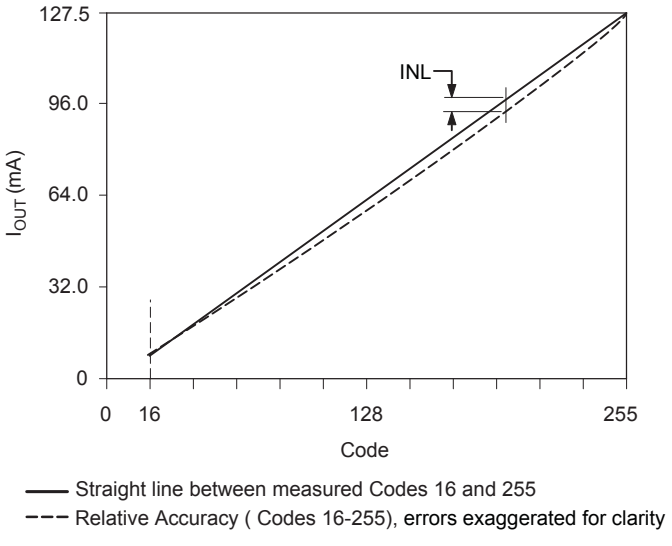


Figure 1. Relative accuracy error

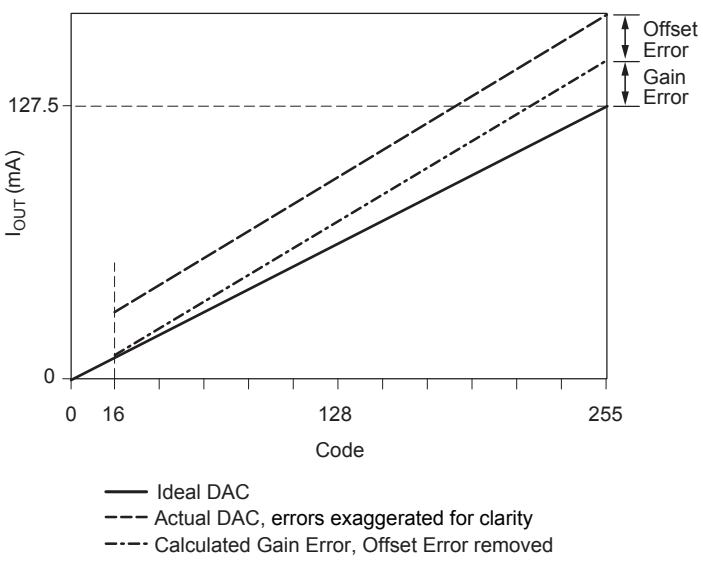
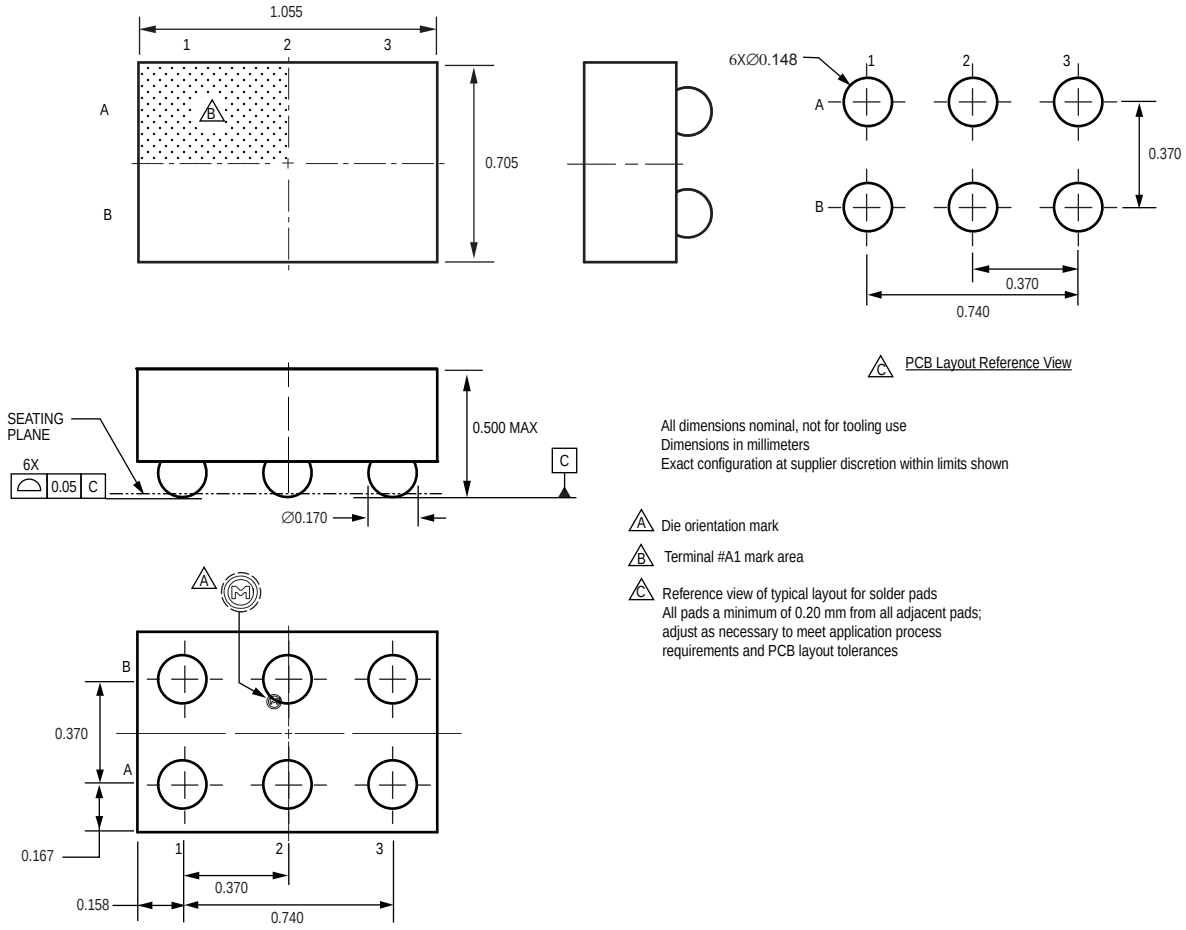


Figure 2. Gain error

CG Package, 6-Bump WLCSP



PCB Layout Reference View

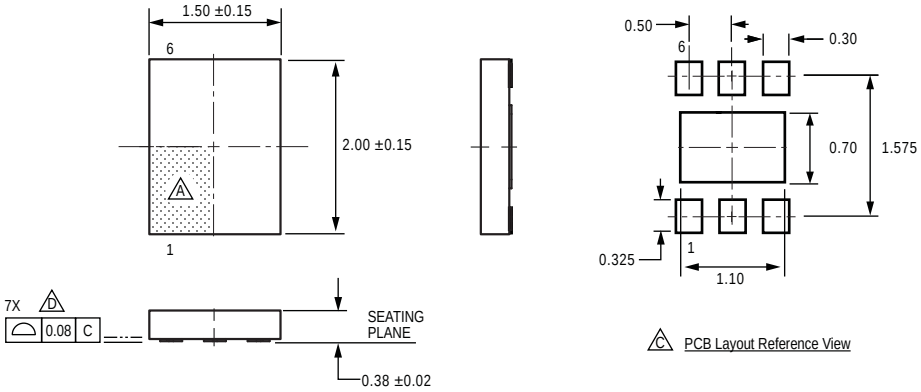
All dimensions nominal, not for tooling use
Dimensions in millimeters
Exact configuration at supplier discretion within limits shown

A Die orientation mark

B Terminal #A1 mark area

C Reference view of typical layout for solder pads
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

EW Package, 6-Contact DFN



For Reference Only
(similar to JEDEC Type 1, MO-229"X2"BCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals