FAIRCHILD SEMICONDUCTOR®

May 2007

74ACTQ74
Quiet Series Dual D-Type Positive Edge-Triggered Flip-Flop

Features

- I_{CC} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- 4kV minimum ESD immunity
- TTL-compatible inputs

General Description

The 74ACTQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

The ACTQ74 utilizes Fairchild Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Asynchronous Inputs:

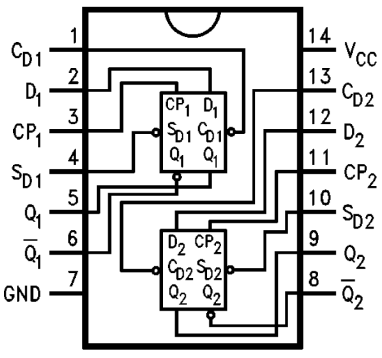
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Information

Order Number	Package Number	Package Description
74ACTQ74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACTQ74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

Connection Diagram



Pin Descriptions

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

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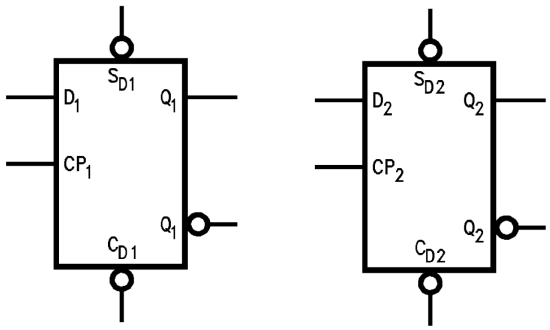
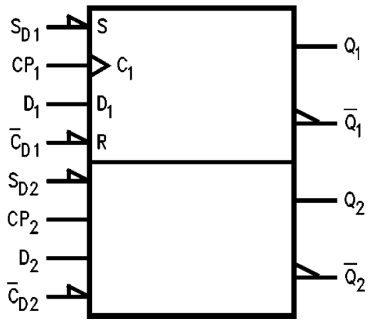
Logic Symbols



IEEE/IEC



Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level

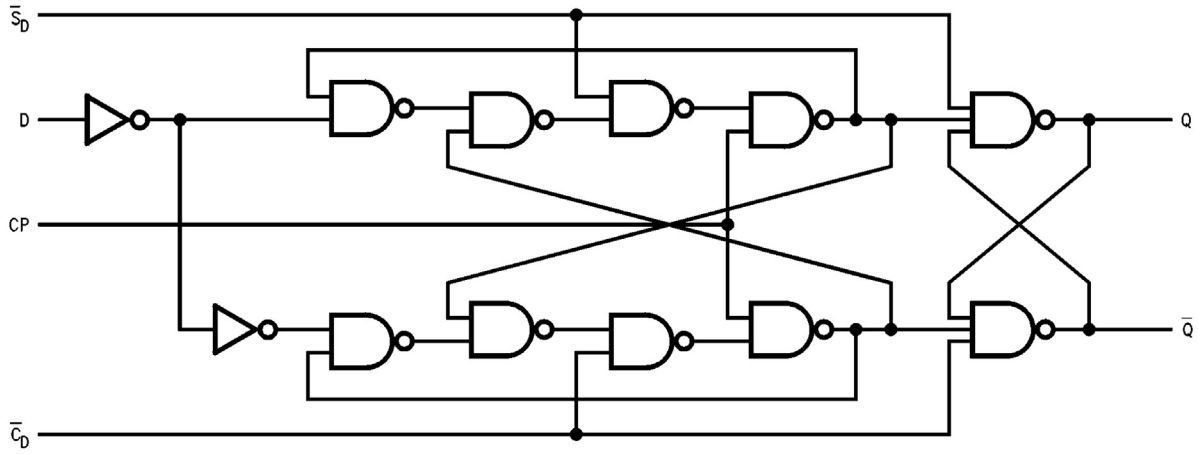
L = LOW Voltage Level

X = Immaterial

⌐ = LOW-to-HIGH Clock Transition

$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = –0.5V$	–20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
	DC Latch-Up Source or Sink Current	±300mA
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1V	4.5	1.5	2.0	2.0	V
			5.5	1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1V	4.5	1.5	0.8	0.8	V
			5.5	1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	I_{OUT} = –50 µA	4.5	4.49	4.4	4.4	V
			5.5	5.49	5.4	5.4	
		V_{IN} = V_{IL} or V_{IH}: I_{OH} = –24mA	4.5		3.86	3.76	
		I_{OH} = –24mA(1)	5.5		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	I_{OUT} = 50µA	4.5	0.001	0.1	0.1	V
			5.5	0.001	0.1	0.1	
		V_{IN} = V_{IL} or V_{IH}: I_{OL} = 24mA	4.5		0.36	0.44	
		I_{OL} = 24mA(1)	5.5		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	V_I = V_{CC}, GND	5.5		±0.1	±1.0	µA
I_{OZ}	Maximum 3-STATE Leakage Current	V_I = V_{IL}, V_{IH}; V_O = V_{CC}, GND	5.5		±0.5	±5.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1V	5.5	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current(1)	V_{OLD} = 1.65V Max.	5.5			75	mA
I_{OHD}		V_{OHD} = 3.85V Min.	5.5			–75	mA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5		2.0	20.0	µA
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	Figures 1 & 2(3)	5.0	1.1	1.5		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	Figures 1 & 2(3)	5.0	–0.6	–1.2		V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	(4)	5.0	1.9	2.2		V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	(4)	5.0	1.2	0.8		V

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.
4. Max number of data inputs (n) switching. (n – 1) inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)[5]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	5.0	145	200		125		MHz
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	7.0	8.5	3.0	9.0	ns
t_{PLH}, t_{PHL}	Propagation Delay, CP_n to Q_n or $\overline{Q}_n$	5.0	3.0	6.5	8.0	3.0	8.6	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew[6]	5.0		0.5	1.0		1.0	ns

Notes:

5. Voltage range 5.0 is 5.0V ± 0.5V.
6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50pF	T_A = –40°C to +85°C, C_L = 50pF		Units
			Typ.	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, D_n to CP_n	5.0	1.0	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW, D_n to CP_n	5.0	–0.5	1.5	1.5	ns
t_W	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$, Pulse Width	5.0	3.0	4.0	4.0	ns
t_{REC}	Recovery Time, $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	–2.5	1.5	1.5	ns

Note:

7. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	60.0	pF

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

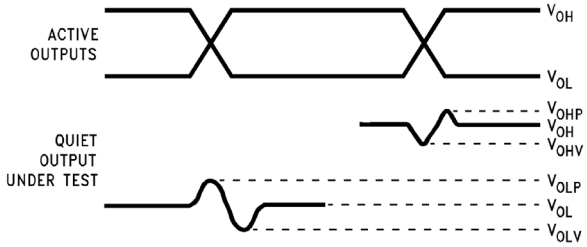
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.



Notes:

8. V_{OHV} and V_{OLP} are measured with respect to ground reference.
9. Input pulses have the following characteristics: f = 1MHz, t_r = 3ns, t_f = 3ns, skew < 150ps.

Figure 1. Quiet Output Noise Voltage Waveforms

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case transition for active and enable.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

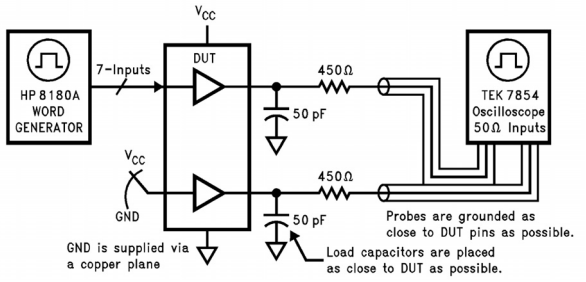


Figure 2. Simultaneous Switching Test Circuit

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

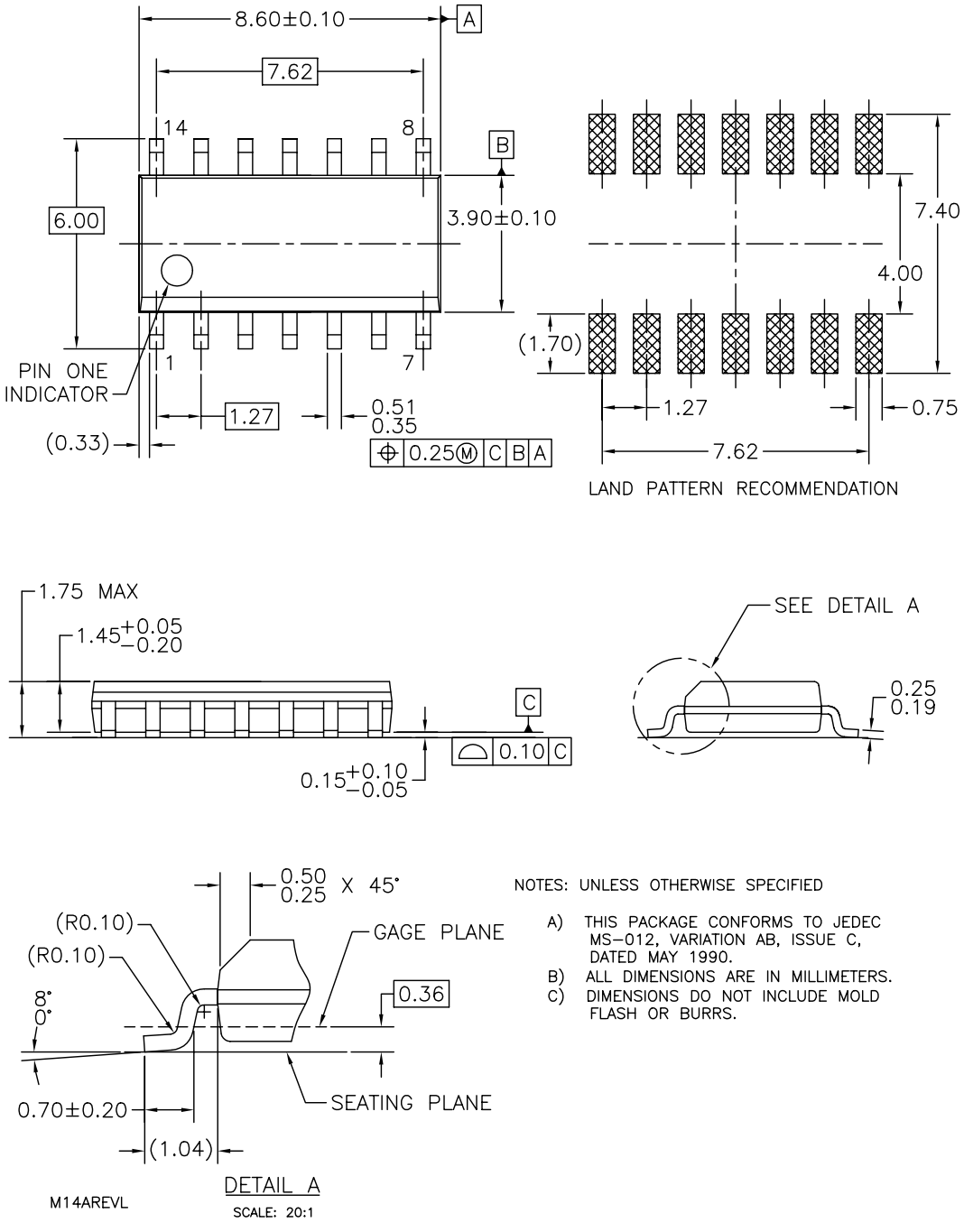
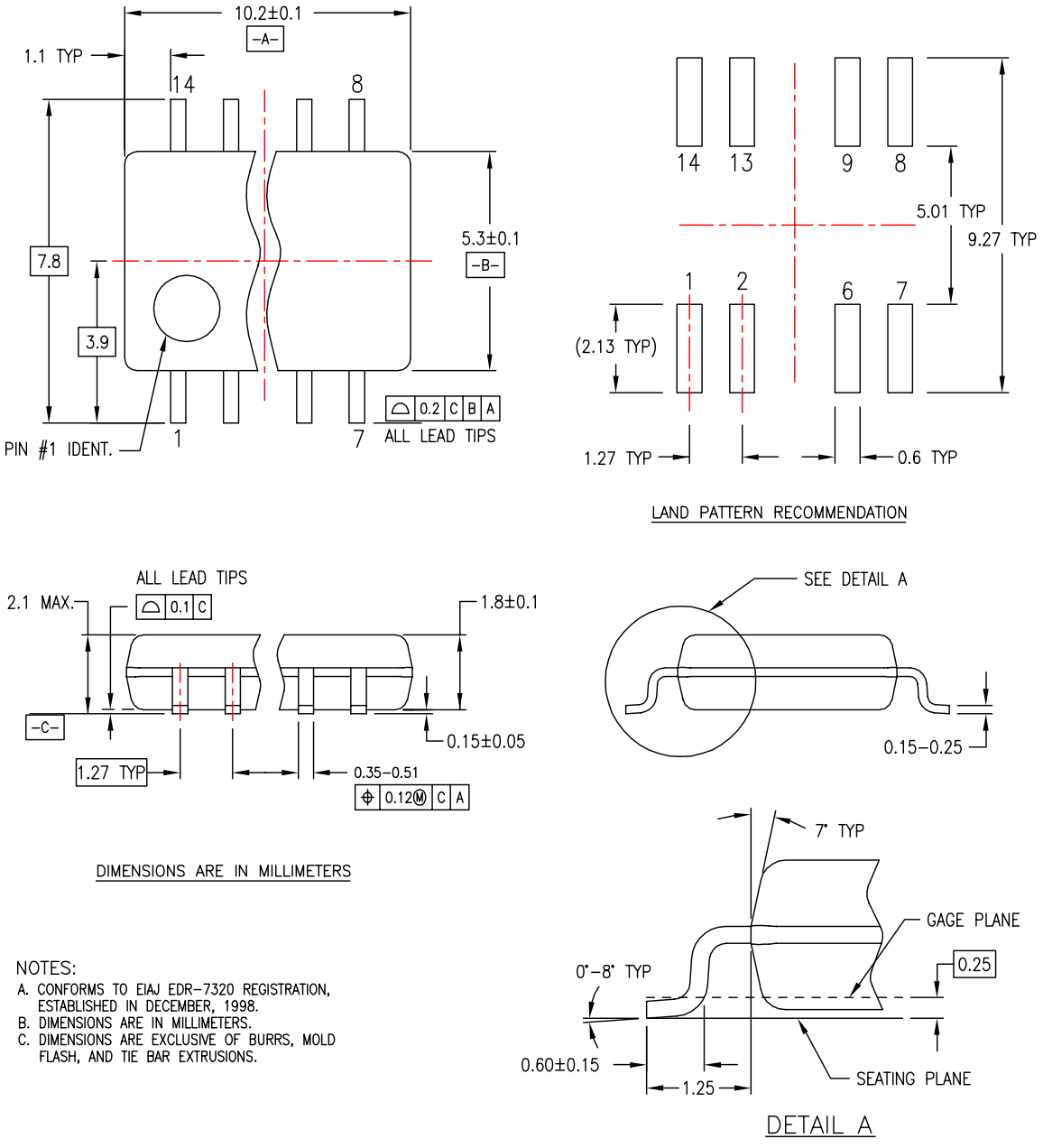


Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 4. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

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Rev. I26