FAIRCHILD SEMICONDUCTOR™

August 1999
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74ACT16543
16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The ACT16543 contains sixteen non-inverting transceivers containing two sets of D-type registers for temporary storage of data flowing in either direction. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

Features

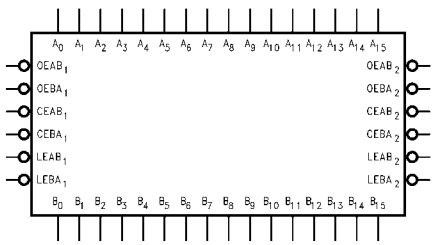
- Independent registers for A and B buses
- Separate controls for data flow in each direction
- Back-to-back registers for storage
  Multiplexed real-time and stored data transfers
- Separate control logic for each byte
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

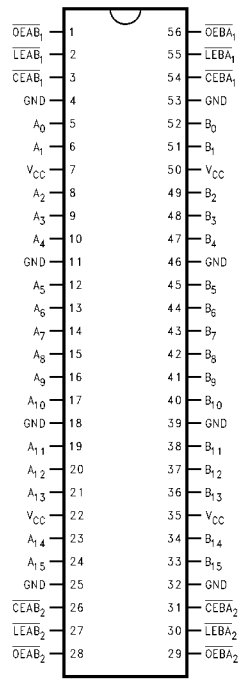
Order Number	Package Number	Package Description
74ACT16543SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16543MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Descriptions
$\overline{OEAB}_n$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}_n$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}_n$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}_n$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}_n$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}_n$	B-to-A Latch Enable Input (Active LOW)
A_0–A_{15}	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B_0–B_{15}	B-to-A Data Inputs or A-to-B 3-STATE Outputs

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Functional Description

The ACT16543 contains sixteen non-inverting transceivers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The following description applies to each byte. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}_n$) input must be LOW in order to enter data from A_0–A_{15} or take data from B_0–B_{15}, as indicated in the Data I/O Control Table. With $\overline{CEAB}_n$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}_n$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}_n$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}_n$ and $\overline{OEAB}_n$ both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$ inputs.

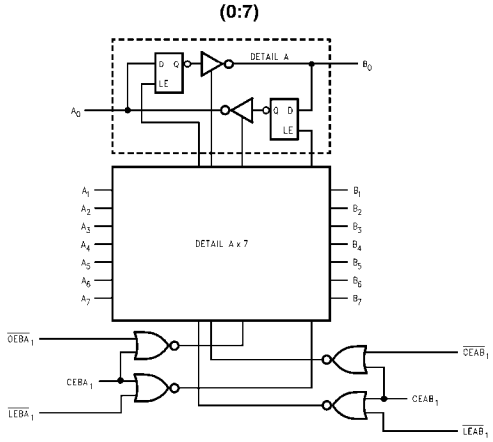
Data I/O Control Table

Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
$\overline{CEAB}_n$	$\overline{LEAB}_n$	$\overline{OEAB}_n$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

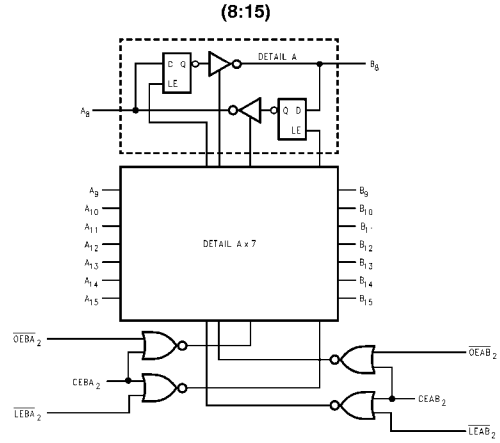
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

Logic Diagrams

Byte 1 (0:7)



Byte 2 (8:15)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	$I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 2)
V_{OL}	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	
		5.5	0.001	0.1	0.1		$I_{OUT} = 50\ \mu A$
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 2)
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.5	±5.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Max Quiescent Supply Current	5.5		8.0	80.0	µA	$V_{IN} = V_{CC}$ or GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}					−75	mA	$V_{OHD} = 3.85V$ Min

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 4)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to $B_n$or B_n to A_n	5.0	3.8 3.5	5.9 5.5	8.3 7.9	3.0 2.6	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}_n$, $\overline{LEAB}_n$ to A_n, B_n	5.0	4.7 3.9	6.9 6.3	9.8 9.0	3.4 3.1	10.8 9.8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	5.0	4.2 4.9	6.3 7.3	9.2 10.3	3.0 3.6	9.9 10.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to A_n or B_n $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to A_n or B_n	5.0	2.8 2.6	5.2 5.0	8.0 7.6	2.1 2.0	8.3 8.1	ns

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

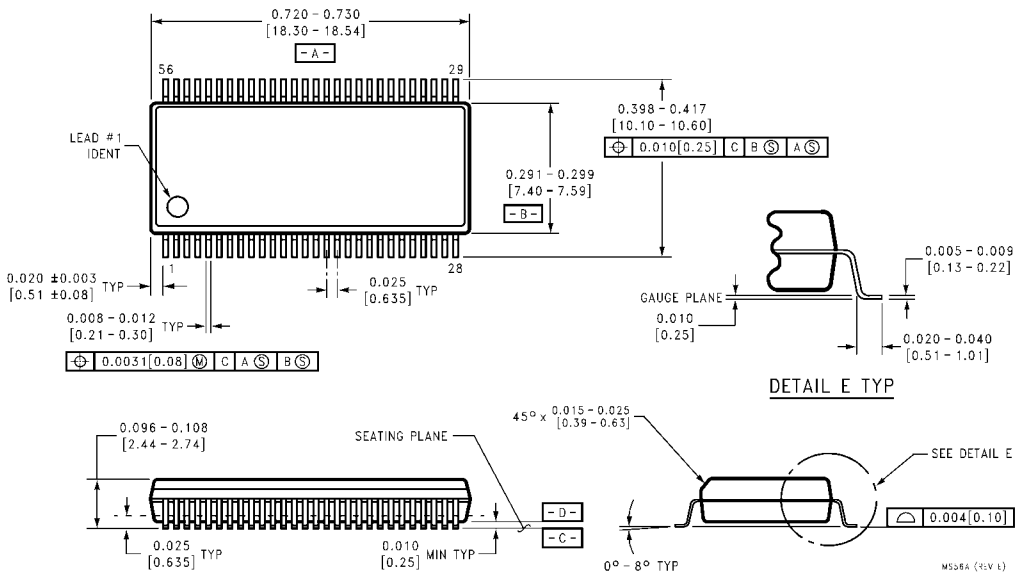
Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$, $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}_n$ or $\overline{LEAB}_n$	5.0	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}_n$ or $\overline{LEAB}_n$	5.0	1.5	1.5	ns
t_W	Latch Enable, B to A Pulse Width, LOW	5.0	4.0	4.0	ns

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

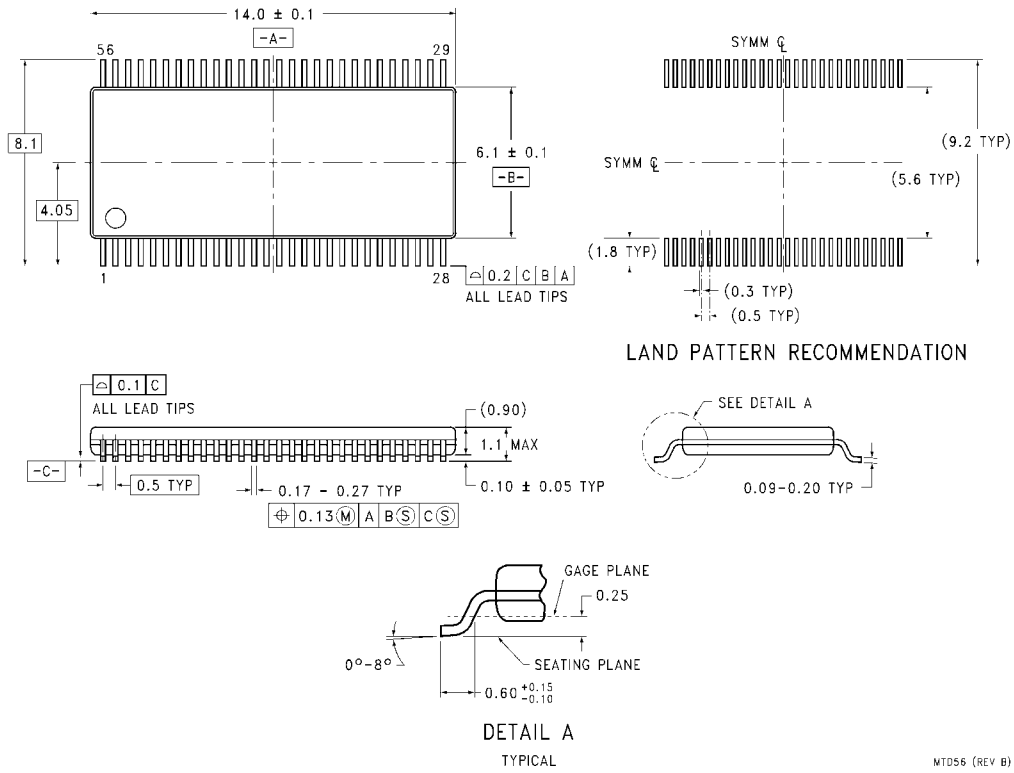
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation.Capacitance	95.0	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (SSOP), JEDEC MO-153, 6.1mm Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56