TW2826

16-Channel Record Multiplexer for Security Applications

FN7913
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TW2826 is a record multiplexer that converts multiple D1 video inputs into quad CIF format for multi-channel DVR applications. The maximum number of D1 video that can be accepted is 16. The output can be selected from any D1 video or quad CIF video.

Description

This product accepts multiple channels BT.656 compliant video data in byte interleaving format, processes them and outputs them in either its original size or in quad CIF size based on user control. The output will be in BT.656 byte interleaving format in the case of multi-channel output.

Features

- Four BT.656 Compliant Input
- Maximum Input Rate of 108 MHz with Byte-Interleaved Format Support
- Four BT.656 Compliant Output Ports
- Up to 108 MHz Byte-Interleave Output Support
- Channel ID Support
- User Selectable D1 or Quad CIF Output
- Single SDRAM 16 Bits @166MHz
- Optional GPIO
- Miscellaneous
- 1.8/3.3V Operation Voltage
- Supports 2-wire Serial Bus Interface
- 144 Ld LQFP Package

Applications

- Video Surveillance DVR

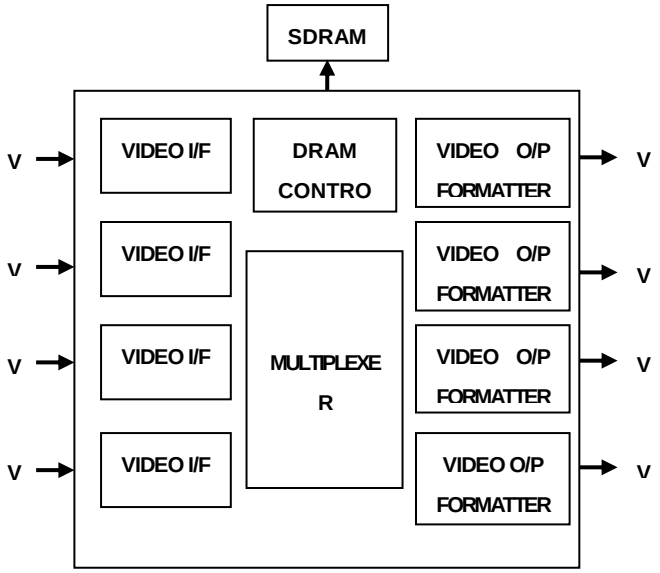

FIGURE 1. TW2826 BLOCK DIAGRAM

Pin Diagram

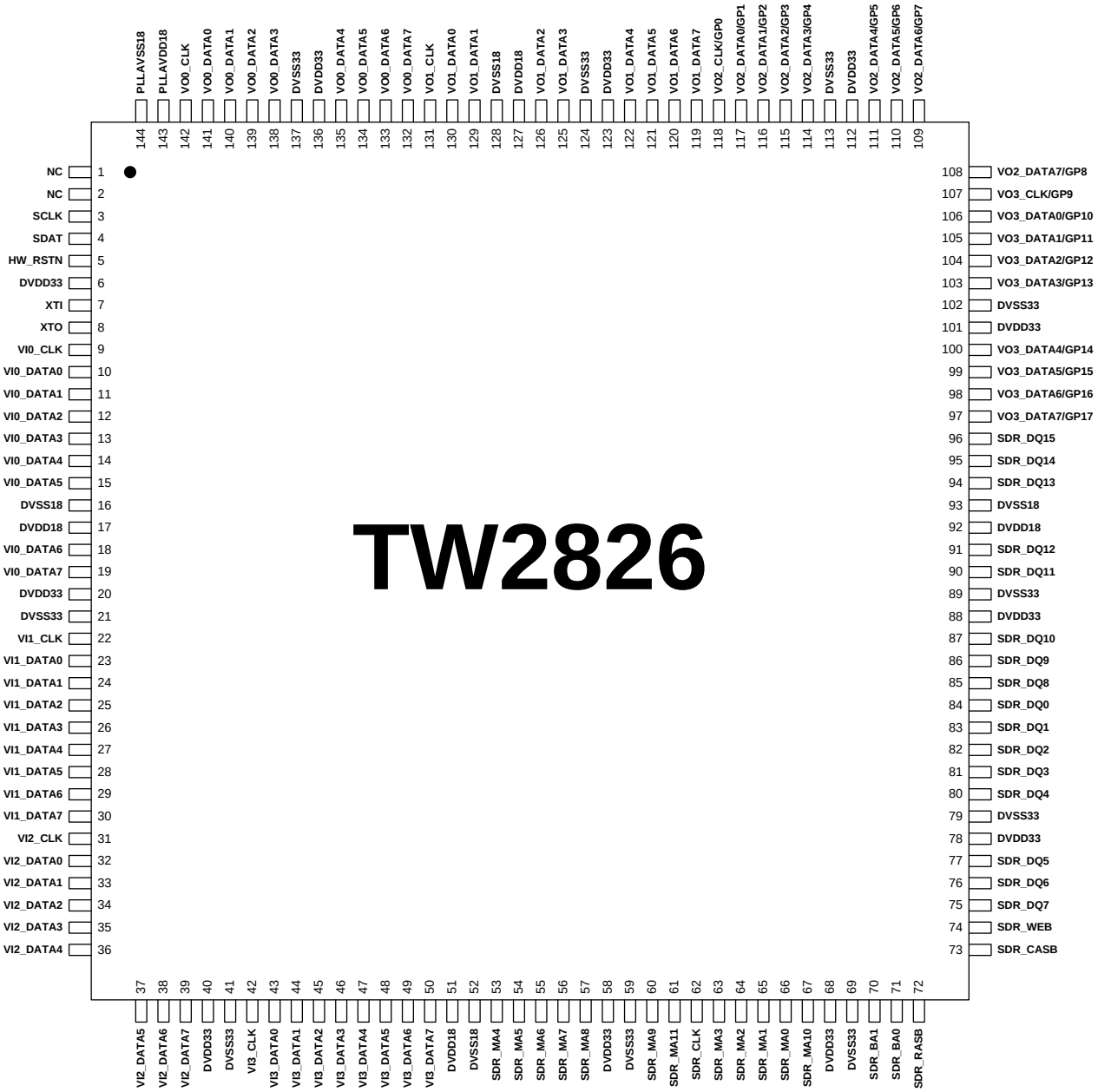

FIGURE 2. TW2826 PIN DIAGRAM

Pin Descriptions

Digital Video Input Pins

NAME	NUMBER	TYPE	DESCRIPTION
VI0_CLK	9	I	Video clock input of channel1
VI0_DATA0	10	I	Video data input of channel1, bit0
VI0_DATA1	11	I	Video data input of channel1, bit1
VI0_DATA2	12	I	Video data input of channel1, bit2
VI0_DATA3	13	I	Video data input of channel1, bit3
VI0_DATA4	14	I	Video data input of channel1, bit4
VI0_DATA5	15	I	Video data input of channel1, bit5
VI0_DATA6	18	I	Video data input of channel1, bit6
VI0_DATA7	19	I	Video data input of channel1, bit7
VI1_CLK	22	I	Video clock input of channel2
VI1_DATA0	23	I	Video data input of channel2, bit0
VI1_DATA1	24	I	Video data input of channel2, bit1
VI1_DATA2	25	I	Video data input of channel2, bit2
VI1_DATA3	26	I	Video data input of channel2, bit3
VI1_DATA4	27	I	Video data input of channel2, bit4
VI1_DATA5	28	I	Video data input of channel2, bit5
VI1_DATA6	29	I	Video data input of channel2, bit6
VI1_DATA7	30	I	Video data input of channel2, bit7
VI2_CLK	31	I	Video clock input of channel3
VI2_DATA0	32	I	Video data input of channel3, bit0
VI2_DATA1	33	I	Video data input of channel3, bit1
VI2_DATA2	34	I	Video data input of channel3, bit2
VI2_DATA3	35	I	Video data input of channel3, bit3
VI2_DATA4	36	I	Video data input of channel3, bit4
VI2_DATA5	37	I	Video data input of channel3, bit5
VI2_DATA6	38	I	Video data input of channel3, bit6
VI2_DATA7	39	I	Video data input of channel3, bit7
VI3_CLK	42	I	Video clock input of channel4
VI3_DATA0	43	I	Video data input of channel4, bit0/auto_mode (strap-pin, Auto run mode: 0 = manual-run, 1 = auto-run)
VI3_DATA1	44	I	Video data input of channel4, bit1/video_mode (strap-pin, Video system: 0 = NTSC, 1 = PAL)
VI3_DATA2	45	I	Video data input of channel4, bit2/D1_mode (strap-pin, reserved mode, 0 = normal mode, 1 = test mode)
VI3_DATA3	46	I	Video data input of channel4, bit3/VO_mode (strap-pin, Quad CIF output mode: 0 = frame CIF, 1 = field CIF)

NAME	NUMBER	TYPE	DESCRIPTION
VI3_DATA4	47	I	Video data input of channel4, bit4/mem_speed(strap-pin, memory speed: 0 = 166MHz,1 = 133MHz)
VI3_DATA5	48	I	Video data input of channel4, bit5/mem_size(strap-pin, memory size: 0 = 64Mb, 1 = 128Mb)
VI3_DATA6	49	I	Video data input of channel4, bit6/sad (strap-pin, serial bus default device ID, 0 = 0x2C, 1 = 0x2D)
VI3_DATA7	50	I	Video data input of channel4, bit7

Digital Video Output/General-purpose Pins

NAME	NUMBER	TYPE	DESCRIPTION
VO0_CLK	142	O	Video clock output of channel1
VO0_DATA0	141	O	Video data output of channel1, bit0
VO0_DATA1	140	O	Video data output of channel1, bit1
VO0_DATA2	139	O	Video data output of channel1, bit2
VO0_DATA3	138	O	Video data output of channel1, bit3
VO0_DATA4	135	O	Video data output of channel1, bit4
VO0_DATA5	134	O	Video data output of channel1, bit5
VO0_DATA6	133	O	Video data output of channel1, bit6
VO0_DATA7	132	O	Video data output of channel1, bit7
VO1_CLK	131	O	Video clock output of channel2
VO1_DATA0	130	O	Video data output of channel2, bit0
VO1_DATA1	129	O	Video data output of channel2, bit1
VO1_DATA2	126	O	Video data output of channel2, bit2
VO1_DATA3	125	O	Video data output of channel2, bit3
VO1_DATA4	122	O	Video data output of channel2, bit4
VO1_DATA5	121	O	Video data output of channel2, bit5
VO1_DATA6	120	O	Video data output of channel2, bit6
VO1_DATA7	119	O	Video data output of channel2, bit7
VO2_CLK	118	O	Video clock output of channel3/GPIO0
VO2_DATA0	117	O	Video data output of channel3, bit0/GPIO1
VO2_DATA1	116	O	Video data output of channel3, bit1/GPIO2
VO2_DATA2	115	O	Video data output of channel3, bit2/GPIO3
VO2_DATA3	114	O	Video data output of channel3, bit3/GPIO4
VO2_DATA4	111	O	Video data output of channel3, bit4/GPIO5
VO2_DATA5	110	O	Video data output of channel3, bit5/GPIO6

NAME	NUMBER	TYPE	DESCRIPTION
VO2_DATA6	109	O	Video data output of channel3, bit6/GPIO7
VO2_DATA7	108	O	Video data output of channel3, bit7/GPIO8
VO3_CLK	107	O	Video clock output of channel4/GPIO9
VO3_DATA0	106	O	Video data output of channel4, bit0/GPIO10
VO3_DATA1	105	O	Video data output of channel4, bit1/GPIO11
VO3_DATA2	104	O	Video data output of channel4, bit2/GPIO12
VO3_DATA3	103	O	Video data output of channel4, bit3/GPIO13
VO3_DATA4	100	O	Video data output of channel4, bit4/GPIO14
VO3_DATA5	99	O	Video data output of channel4, bit5/GPIO15
VO3_DATA6	98	O	Video data output of channel4, bit6/GPIO16
VO3_DATA7	97	O	Video data output of channel4, bit7/GPIO17

Memory Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
SDR_CLK	62	O	SDRAM clock
SDR_RASB	72	O	SDRAM row address selection
SDR_CASB	73	O	SDRAM column address selection
SDR_WEB	74	O	SDRAM write enable
SDR_BA0	71	O	SDRAM bank0 selection
SDR_BA1	70	O	SDRAM bank1 selection
SDR_MA0	66	O	SDRAM address bus, bit0
SDR_MA1	65	O	SDRAM address bus, bit1
SDR_MA2	64	O	SDRAM address bus, bit2
SDR_MA3	63	O	SDRAM address bus, bit3
SDR_MA4	53	O	SDRAM address bus, bit4
SDR_MA5	54	O	SDRAM address bus, bit5
SDR_MA6	55	O	SDRAM address bus, bit6
SDR_MA7	56	O	SDRAM address bus, bit7
SDR_MA8	57	O	SDRAM address bus, bit8
SDR_MA9	60	O	SDRAM address bus, bit9
SDR_MA10	67	O	SDRAM address bus, bit10
SDR_MA11	61	O	SDRAM address bus, bit11
SDR_DQ0	84	IO	SDRAM data bus, bit0

NAME	NUMBER	TYPE	DESCRIPTION
SDR_DQ1	83	IO	SDRAM data bus, bit1
SDR_DQ2	82	IO	SDRAM data bus, bit2
SDR_DQ3	81	IO	SDRAM data bus, bit3
SDR_DQ4	80	IO	SDRAM data bus, bit4
SDR_DQ5	77	IO	SDRAM data bus, bit5
SDR_DQ6	76	IO	SDRAM data bus, bit6
SDR_DQ7	75	IO	SDRAM data bus, bit7
SDR_DQ8	85	IO	SDRAM data bus, bit8
SDR_DQ9	86	IO	SDRAM data bus, bit9
SDR_DQ10	87	IO	SDRAM data bus, bit10
SDR_DQ11	90	IO	SDRAM data bus, bit11
SDR_DQ12	91	IO	SDRAM data bus, bit12
SDR_DQ13	94	IO	SDRAM data bus, bit13
SDR_DQ14	95	IO	SDRAM data bus, bit14
SDR_DQ15	96	IO	SDRAM data bus, bit15

System Control Pins

NAME	NUMBER	TYPE	DESCRIPTION
XTI	7	I	27MHz oscillator / Cristal input
XTO	8	O	27MHz Cristal output
SCLK	3	I	Serial control clock line
SDAT	4	IO	Serial control data line
HW_RSTN	5	I	System reset

Power and Ground Pins

NAME	NUMBER	TYPE	DESCRIPTION
DVDD33	6, 20, 40, 58, 68, 78, 88, 101, 112, 123, 136	P	3.3V Power for interface
DVSS33	21, 41, 59, 69, 79, 89, 102, 113, 124, 137	G	Ground for interface
DVDD18	17, 51, 92, 127	P	1.8V Power for internal logic
DVSS18	16,52,93,128	G	Ground for internal logic
PLLAVDD18	143	P	1.8V Power for PLLs
PLLAVSS18	144	G	Ground for PLLs

Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
TW2826-LA2-CR (Note 1)	TW2826 LA2-CR	144 Ld LQFP	Q144.20X20

NOTE:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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Functional Description

Video Input

There are four physical BT.656 complaint video input ports; each port must be 108 MHz 4- channel byte interleave. The TW2826 can handle up to 16 channels D1 video input data.

Each channel video input data has its own independent sync-processing engine, which can handle sync-lost, double EAV, double SAV, illegal length between sync, etc. un-normal/illegal video input signal and recover to normal BT.656 data.

The TW2826 video output can bypass any input video, so it require the TW2826 and front end video decoder chip (TW2868/TW2866/TW2864) having the same clock source.

Please refer "Application Guide 1: System Design Consideration" on page 36 on system clock, and Guide 5 and 6 on video input setting and channel ID detection.

Video Multiplex Engine

There are four identical video multiplex engines inside TW2826. Each video input port has one independent video multiplex engine, can down-sample four channel D1 video into four CIF video, write into the SDRAM, then read back and multiplex them into one Quad CIF D1 sending out through video output port.

The video multiplex engine has field and frame operation mode:

The Field mode only selects odd line video input data, drop off even line data, then do the horizontal down-sample, in this mode, use less memory band-width (can use 133MHz SDRAM). the video output is visible, better for fast moving situation, we suggest back end video encoder use FIELD mode (in H264 case, main profile field mode) to do the video compression.

The Frame mode will only selects one field video input data, drop off another field, then do the horizontal down-sample, this mode use more memory band-width(must use 166MHz SDRAM), generate more stable image, the video output format is DVR friendly, we suggest the back end video compress engine working on FRAME mode (In H.264 case, base-line frame mode)

Please refer to "Application Guide 7: Video Multiplex Engine Configuration" on page 39 on configuration.

DRAM Controller

The TW2826 uses a single 16 bits SRAM, the memory size can be 64Mb or 128Mb, and the speed can be 133 MHz or 166 MHz (please refer to "Video Multiplex Engine" section on the speed selection).

Although 128Mb will provide bigger frame buffer, but by default, we suggest to use the 64Mb memory to save system cost.

The memory size and speed information can be configured by strap pins in chip boot up sequence, where VI3_DATA4 serves for memory speed setting, and VI3_DATA5 serves for memory size information.

The outside SDRAM component provide frame buffers for video multiplex processing, in the case of only aggregating video data directly from 16 video input D1 data (not doing any video multiplexing from input D1 video into Quad CIF D1 video), the TW2826 can run without SDRAM.

Video Output

The video output formatter/aggregator engine can aggregate up to four channels video data into one VO port, the data source can be from 16 video input D1 data, or from 4 video multiplex engines (Quad CIF), the configuration is very flexible, you almost can aggregate any of these 20 video sources in any combination.

There are four physical video output ports, each port has its own video output clock, and the clock can be configured into eight different phase delay to its corresponding video output data.

The TW2826 supports a standard ITU-R BT.656 format. To unify our design, the fourth sync word always carry the channel ID information, even in 27MHz single channel case, that means we don't support sync word CRC mechanism in our video output format.

ITU-R BT.656 FORMAT

In ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. The output timing is illustrated in Figure 3. The SAV and EAV sequences are shown in Table 1.

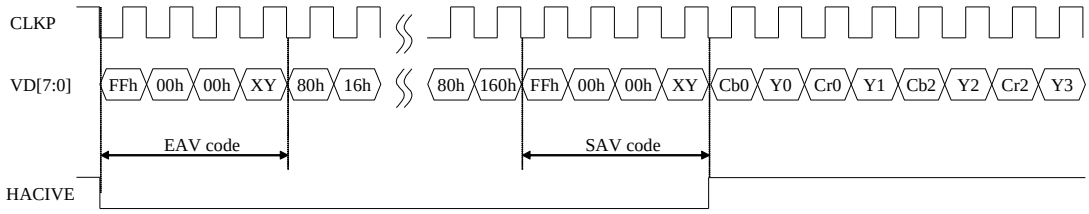

FIGURE 3. TIMING DIAGRAM OF ITU-R BT.656 FORMAT

TABLE 1. ITU-R BT.656 SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE			
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	FOURTH
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80

TWO CHANNEL ITU-R BT.656 TIME-MULTIPLEXED FORMAT WITH 54MHZ

The TW2826 supports two channels ITU-R BT.656 time-multiplexed format with 54MHz.

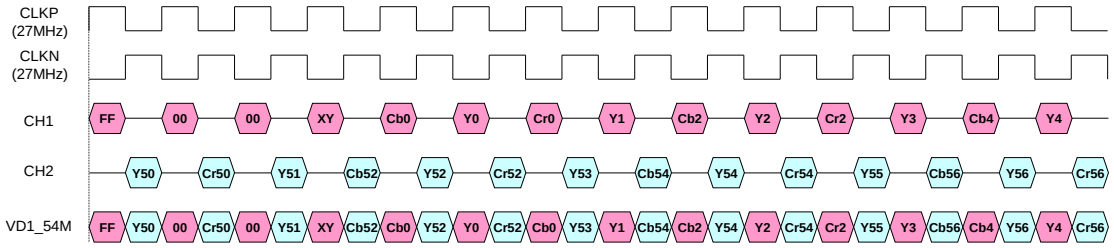

FIGURE 4. TIMING DIAGRAM OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 54MHZ

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TABLE 2. SHOWS THE SPECIAL FORMAT OF ITU-R BT.656 EMBEDDED TIMING CODE AND 2 CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE				
									Fourth	
Field	V-time	H-time	F	V	H	First	Second	Third	Ch1	Ch2
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81

FOUR CHANNEL D1 TIME-DIVISION-MULTIPLEXED FORMAT WITH 108MHZ

The TW2826 also supports four channels ITU-R BT.656 time-multiplexed format with 108MHz.

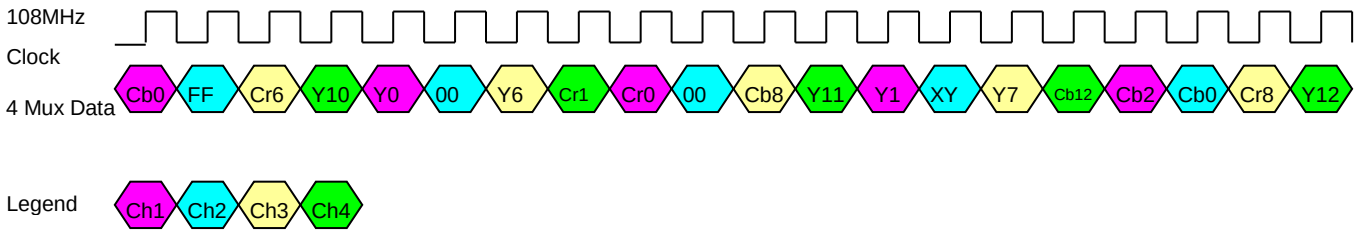


FIGURE 5. TIMING DIAGRAM OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA

TABLE 3. SHOWS THE SPECIAL FORMAT OF ITU-R BT.656 EMBEDDED TIMING CODE AND 4 CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									Fourth			
Field	V-time	H-time	F	V	H	First	Second	Third	Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

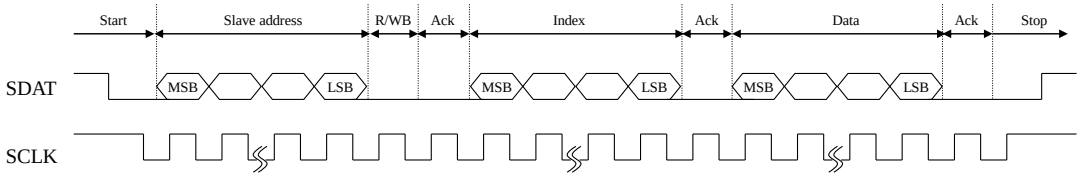
Host Interface

Serial Interface

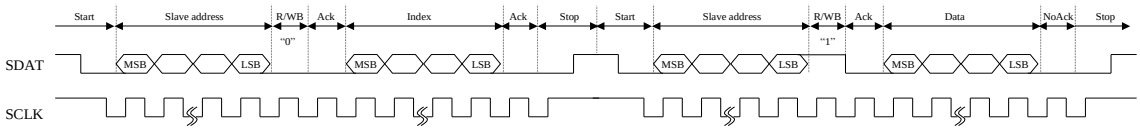
The 2-wire serial bus interface is used to allow an external micro-controller to write to or read from the data through the TW2826 register. The SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by the resistors connected to VDD. The SADD_R (0x25[6]) where the data come from strapping pin VI3_DATA6, defines LSB of the slave device ID/address. The data transfer rate on the bus is up to 400 Kbits/s.

TABLE 4. SERIAL BUS DEVICE ID

SLAVE ADDRESS							R/W
0	1	0	1	1	0	SADD_R	1 = Read 0 = Write



(A) WRITE MODE



(B)READ MODE

FIGURE 6. TIMING CHART OF SERIAL INTERFACE

Control Register

REGISTER MAP

Note:

All address not listed are reserved.

On table in the following:

- RSV means reserved
- <RO> or R means read only
- <WO> or W means write only
- <W>/<R> or W/R means write and read register(s) are difference.
- {xx} default value

Please **DO NOT WRITE/MODIFY** any reserved address or bit(s) to its non-default value, most of them are reserved for debugging purpose, miss modifying will result in unexpected behavior, even damage the chip.

All the register bits default value should be “0”, except we put default value comment {xx}

ADDRESS	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x20	CTRL0	SOFT_RESET <WO>	RSV	RSV	RSV	RSV	RSV	VIO_STOP<WO>	VIO_START <WO>
0X21	CTRL1	RSV	RSV	RSV		FRAME_TOP{1}	FRAME_MODE{1}	RSV	RSV
0X22	CTRL2	VIN_CFG[3:0]				RSV	RSV	RSV	RSV
0X23	CTRL3	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
0X24	CTRL4	RSV	RSV	RSV	TOP_SEL_SET_ON	RSV	RSV	RSV	RSV
0X25	STRAP_STATUS	RSV	SADD_R<RO>	MEM_SZ_R<RO>	SPEED_MODE_R<RO>	VO_MODE_R<RO>	D1_MODE<RO>	V_MODE_R<RO>	AUTO_MODE_R<RO>
0X26	TOP_SEL_SET0	TOP_SEL_SET[7:0]							
0X27	TOP_SEL_SET1	TOP_SEL_SET[15:8]							

ADDRESS	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x30	VO_CLK_CFG_0	RSV	RSV	RSV	VO_CLK_CFG_0[4:0] {5'h04}				
0X31	VO_CLK_CFG_1	RSV	RSV	RSV	VO_CLK_CFG_1[4:0] {5'h04}				
0X32	VO_CLK_CFG_2	RSV	RSV	RSV	VO_CLK_CFG_2[4:0] {5'h04}				
0X33	VO_CLK_CFG_3	RSV	RSV	RSV	VO_CLK_CFG_3[4:0] {5'h04}				
0X34	VO_CFG_0_CH0	RSV	RSV	VIDEO_SOURCE[1:0]{2'h2}		VIDEO_SOURCE_CH[3:0]			
0X35	VO_CFG_0_CH1	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X36	VO_CFG_0_CH2	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X37	VO_CFG_0_CH3	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X38	VO_CFG_1_CH0	RSV	RSV	VIDEO_SOURCE[1:0]{2'h2}		VIDEO_SOURCE_CH[3:0]			
0X39	VO_CFG_1_CH1	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X3A	VO_CFG_1_CH2	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X3B	VO_CFG_1_CH3	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X3C	VO_CFG_2_CH0	RSV	RSV	VIDEO_SOURCE[1:0]{2'h2}		VIDEO_SOURCE_CH[3:0]			
0X3D	VO_CFG_2_CH1	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X3E	VO_CFG_2_CH2	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X3F	VO_CFG_2_CH3	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X40	VO_CFG_3_CH0	RSV	RSV	VIDEO_SOURCE[1:0]{2'h2}		VIDEO_SOURCE_CH[3:0]			
0X41	VO_CFG_3_CH1	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X42	VO_CFG_3_CH2	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			
0X43	VO_CFG_3_CH3	RSV	RSV	VIDEO_SOURCE[1:0]		VIDEO_SOURCE_CH[3:0]			

ADDRESS	MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x47	REV_ID	REV_ID[7:0] <RO>							
0X88	VO2_GPIO_CTRL0	VO2_GPIO_OUT_1_SEL	VO2_GPIO_OUT_1_EN	VO2_GPIO_OUT_1	VO2_GPIO_IN_1	VO2_GPIO_OUT_0_SEL	VO2_GPIO_OUT_0_EN	VO2_GPIO_OUT_0	VO2_GPIO_IN_0
0X89	VO2_GPIO_CTRL1	VO2_GPIO_OUT_3_SEL	VO2_GPIO_OUT_3_EN	VO2_GPIO_OUT_3	VO2_GPIO_IN_3	VO2_GPIO_OUT_2_SEL	VO2_GPIO_OUT_2_EN	VO2_GPIO_OUT_2	VO2_GPIO_IN_2
0X8A	VO2_GPIO_CTRL2	VO2_GPIO_OUT_5_SEL	VO2_GPIO_OUT_5_EN	VO2_GPIO_OUT_5	VO2_GPIO_IN_5	VO2_GPIO_OUT_4_SEL	VO2_GPIO_OUT_4_EN	VO2_GPIO_OUT_4	VO2_GPIO_IN_4
0X8B	VO2_GPIO_CTRL3	VO2_GPIO_OUT_7_SEL	VO2_GPIO_OUT_7_EN	VO2_GPIO_OUT_7	VO2_GPIO_IN_6	VO2_GPIO_OUT_6_SEL	VO2_GPIO_OUT_6_EN	VO2_GPIO_OUT_6	VO2_GPIO_IN_6
0X8C	VO3_GPIO_CTRL0	VO3_GPIO_OUT_1_SEL	VO3_GPIO_OUT_1_EN	VO3_GPIO_OUT_1	VO3_GPIO_IN_1	VO3_GPIO_OUT_0_SEL	VO3_GPIO_OUT_0_EN	VO3_GPIO_OUT_0	VO3_GPIO_IN_0
0X8D	VO3_GPIO_CTRL1	VO3_GPIO_OUT_3_SEL	VO3_GPIO_OUT_3_EN	VO3_GPIO_OUT_3	VO3_GPIO_IN_3	VO3_GPIO_OUT_2_SEL	VO3_GPIO_OUT_2_EN	VO3_GPIO_OUT_2	VO3_GPIO_IN_2
0X8E	VO3_GPIO_CTRL2	VO3_GPIO_OUT_5_SEL	VO3_GPIO_OUT_5_EN	VO3_GPIO_OUT_5	VO3_GPIO_IN_5	VO3_GPIO_OUT_4_SEL	VO3_GPIO_OUT_4_EN	VO3_GPIO_OUT_4	VO3_GPIO_IN_4
0X8F	VO3_GPIO_CTRL3	VO3_GPIO_OUT_7_SEL	VO3_GPIO_OUT_7_EN	VO3_GPIO_OUT_7	VO3_GPIO_IN_6	VO3_GPIO_OUT_6_SEL	VO3_GPIO_OUT_6_EN	VO3_GPIO_OUT_6	VO3_GPIO_IN_6
0X90	VO_CLK_GPIO_CTRL	VO3_CLK_GPIO_OUT_SEL	VO3_CLK_GPIO_OUT_EN	VO3_CLK_GPIO_OUT	VO3_CLK_GPIO_IN	VO3_CLK_GPIO_OUT_SEL	VO2_CLK_GPIO_OUT_EN	VO2_CLK_GPIO_OUT	VO2_CLK_GPIO_IIN

REGISTER DESCRIPTION

0X20 – CONTROL0 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	SOFT_RESET	W	1 = write 1 to do the whole chip software reset 0 = do nothing	0
6	RSV	R	Reserved	0
5	RSV	R	Reserved	0
4	RSV	R	Reserved	0
3	RSV	R	Reserved	0
2	RSV	R	Reserved	0
1	VIO_STOP	W	1 = write 1 to stop the chip from working 0 = do nothing	0
0	VIO_START/VIO_EN	R/W	Write operation: 1 = write 1 to start the chip to working 0 = do nothing Read operation: 1 = indicate chip is in working 0 = indicate chip is in stop	0

0X21 – CONTROL1 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	0
6	RSV	R	Reserved	0
5-4	RSV[1:0]	R/W	Reserved	2'h0
3	FRAME_TOP	R/W	Only take effect when 0x21[1](FRAME_MODE) = 1 1 = down sample engine will pick video input top field only 0 = down sample engine will pick the top/bottom field base on customer setting Please refer to "Application Guide 7: Video Multiplex Engine Configuration" on page 39 for details	1
2	FRAME_MODE	R/W	0 = field mode 1 = frame mode Please refer to "Application Guide 7: Video Multiplex Engine Configuration" on page 39 for details	1
1	RSV	R	Reserved	0
0	RSV	R	Reserved	0

0X22 – CONTROL2 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7-4	VIN_CFG[3:0]	R/W	vin_cfg[0] = video input port0 vin_cfg[1] = video input port1 vin_cfg[2] = video input port2 vin_cfg[3] = video input port3 0 = use posedge to latch-in video input data 1 = use negedge to latch-in video input data	4'h0
3	RSV	R	Reserved	0
2	RSV	R	Reserved	0
1	RSV	R	Reserved	0
0	RSV	R	Reserved	0

0X24 – CONTROL4 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	0
6	RSV	R	Reserved	0
5	RSV	R	Reserved	0
4	TOP_SEL_SET_ON	R/W	1 = down sample engine will pick input video field by user define (register 0x26-0x27) 0 = down sample engine will pick input video field randomly	0
3	RSV	R	Reserved	0
2	RSV	R	Reserved	0
1	RSV	R	Reserved	0
0	RSV	R	Reserved	0

0X25 – STRAP STATUS REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	1
6	SADD_R	R	1 = the serial bus device ID is 0x2D 0 = the serial bus device ID is 0x2C	0
5	MEM_SZ_R	R	1 = the SDRAM size is 128Mb 0 = the SDRAM size is 64Mb	0
4	SPEED_MODE_R	R	1 = the SDRAM is 133MHz 0 = the SDRAM is 166MHz	0
3	VO_MODE_R	R	1 = video output is in field mode 0 = video output is in frame mode	0
2	D1_MODE_R	R	1 = d1 mode (for intersil internal test/debug) 0 = normal operation mode	0
1	V_MODE_R	R	1 = the video system is PAL 0 = the video system id NTSC	0
0	AUTO_MODE_R	R	1 = the chip is in auto run mode, after hardware reset, the hardware engine will run. 0 = the chip is in manual run mode, need to write bit0 of 0x20 to 1 to run	0

0X26 – TOP_SEL_SET0 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	TOP_SEL_SET[7]	R/W	Video input port1,Channel 3: 1 = pick bottom field 0 = pick top field	0
6	TOP_SEL_SET[6]	R/W	Video input port1,Channel 2: 1 = pick bottom field 0 = pick top field	0
5	TOP_SEL_SET[5]	R/W	Video input port1,Channel 1: 1 = pick bottom field 0 = pick top field	0
4	TOP_SEL_SET[4]	R/W	Video input port1,Channel 0: 1 = pick bottom field 0 = pick top field	0
3	TOP_SEL_SET[3]	R/W	Video input port0,Channel 3: 1 = pick bottom field 0 = pick top field	0
2	TOP_SEL_SET[2]	R/W	Video input port0,Channel 2: 1 = pick bottom field 0 = pick top field	0
1	TOP_SEL_SET[1]	R/W	Video input port0,Channel 1: 1 = pick bottom field 0 = pick top field	0
0	TOP_SEL_SET[0]	R/W	Video input port0,Channel 0: 1 = pick bottom field 0 = pick top field	0

NOTE:

only takes effect when:

0x21[2] (FRAME_MODE) = 1

0x21[3] (FRAME_TOP) = 0

0x24[4] (TOP_SEL_SET_ON) = 1

0X27 – TOP_SEL_SET1 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	TOP_SEL_SET[15]	R/W	Video input port3,Channel 3: 1 = pick bottom field 0 = pick top field	0
6	TOP_SEL_SET[14]	R/W	Video input port3,Channel 2: 1 = pick bottom field 0 = pick top field	0
5	TOP_SEL_SET[13]	R/W	Video input port3,Channel 1: 1 = pick bottom field 0 = pick top field	0
4	TOP_SEL_SET[12]	R/W	Video input port3,Channel 0: 1 = pick bottom field 0 = pick top field	0
3	TOP_SEL_SET[11]	R/W	Video input port2,Channel 3: 1 = pick bottom field 0 = pick top field	0
2	TOP_SEL_SET[10]	R/W	Video input port2,Channel 2: 1 = pick bottom field 0 = pick top field	0
1	TOP_SEL_SET[9]	R/W	Video input port2,Channel 1: 1 = pick bottom field 0 = pick top field	0
0	TOP_SEL_SET[8]	R/W	Video input port2,Channel 0: 1 = pick bottom field 0 = pick top field	0

NOTE:

only takes effect when:

0x21[2] (FRAME_MODE) = 1

0x21[3] (FRAME_TOP) = 0

0x24[4] (TOP_SEL_SET_ON) = 1

0X30 – VO_CLK_CFG_0 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	0
6	RSV	R	Reserved	0
5	RSV	R	Reserved	0
4-3	VO_CLK_CFG_0[4:3]	R/W	vo0_clk frequency: 2'b00:27MHz {default} 2'b01:54MHz 2'b10:108MHz 2'b11:reserved	2'h0
2-0	VO_CLK_CFG_0[2:0]	R/W	vo0_clk phase delay to the vo0_data[7:0]: 3'b000:0 degrees delay 3'b001:45 degrees delay 3'b010:90 degrees delay 3'b011:135 degrees delay 3'b100:180 degrees delay {default} 3'b101:225 degrees delay 3'b110:270 degrees delay 3'b111:315 degrees delay	3'h4

0X31 – VO_CLK_CFG_1 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	0
6	RSV	R	Reserved	0
5	RSV	R	Reserved	0
4-3	VO_CLK_CFG_1[4:3]	R/W	vo1_clk clock frequency: 2'b00:27MHz {default} 2'b01:54MHz 2'b10:108MHz 2'b11:reserved	2'h0
2-0	VO_CLK_CFG_1[2:0]	R/W	vo1_clk phase delay to the vo1_data[7:0]: 3'b000:0 degrees delay 3'b001:45 degrees delay 3'b010:90 degrees delay 3'b011:135 degrees delay 3'b100:180 degrees delay {default} 3'b101:225 degrees delay 3'b110:270 degrees delay	3'h4

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
			3'b111:315 degrees delay	

0X32 – VO_CLK_CFG_2 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	0
6	RSV	R	Reserved	0
5	RSV	R	Reserved	0
4-3	VO_CLK_CFG_2[4:3]	R/W	vo2_clk frequency: 2'b00:27MHz {default} 2'b01:54MHz 2'b10:108MHz 2'b11:reserved	2'h0
2-0	VO_CLK_CFG_2[2:0]	R/W	vo2_clk phase delay to the vo2_data[7:0]: 3'b000:0 degrees delay 3'b001:45 degrees delay 3'b010:90 degrees delay 3'b011:135 degrees delay 3'b100:180 degrees delay {default} 3'b101:225 degrees delay 3'b110:270 degrees delay 3'b111:315 degrees delay	3'h4

0X33 – VO_CLK_CFG_3 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	0
6	RSV	R	Reserved	0
5	RSV	R	Reserved	0
4-3	VO_CLK_CFG_3[4:3]	R/W	vo3_clk frequency: 2'b00:27MHz {default} 2'b01:54MHz 2'b10:108MHz 2'b11:reserved	2'h0
2-0	VO_CLK_CFG_3[2:0]	R/W	vo3_clk phase delay to the vo03_data[7:0]: 3'b000:0 degrees delay 3'b001:45 degrees delay	3'h4

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
			3’b010:90 degrees delay 3’b011:135 degrees delay 3’b100:180 degrees delay {default} 3’b101:225 degrees delay 3’b110:270 degrees delay 3’b111:315 degrees delay	

0X34 –0X43: VIDEO OUTPUT FORMATTER CONTROL REGISTERS

0x34: Configure video output port0 channel0 data source
0x35: Configure video output port0 channel1 data source
0x36: Configure video output port0 channel2 data source
0x37: Configure video output port0 channel3 data source
0x38: Configure video output port1 channel0 data source
0x39: Configure video output port1 channel1 data source
0x3A: Configure video output port1 channel2 data source
0x3B: Configure video output port1 channel3 data source
0x3C: Configure video output port2 channel0 data source
0x3D: Configure video output port2 channel1 data source
0x40: Configure video output port2 channel2 data source
0x41: Configure video output port2 channel3 data source
0x42: Configure video output port3 channel0 data source
0x43: Configure video output port3 channel1 data source
0x44: Configure video output port3 channel2 data source
0x45: Configure video output port3 channel3 data source

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	RSV	R	Reserved	0
6	RSV	R	Reserved	0
5-4	VIDEO_SOURCE[1:0]	R/W	2'b11:direct from video input port, detail channel number is in bit3-bit0 2'b10:from down sample engine, detail channel number is in bit3-bit0 2'b00,2'b01:reserved	0x34/38/3c/40 is 2'h2,others is 2'h0
3-0	VIDEO_SOURCE_CH[3:0]	R/W	When video_source[1:0] is 2'b11: 4'b0000:from video input port0 channel0 4'b0001:from video input port0 channel1 4'b0010:from video input port0 channel2 4'b0011:from video input port0 channel3 4'b0100:from video input port1 channel0 4'b0101:from video input port1 channel1 4'b0110:from video input port1 channel2	0x34=4'h00x38=4'h10x3c=4'h20x40=4'h3 others is 4'h0

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
			4’b0111:from video input port1 channel3 4’b1000:from video input port2 channel0 4’b1001:from video input port2 channel1 4’b1010:from video input port2 channel2 4’b1011:from video input port2 channel3 4’b1100:from video input port3 channel0 4’b1101:from video input port3 channel1 4’b1110:from video input port3 channel2 4’b1111:from video input port3 channel3 When video_source[1:0] is 2’b10: video_source_ch[1:0]=2’b00: from video port0 down sample engine video_source_ch[1:0]=2’b01: from video port1 down sample engine video_source_ch[1:0]=2’b02: from video port2 down sample engine video_source_ch[1:0]=2’b03: from video port3 down sample engine video_source_ch[3:2]:not used	

0X47 – TW2826 REVISION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7-0	REV_ID[7:0]	R	TW2826 revision ID	8'h00

0X88: VO2 GPIO CONTROL0 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO2_GPIO_OUT_1_SEL	R/W	VO2_DATA1 output select: 0: VO2_DATA1 data source is video engine 1:VO2_DATA1 data source is vo2_gpio_out_1(0x88[5])	0
6	VO2_GPIO_OUT_1_EN	R/W	VO2_DATA1 output enable: 0: VO2_DATA1 is output 1: VO2_DATA1 is input	0
5	VO2_GPIO_OUT_1	R/W	VO2_DATA1 output value as GPIO output	0
4	VO2_GPIO_IN_1	R	VO2_DATA1 input value as GPIO input	0
3	VO2_GPIO_OUT_0_SEL	R/W	VO2_DATA0 output select: 0: VO2_DATA0 data source is video engine 1:VO2_DATA0 data source is vo2_gpio_out_0(0x88[1])	0
2	VO2_GPIO_OUT_0_EN	R/W	VO2_DATA0 output enable: 0: VO2_DATA0 is output 1: VO2_DATA0 is input	0
1	VO2_GPIO_OUT_0	R/W	VO2_DATA0 output value as GPIO output	0
0	VO2_GPIO_IN_0	R	VO2_DATA0 input value as GPIO input	0

0X89: VO2 GPIO CONTROL1 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO2_GPIO_OUT_3_SEL	R/W	VO2_DATA3 output select: 0: VO2_DATA3 data source is video engine 1:VO2_DATA3 data source is vo2_gpio_out_3(0x89[5])	0
6	VO2_GPIO_OUT_3_EN	R/W	VO2_DATA3 output enable: 0: VO2_DATA3 is output 1: VO2_DATA3 is input	0
5	VO2_GPIO_OUT_3	R/W	VO2_DATA3 output value as GPIO output	0
4	VO2_GPIO_IN_3	R	VO2_DATA3 input value as GPIO input	0
3	VO2_GPIO_OUT_2_SEL	R/W	VO2_DATA2 output select: 0: VO2_DATA2 data source is video engine 1:VO2_DATA2 data source is vo2_gpio_out_2(0x89[1])	0
2	VO2_GPIO_OUT_2_EN	R/W	VO2_DATA2 output enable: 0: VO2_DATA2 is output 1: VO2_DATA2 is input	0
1	VO2_GPIO_OUT_2	R/W	VO2_DATA2 output value as GPIO output	0
0	VO2_GPIO_IN_2	R	VO2_DATA2 input value as GPIO input	0

0X8A: VO2 GPIO CONTROL2 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO2_GPIO_OUT_5_SEL	R/W	VO2_DATA5 output select: 0: VO2_DATA5 data source is video engine 1:VO2_DATA5 data source is vo2_gpio_out_5(0x8A[5])	0
6	VO2_GPIO_OUT_5_EN	R/W	VO2_DATA5 output enable: 0: VO2_DATA5 is output 1: VO2_DATA5 is input	0
5	VO2_GPIO_OUT_5	R/W	VO2_DATA5 output value as GPIO output	0
4	VO2_GPIO_IN_5	R	VO2_DATA5 input value as GPIO input	0
3	VO2_GPIO_OUT_4_SEL	R/W	VO2_DATA4 output select: 0: VO2_DATA4 data source is video engine 1:VO2_DATA4 data source is vo2_gpio_out_4(0x8A[1])	0
2	VO2_GPIO_OUT_4_EN	R/W	VO2_DATA4 output enable: 0: VO2_DATA4 is output 1: VO2_DATA4 is input	0
1	VO2_GPIO_OUT_4	R/W	VO2_DATA4 output value as GPIO output	0
0	VO2_GPIO_IN_4	R	VO2_DATA4 input value as GPIO input	0

0X8B: VO2 GPIO CONTROL3 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO2_GPIO_OUT_7_SEL	R/W	VO2_DATA7 output select: 0: VO2_DATA7 data source is video engine 1:VO2_DATA7 data source is vo2_gpio_out_7(0x8B[5])	0
6	VO2_GPIO_OUT_7_EN	R/W	VO2_DATA7 output enable: 0: VO2_DATA7 is output 1: VO2_DATA7 is input	0
5	VO2_GPIO_OUT_7	R/W	VO2_DATA7 output value as GPIO output	0
4	VO2_GPIO_IN_7	R	VO2_DATA7 input value as GPIO input	0
3	VO2_GPIO_OUT_6_SEL	R/W	VO2_DATA6 output select: 0: VO2_DATA6 data source is video engine 1:VO2_DATA6 data source is vo2_gpio_out_6(0x8B[1])	0
2	VO2_GPIO_OUT_6_EN	R/W	VO2_DATA6 output enable: 0: VO2_DATA6 is output 1: VO2_DATA6 is input	0
1	VO2_GPIO_OUT_6	R/W	VO2_DATA6 output value as GPIO output	0
0	VO2_GPIO_IN_6	R	VO2_DATA6 input value as GPIO input	0

0X8C: VO3 GPIO CONTROL0 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO3_GPIO_OUT_1_SEL	R/W	VO3_DATA1 output select: 0: VO3_DATA1 data source is video engine 1:VO3_DATA1 data source is vo3_gpio_out_1(0x8C[5])	0
6	VO3_GPIO_OUT_1_EN	R/W	VO3_DATA1 output enable: 0: VO3_DATA1 is output 1: VO3_DATA1 is input	0
5	VO3_GPIO_OUT_1	R/W	VO3_DATA1 output value as GPIO output	0
4	VO3_GPIO_IN_1	R	VO3_DATA1 input value as GPIO input	0
3	VO3_GPIO_OUT_0_SEL	R/W	VO3_DATA0 output select: 0: VO3_DATA0 data source is video engine 1:VO3_DATA0 data source is vo3_gpio_out_0(0x8C[1])	0
2	VO3_GPIO_OUT_0_EN	R/W	VO3_DATA0 output enable: 0: VO3_DATA0 is output 1: VO3_DATA0 is input	0
1	VO3_GPIO_OUT_0	R/W	VO3_DATA0 output value as GPIO output	0
0	VO3_GPIO_IN_0	R	VO3_DATA0 input value as GPIO input	0

0X8D: VO3 GPIO CONTROL1 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO3_GPIO_OUT_3_SEL	R/W	VO3_DATA3 output select: 0: VO3_DATA3 data source is video engine 1:VO3_DATA3 data source is vo3_gpio_out_3(0x8D[5])	0
6	VO3_GPIO_OUT_3_EN	R/W	VO3_DATA3 output enable: 0: VO3_DATA3 is output 1: VO3_DATA3 is input	0
5	VO3_GPIO_OUT_3	R/W	VO3_DATA3 output value as GPIO output	0
4	VO3_GPIO_IN_3	R	VO3_DATA3 input value as GPIO input	0
3	VO3_GPIO_OUT_2_SEL	R/W	VO3_DATA2 output select: 0: VO3_DATA2 data source is video engine 1:VO3_DATA2 data source is vo3_gpio_out_2(0x8D[1])	0
2	VO3_GPIO_OUT_2_EN	R/W	VO3_DATA2 output enable: 0: VO3_DATA2 is output 1: VO3_DATA2 is input	0
1	VO3_GPIO_OUT_2	R/W	VO3_DATA2 output value as GPIO output	0
0	VO3_GPIO_IN_2	R	VO3_DATA2 input value as GPIO input	0

0X8E: VO3 GPIO CONTROL2 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO3_GPIO_OUT_5_SEL	R/W	VO3_DATA5 output select: 0: VO3_DATA5 data source is video engine 1:VO3_DATA5 data source is vo3_gpio_out_5(0x8E[5])	0
6	VO3_GPIO_OUT_5_EN	R/W	VO3_DATA5 output enable: 0: VO3_DATA5 is output 1: VO3_DATA5 is input	0
5	VO3_GPIO_OUT_5	R/W	VO3_DATA5 output value as GPIO output	0
4	VO3_GPIO_IN_5	R	VO3_DATA5 input value as GPIO input	0
3	VO3_GPIO_OUT_4_SEL	R/W	VO3_DATA4 output select: 0: VO3_DATA4 data source is video engine 1:VO3_DATA4 data source is vo3_gpio_out_4(0x8E[1])	0
2	VO3_GPIO_OUT_4_EN	R/W	VO3_DATA4 output enable: 0: VO3_DATA4 is output 1: VO3_DATA4 is input	0
1	VO3_GPIO_OUT_4	R/W	VO3_DATA4 output value as GPIO output	0
0	VO3_GPIO_IN_4	R	VO3_DATA4 input value as GPIO input	0

0X8F: VO3 GPIO CONTROL3 REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO3_GPIO_OUT_7_SEL	R/W	VO3_DATA7 output select: 0: VO3_DATA7 data source is video engine 1:VO3_DATA7 data source is vo3_gpio_out_7(0x8F[5])	0
6	VO3_GPIO_OUT_7_EN	R/W	VO3_DATA7 output enable: 0: VO3_DATA7 is output 1: VO3_DATA7 is input	0
5	VO3_GPIO_OUT_7	R/W	VO3_DATA7 output value as GPIO output	0
4	VO3_GPIO_IN_7	R	VO3_DATA7 input value as GPIO input	0
3	VO3_GPIO_OUT_6_SEL	R/W	VO3_DATA6 output select: 0: VO3_DATA6 data source is video engine 1:VO3_DATA6 data source is vo3_gpio_out_6(0x8F[1])	0
2	VO3_GPIO_OUT_6_EN	R/W	VO3_DATA6 output enable: 0: VO3_DATA6 is output 1: VO3_DATA6 is input	0
1	VO3_GPIO_OUT_6	R/W	VO3_DATA6 output value as GPIO output	0
0	VO3_GPIO_IN_6	R	VO3_DATA6 input value as GPIO input	0

0X90: VO_CLK_GPIO CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	DEFAULT
7	VO3_CLK_GPIO_OUT_SEL	R/W	VO3_CLK output select: 0: VO3_CLK data source is video engine 1:VO3_CLK data source is VO3_CLK_GPIO_OUT(0x90[5])	0
6	VO3_CLK_GPIO_OUT_EN	R/W	VO3_CLK output enable: 0: VO3_CLK is output 1: VO3_CLK is input	0
5	VO3_CLK_GPIO_OUT	R/W	VO3_CLK output value as GPIO output	0
4	VO3_CLK_GPIO_IN	R	VO3_CLK input value as GPIO input	0
3	VO2_CLK_GPIO_OUT_SEL	R/W	VO2_CLK output select: 0: VO2_CLK data source is video engine 1:VO2_CLK data source is VO2_CLK_GPIO_OUT(0x90[1])	0
2	VO2_CLK_GPIO_OUT_EN	R/W	VO2_CLK output enable: 0: VO2_CLK is output 1: VO2_CLK is input	0
1	VO2_CLK_GPIO_OUT	R/W	VO2_CLK output value as GPIO output	0
0	VO2_CLK_GPIO_IN	R	VO2_CLK input value as GPIO input	0

Application Guide

1: System Design Consideration

The TW2826 requires that the system clock source synchronize with the video decoder chips. We suggest using one 27 MHz oscillator to provide clocks for both video decoders (TW2868/TW2866/TW2864, etc.) and TW2826.

Please check the reference design for details (27MHz oscillator is X1).

2: Reset and Clock

The TW2826 has one hardware reset pin: HW_RSTN (active low). It can be controlled by HOST CPU/MPUS's GPIO signal.

We recommend below hardware reset routine:

1. MPU assert hardware reset GPIO signal and release.
2. Wait about 3ms.
3. MPU read TW2826 register 0x47(revision register), if return value is "0x00", exit this reset routine, else repeat Steps 1-3.

Meanwhile, the TW2826 provide a software reset mechanism, the HOST can write 0x20[7] to "1" to perform a software reset. Please note that the software reset will NOT reset PLLs and HOST registers, it will only reset all the video engine logic and internal state machines, also the TW2826 has software reset counter to make sure the reset will be stable, it count about 1ms, so please give 1ms delay after software reset before writing other registers.

There are two PLLs inside TW2826, using the same reference 27MHz clock (XTI), generate 108MHz core clock and 166MHz/133MHz memory clocks separately. All the input data VI_DATA and Serial Bus data SDAT will be captured by their/its corresponding data clock VI_CLK/SCLK, and then synchronized to the 108MHz core clock. The whole chip is running at 108MHz core clock except memory controller, which is running at 133MHz/166MHz.

All the PLLs only can be reset by hardware reset, and have about 1ms stabilization time.

3: Strap Pins

TW2826 has 7 strap pins:

TABLE 5. TW2826 STRAP PINS

PIN NAME	STRAPPING NAME	STRAPPING MEANING	DEFAULT	REGISTER
VI3_DATA0	AUTO_MODE	1 = auto run mode, video engine will automatically start after power up 0 = manual run mode, have to write 0x20[0] to "1" to start the video engine	0	0x25[0] AUTO_MODE_R
VI3_DATA1	VIDEO_MODE	1 = PAL 0 = NTSC	0	0x25[1] V_MODE_R

PIN NAME	STRAPPING NAME	STRAPPING MEANING	DEFAULT	REGISTER
VI3_DATA2	D1_MODE	1 = d1 mode (for intersil internal test/debug only) 0 = normal operation mode	0	0x25[2] D1_MODE_R
VI3_DATA3	VO_MODE	1 = video engine is field mode 0 = video engine is frame mode	0	0x25[3] VO_MODE_R
VI3_DATA4	MEM_SPEED	1 = memory speed is 133mhz 0 = memory speed is 166mhz	0	0x25[4] SPEED_MODE_R
VI3_DATA5	MEM_SIZE	1 = memory size is 128Mb 0 = memory size is 64Mb	0	0x25[5] MEM_SZ_R
VI3_DATA6	SADD	1 = tw2826 device ID is 0x2D 0 = tw2826 device ID is 0x2C	0	0x25[6] SADD_R

When TW2826 powers up, it will latch VI3_DATA0 to VI3_DATA6 strapping data into register 0x25, then configure the chip based on this information. 0x25 register is read only and cannot be changed by HOST.

VO_MODE_R value will be directly passed to 0x21[2] MODE_FRAME (the value will be inverted); the host can write MODE_FRAME to make modifications. All other trapping values are not directly passed to other registers.

4: Configuration Sequence

The TW2826 is very flexible in order for customers to configure/re-configure by reading/writing HOST registers through the Serial Bus interface. We suggest to stop video engine, do a software reset, do the registers read/write operation, and then re-start the video engine, and the new configuration will take effect.

Please follow below sequence to perform a HOST configuration:

1. Stop the video engine by write 0x20[1] to “1”, then read back 0x20, the bit0 indicate the engine running status (0 = stop).

2. Do a software reset by writing 0x20[7] to “1”.

3. Delay 1ms, then check 0x47(revision register), if it return “0xff” means reset is not done, wait more time and check again, till get “0x00” value.

4. Configure all the HOST registers you are willing to control/change.

5. Start the video engine by writing 0x20[0] to 1, the read back 0x20, the bit0 should be “1” (means video engine is running).

5: Channel ID

TW2826 only accepts and generates channel ID built inside the fourth sync word:

In Figure 7, the 4th sync word “XY”, the LSB are channel ID.

On video input port0 and port2 (VI0 and VI2), the tw2826 will check 4th sync word "XY" LSB all 4bits (can accept channel ID 0~3)

4'h0 = channel 0

4'h1 = channel 1

4'h2 = channel 2

4'h3 = channel 3

On video input port1 and port3 (VI1 and VI3), the tw2826 will only check 4th sync word "XY" LSB 2bits (can accept channel ID 0~15)

2'h0 = channel 0

2'h1 = channel 1

2'h2 = channel 2

2'h3 = channel 3

Please note: customers should not put more than two channels with same two LSB (bit0 and bit1) into VI input port1 and port3. For example: for channel 0(CHID=4b'0000) and channel 4(CHID=4'b0100), their channel ID's last two bits are all 2'b00, which will result in channel ID confliction.

We highly recommend that the customer put channel 0~3 into VI port0 and port2, and put channel 4~7 into VI port1 and port3.

On video output side: the VO clock is 27MHz, the tw2826 will only use channel ID 0; when VO clock is 54MHz, the TW2826 will use channel ID 0/1; when VO clock is 108MHz, the tw2826 will generate channel ID 0/1/2/3

4'h0 = channel 0

4'h1 = channel 1

4'h2 = channel 2

4'h3 = channel 3

Please note, to avoid channel ID confliction, even directly bypassing one channel video from input port, the channel ID will be replaced with new channel ID (can't carry/bypass the old channel ID).

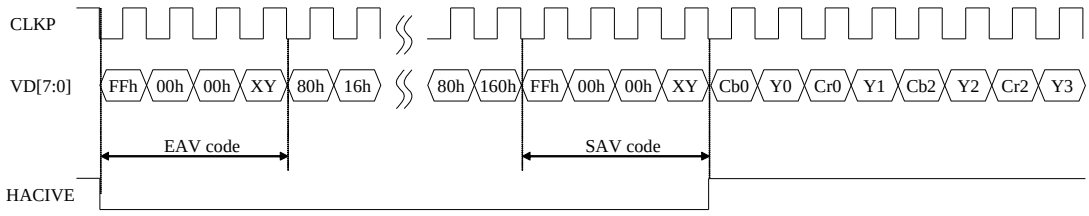


FIGURE 7. TIMING DIAGRAM OF ITU-R BT.656 FORMAT

6: Video Input Configuration

The TW2826 has four physical video input ports: VI0, VI1, VI2, and VI3. They are all running independently. We assume they are all 108MHz 4-channel byte interleave BT656 video.

The TW2826 provides video input data latching option for each port: 0x22[7:4] (VIN_CFG [3:0]). Video input data can be latched in by related video clock with either positive edge or negative edge.

Configuration Example: port0 and port2 are latched with posedge, and port1 and port3 are latched with negedge

VIN_CFG [3:0] =4'b1010

7: Video Multiplex Engine Configuration

The TW2826 video multiplex engine has two operation modes: field mode and frame mode.

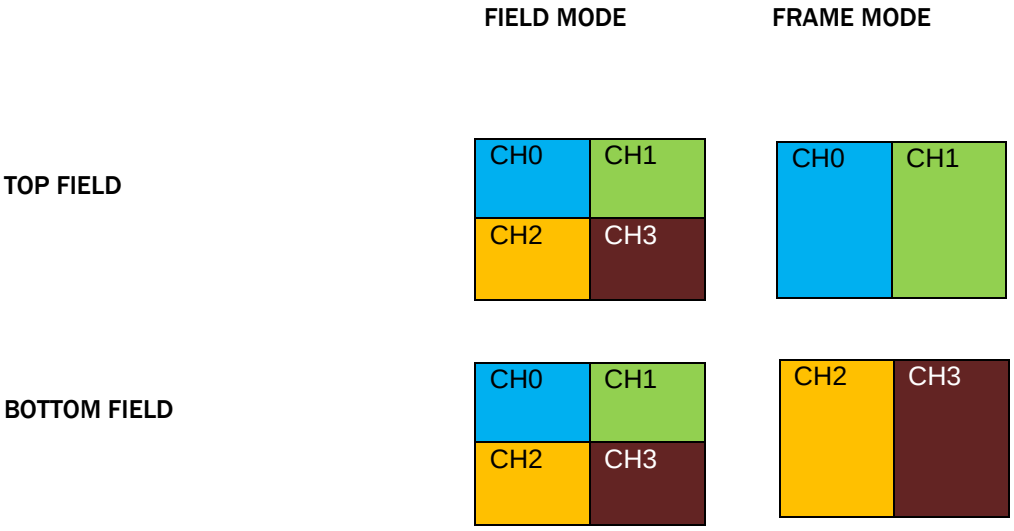


FIGURE 8. VIDEO MULTIPLEX/OUTPUT MODE

FIELD mode: video multiplex engine pick each channel D1 video's odd lines (drop even lines) and do the horizontal two to one fix ratio down-sample to generate each CIF video data, operation apply on input video's both top field and bottom field, then multiplex all four channels CIF video into one D1 video. The display order is fixed and comes from the same physical video input port, where:

Top left CIF: channel 0

Top right CIF: channel 1

Bottom left CIF: channel 2

Bottom right CIF: channel 3

FRAME mode: video multiplex engine only pick one field input video data (drop another field data), then do the horizontal two to one fix ratio down-sample on this selected field. The multiplexer puts channel 0 and channel 1 into the top field, and puts channel 2 and channel 3 into the bottom field. The display order is fixed and comes from the same physical video input port too, where:

Top filed left CIF: channel 0

Top field right CIF: channel 1

Bottom field left CIF: channel 2

Bottom field right CIF: channel 3

Please note:

1. This multiplex mode applies to all four ports/engines and cannot be mixed at the same time.

2. Video output mode must be the same as video multiplex mode, can't multiplex video with frame mode but output in field mode format, can't multiplex video with field mode but output in frame mode either.

3. The video input must be all 108 MHz.

4. All four channels video data(ch0-ch3) comes from same physical video input port; different video input port's video data cannot be multiplexed into one Quad CIF D1 video.

5. The Quad CIF position is fixed based on the input channel ID.

6. Video multiplex mode and field selection configuration table:

TABLE 6. VIDEO MULTIPLEX/OUTPUT MODE AND FIELD SELECTION

0X21[2]=FRAME_MODE	0X21[3]=FRAME_TOP	0X24[4]=TOP_SEL_SET_ON	MODE	FIELD SELECTED
0	x	x	FIELD MODE	Both top and bottom
1	1	x	FRAME MODE	Top only
1	0	1	FRAME MODE	Base on 0x26,0x27 define
1	0	0	FRAME MODE	Randomly select top/bottom field (optimize for less DRAM bandwidth usage)

8: Video Input Position Adjustment

The nature video camera output has a black zone (non-active area) on both the left and right side; this will result in the TW2826 Quad-CIF output, as shown in Figure 9:

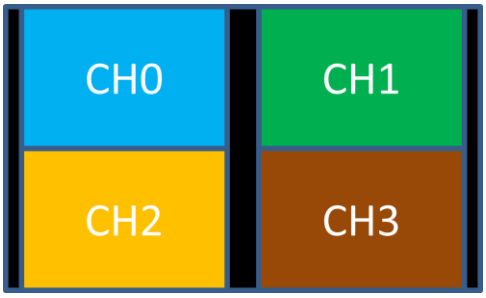


FIGURE 9. NATURE TW2826 QUAD-CIF OUTPUT

Since the video encode engine is macro-block (16x16) based, we suggest to adjust the front-end video decoder's register, move CH0/CH2 active area to the left (for TW2868: adjust register 0x0A/0x2A), and move CH1/CH3 active area to the right (for tw2868: adjust register 0x1B/0x3B). This will leave pixel 352 ~ 367 to black (Figure 10) instead of a black zone on both/one side.

Also please configure the video encode engine as follows:

Encoding start point for CH0/CH2:0

Encoding end point for CH0/CH2:351

Encoding start point for CH1/CH3:368

Encoding end point for CH1/CH3:719

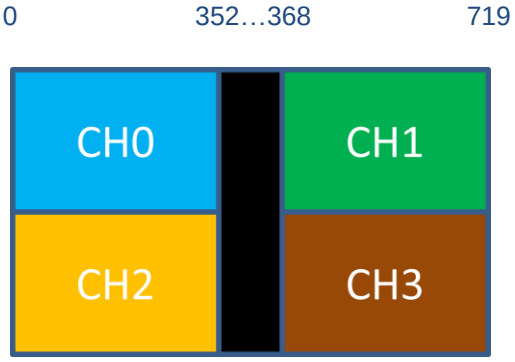


FIGURE 10. ADJUSTED TW2826 QUAD-CIF OUTPUT

Please note, this can apply on both operation modes (see "Application Guide 7: Video Multiplex Engine Configuration" on page 39):

FIELD MODE and FRAME MODE

9: Video Output Formatter/Aggregator Configuration

There are four physical video output ports: VO0, VO1, VO2 and VO3. Each one can be configured as:

1. 27MHz single channel with channel ID0

2. 54MHz 2-channel byte interleave with channel ID 0/1

3. 108MHz 4-channel byte interleave with channel ID 0/1/2/3

The regarding video output clock can be configured 0, 45, 90, 135, 180, 225, 270, 315 degrees delay to the corresponding video output data. Please refer to register 0x30-0x33.

Each video output port can aggregate up to four channel D1 video data into byte interleave format, the video source can be any 16 channel video input, or any 4 Quad CIF multiplexed D1 data. Please refer to register 0x34-0x43.

If for some reason, the customer wants to disable the video output port, you can set 0x34~0x37(vo0), 0x38~0x3b(vo1), 0x3c~0x3f(vo2) or 0x40~0x43(vo3) register's bit[5:4] to 2'b00. This will force the regarding video output port 0/1/2/3 data to 0x00 (please note that the regarding video port output clock is still running).

The default setting is:
VO0:VI0 Quad CIF,27MHz 180 degrees delay
VO1:VI1 Quad CIF,27MHz 180 degrees delay
VO2:VI2 Quad CIF,27MHz 180 degrees delay
VO3:VI3 Quad CIF, 27MHz 180 degrees delay

Configuration Example:
VO0, 108MHz, channel0=VI0 Quad CIF, channel1=VI1 Quad CIF, channel2=VI2 Quad CIF, channel3=VI3 Quad CIF:
0x30[4:0] =VO_CLK_CFG_0[4:0]=5'b1_0100
0x34[7:0]=VO_CFG_0_CH0[7:0]=8'b0010_0000
0x35[7:0]=VO_CFG_0_CH1[7:0]=8'b0010_0001
0x36[7:0]=VO_CFG_0_CH2[7:0]=8'b0010_0010
0x37[7:0]=VO_CFG_0_CH3[7:0]=8'b0010_0011

VO1, 108MHz,channel0=VI1 Quad CIF,channel1=VI2 CH1,channel2=VI3 CH2,channel3=VI0 CH1:
0x31[4:0]=VO_CLK_CFG_0[4:0]=5'b1_0100
0x38[7:0]=VO_CFG_1_CH0[7:0]=8'b0010_0001
0x38[7:0]=VO_CFG_1_CH1[7:0]=8'b0011_1001
0x3a[7:0]=VO_CFG_1_CH2[7:0]=8'b0011_1110
0x3b[7:0]=VO_CFG_1_CH3[7:0]=8'b0011_0001

VO2,54MHz,channel0=VI3 Quad CIF,channel1=VI1 CH2
0x32[4:0]=VO_CLK_CFG_0[4:0]=5'b0_1100
0x3c[7:0]=VO_CFG_2_CH0[7:0]=8'b0010_0011
0x3d[7:0]=VO_CFG_2_CH1[7:0]=8'b0011_0110
0x3e[7:0]=VO_CFG_2_CH2[7:0]=8'b0000_0000
0x3f[7:0]=VO_CFG_2_CH3[7:0]=8'b0000_0000

VO3,27MHz,channel0=VI2 Quad CIF
0x33[4:0]=VO_CLK_CFG_0[4:0]=5'b0_0100
0x40[7:0]=VO_CFG_3_CH0[7:0]=8'b0010_0010
0x41[7:0]=VO_CFG_3_CH1[7:0]= 8'b0000_0000
0x42[7:0]=VO_CFG_3_CH2[7:0]=8'b0000_0000
0x43[7:0]=VO_CFG_3_CH3[7:0]=8'b0000_0000

10: GPIO Configuration

Video output port 2 and 3:VO2,VO3 can be configured as GPIO pins, this will provide up to 18 GPIO pins, each one can be configured either input or output, please refer to register 0x88-0x90.

Configuration Example:
VO2 as normal video output port
VO3 as GPIO ports:
VO3_DATA0 to VO3_DATA3 gpio input,
VO3_DATA4 gpio output value “1”
VO3_DATA5 gpio output value “0”,
VO3_DATA6 gpio output value “0”,
VO3_DATA7 gpio output value “1”,
VO3_CLK gpio input:

0x88-0x8b=8’b0000_0000
0x8c=VO3_GPIO_CTRL0[7:0]=8’b0100_0100
0x8d=VO3_GPIO_CTRL1[7:0]=8’b0100_0100
0x8e=VO3_GPIO_CTRL2[7:0]=8’b1000_1010
0x8f=VO3_GPIO_CTRL3[7:0]=8’b1010_1000
0x90=VO3_CLK_GPIO_CTRL[7:0]=8’b0100_0000

Electrical Information

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DVDD18 (Measured to DVSS18)	VDD18	-0.5		2.3	V
DVDD33 (Measured to DVSS33)	VDD33	-0.5		4.5	V
Digital Input/Output Voltage	-	–0.5		4.5	V
Storage Temperature	T_S	–65		150	°C
Junction Temperature	T_J	0		125	°C
Reflow Soldering (10-30 Seconds)	T_{PEAK}			255-260	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DVDD18 (Measured to DVSS18)	VDD18	1.62	1.8	1.98	V
DVDD33 (Measured to DVSS33)	VDD33	3.0	3.3	3.6	V
Ambient Operating Temperature	T_A	-40	25	85	°C

DC Electrical Parameters

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0		5.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input Leakage Current @ 3.3V	I_{LH}	-100		-10	µA
Input Leakage Current @ 0V	I_{LL}	10		100	µA
Input Capacitance	C_{IN}		6		pF
DIGITAL OUTPUTS					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current (@ V_{OH} = 2.4V)	I_{OH}	7.6		59.5	mA
Low Level Output Current (@ V_{OL} = 0.4V)	I_{OL}	5.7		34.8	mA
Tri-state Output Leakage Current @ 3.3V	I_{OZ}			10	uA

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
Tri-state Output Leakage Current @0.0V	I_{OZ}	-100			µA
Output Capacitance	C_O		6		pF
SUPPLY CURRENT					
PLL Supply Current	I_{DDPLL}		8		mA
Digital Core Supply Current (DVDD18,1.8V)	I_{DDI}		100		mA
Digital I/O Supply Current (DVDD33, 3.3V)	I_{DDO}		30		mA
Total Power Dissipation	P		300		mW

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Parameters

VI_CLK and VI_DATA Timing

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Setup Time VI_ DATA to VI_CLK	1	0.44		0.5	Ns
Hold Time from VI_CLK to VI_ DATA	2	1.6		2.94	Ns

NOTES:

1. VI_CLK represents VI0_CLK,VI1_CLK,VI2_CLK,VI3_CLK, and VI_DATA represents the corresponding VI0_DATA[0:7],VI2_DATA[0:7],VI3_DATA[0:7] and VI3_DATA[0:7].
2. The TW2826 has option to latch VI data using both positive and negative edge; please refer to register 0x22[7:4] and "Application Guide 6: Video Input Configuration" on page 39. In Figure 11, we only characterize rising edge case.
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

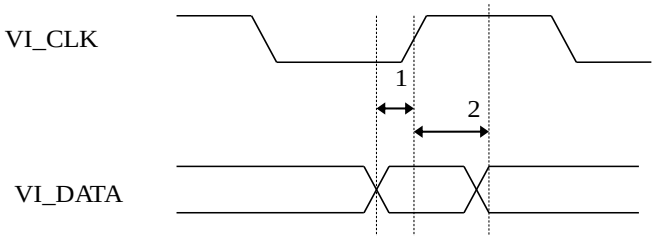


FIGURE 11. VI_CLK AND VI_DATA TIMING

VO_CLK and VO_DATA Timing

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Delay from VO_ DATA to VO_CLK Falling Edge	1	0.7		1.8	Ns

NOTES:

1. VO_CLK represents VO0_CLK,VO1_CLK,VO2_CLK,VO3_CLK, and VO_DATA represents the corresponding VO0_DATA[0:7],VO2_DATA[0:7],VO3_DATA[0:7] and VO3_DATA[0:7].
2. The VO_CLK in Figure 12 is configured as 180 degrees delay to the related VO_DATA.
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

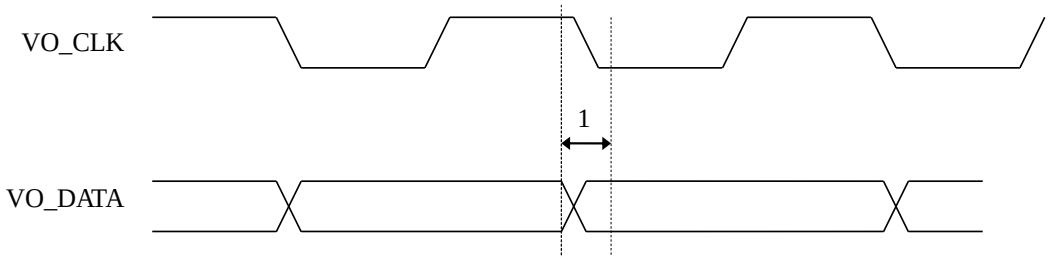


FIGURE 12. VO_CLK AND VO_DATA TIMING

SDR_CLK and SDR_CTRL Timing

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
Delay from SDR_CLK to SDR_CTRL (166MHz)	1(min)/ 2(max)	1.8		3.2	Ns
Delay from SDR_CLK to SDR_CTRL (133MHz)	1(min)/ 2(max)	1.0		2.1	Ns

NOTES:

1. SDR_CTRL represents: SDR_RASB,SDR_CASB,SDR_WEB,SDR_BA0,SDR_BA1,SDR_MA[0:11]
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

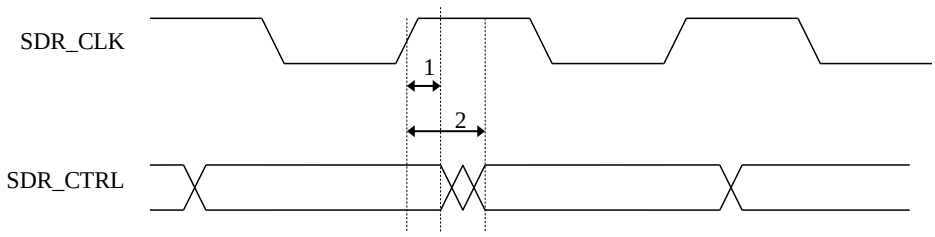


FIGURE 13. SDR_CLK AND SDR_CTRL TIMING

Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
Bus Free Time between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	100			ns
SDAT Hold Time	t_{hSDAT}	50			ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load For Each Bus Line	C_{BUS}			400	pF
LOW Period of SCL	t_{LOW}	0.5			µs
HIGH Period of SCL	t_{HIGH}	0.5			µs
SCLK Clock Frequency	f_{SCLK}			400	kHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

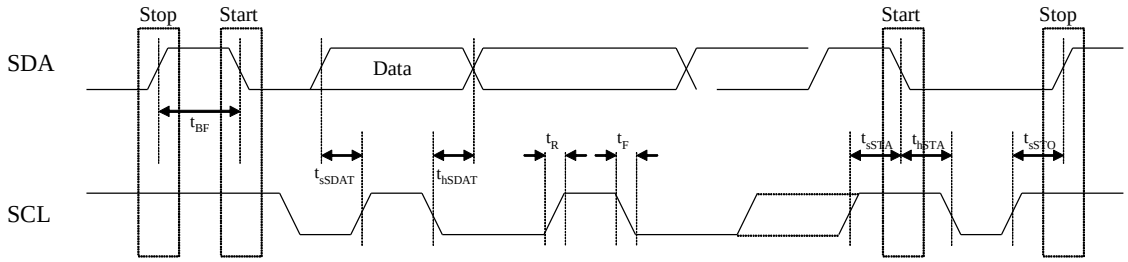
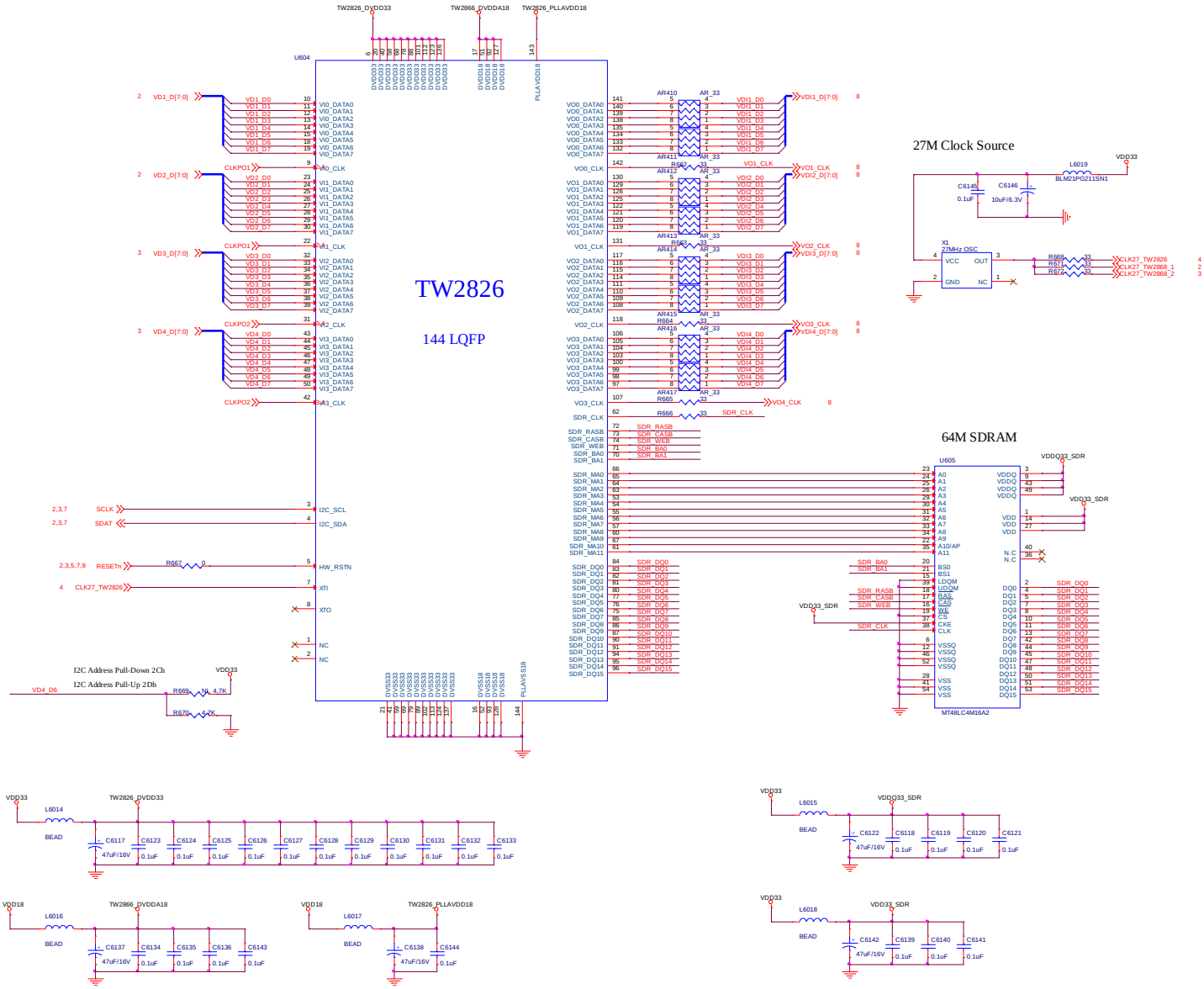


FIGURE 14. SERIAL HOST INTERFACE TIMING

Application Schematic

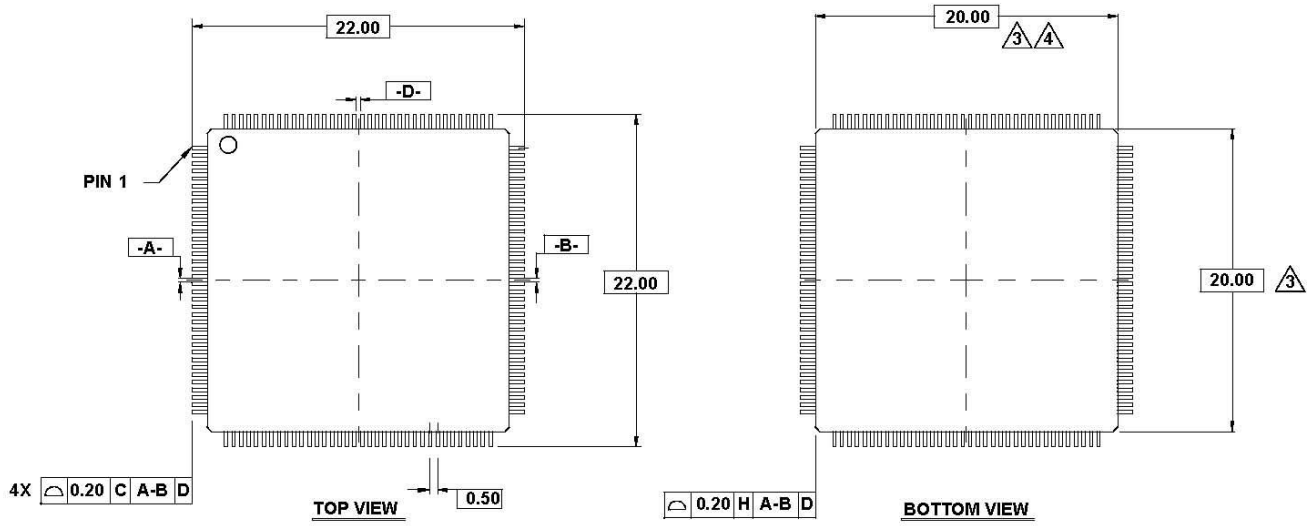


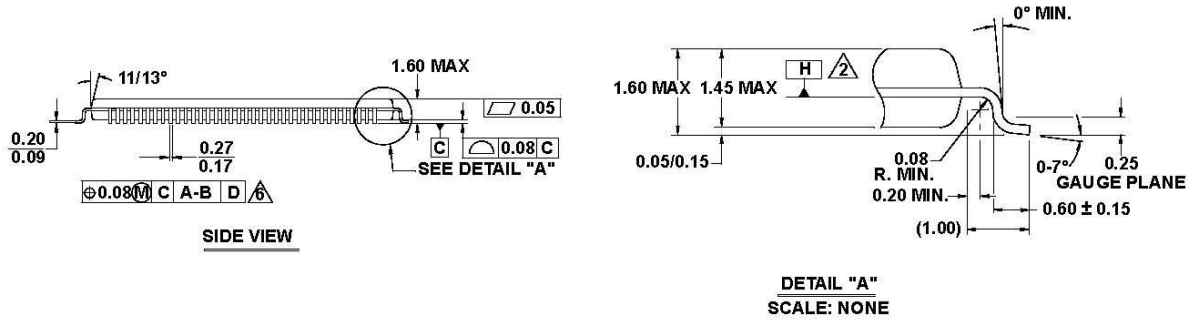
Package Outline Drawing

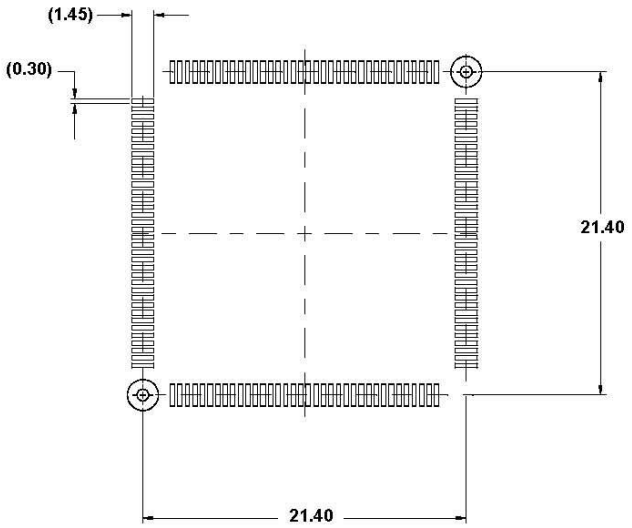
Q144.20x20

144 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE (LQFP)

Rev 3, 8/11







TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.25mm per side.
4. These dimensions to be determined at datum plane H.
5. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
6. Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
7. Controlling dimension: millimeter.
8. This outline conforms to JEDEC publication 95 registration MS-026, variation BFB.
9. Dimensions in ( ) are for reference only.

Datasheet Revision History

DATE	REVISION	CHANGE
9/6/2011	FN7913.0	Initial release

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