ISL91133

High Efficiency 2.3A Boost Regulator with Input-to-Output Bypass

FN8680
Rev 1.00
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The ISL91133 is an integrated boost switching regulator for battery powered applications. The device provides a power supply solution for products using a one cell Li-ion or Li-polymer battery.

The device is capable of delivering up to 2.3A output current from V_{IN} = 2.5V and V_{OUT} = 3.3V. The no load quiescent current is only 108µA in Boost mode and 45µA in Forced Bypass mode, which significantly reduces the standby consumption.

The ISL91133 offers a Bypass mode operation where the output is directly connected to the input through a 38mΩ MOSFET to allow a significantly lower dropout voltage. The Bypass mode can be entered by an external command, or by auto bypass. The Forced Bypass mode allows the output voltage to operate close to the input voltage and improves the efficiency under these conditions.

The ISL91133 is designed to support 6 fixed output voltages ranging from 3.15V to 5V. A voltage select pin is available for each output variant to scale up the output voltage by a small offset to compensate the load transient droop.

The ISL91133 requires only an inductor and a few external components to operate. The 2.5MHz switching frequency further reduces the size of external components.

The ISL91133 is available in a 16 bump, 0.4mm pitch, 1.78mmx1.78mm WLCSP.

Related Literature

For a full list of related documents, visit our website

- ISL91133 product page

Features

- Input voltage range: 2.35V to 5.4V
- Output current: up to 2.3A (V_{IN} = 2.5V, V_{OUT} = 3.3V)
- Burst current up to 2.5A (V_{IN} = 2.5V, V_{OUT} = 3.3V, t_{ON} < 600µs, T = 4.6ms)
- High efficiency: up to 96%
- 108µA quiescent current minimizes standby consumption in Boost mode, 45µA in Forced Bypass mode
- 2.5MHz switching frequency minimizes external component size
- Forced Bypass or Auto Bypass modes with a 38mΩ switch
- PFM mode at light load currents
- Fully protected for overcurrent, over-temperature, and undervoltage
- Load disconnect when disabled
- Small 1.78mmx1.78mm WLCSP

Applications

- Smartphones and tablet PCs
- Wireless communication devices
- 2G/3G/4G RF power amplifiers
- USB OTG power source

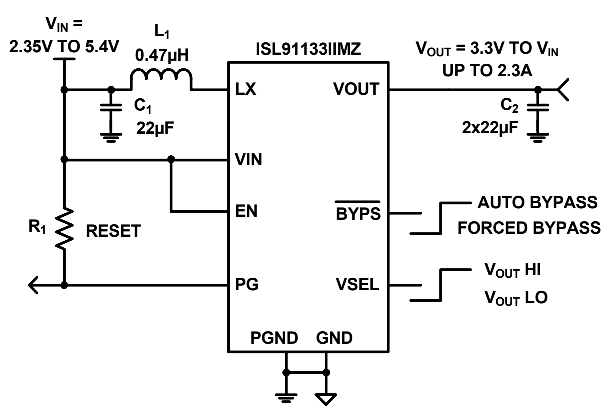


FIGURE 1. TYPICAL APPLICATION

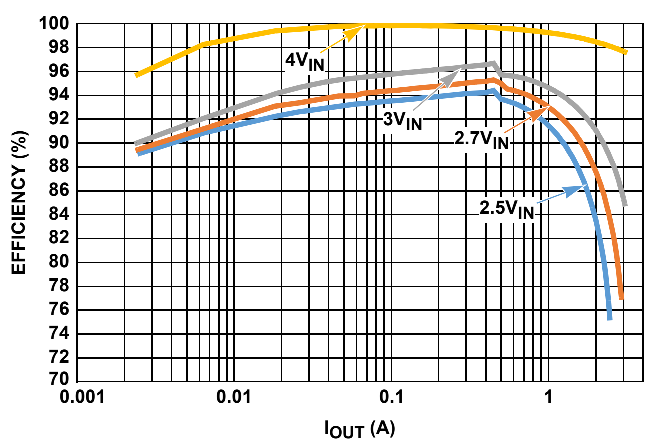


FIGURE 2. EFFICIENCY vs LOAD CURRENT, V_{OUT} = 3.3V

Block Diagram

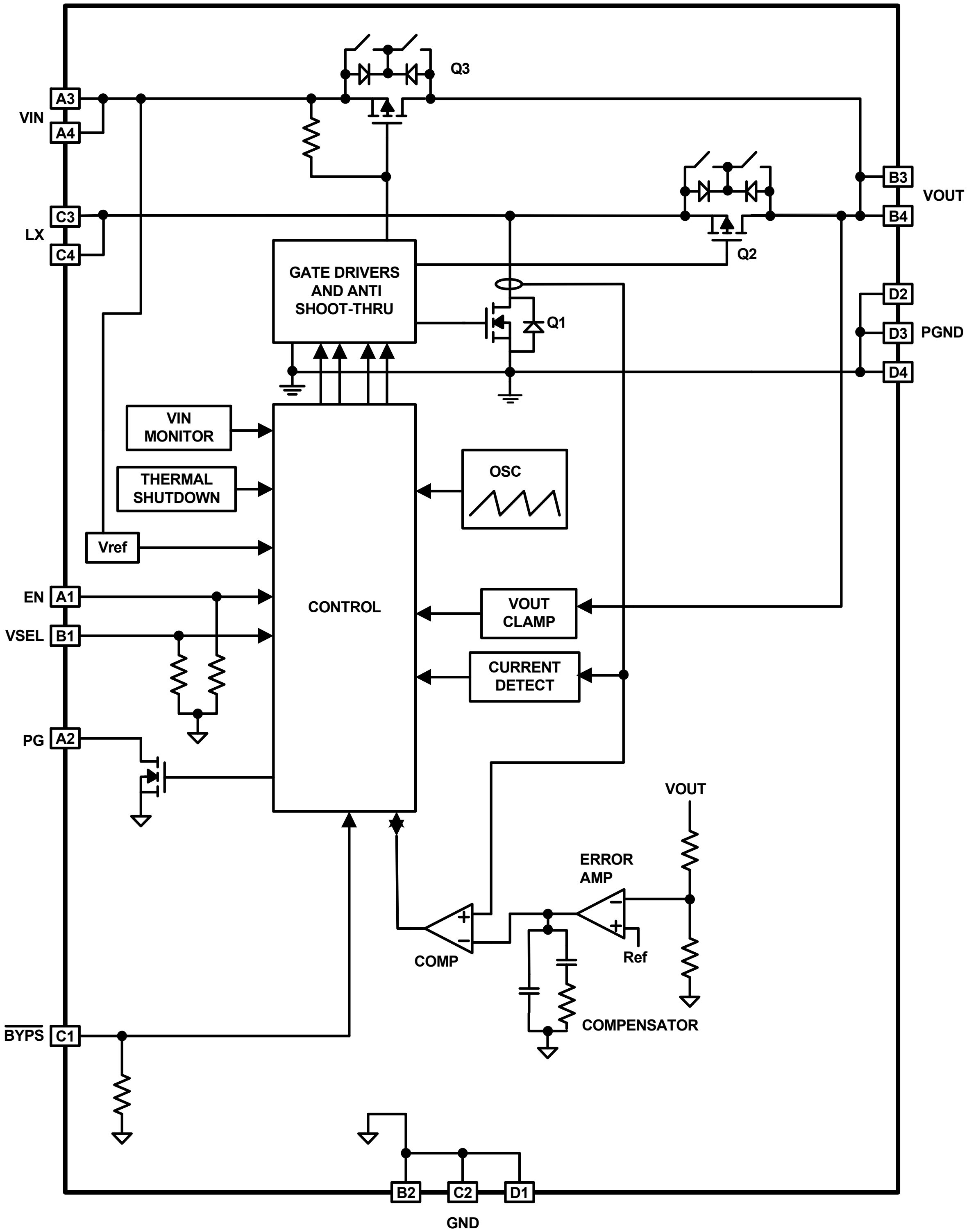
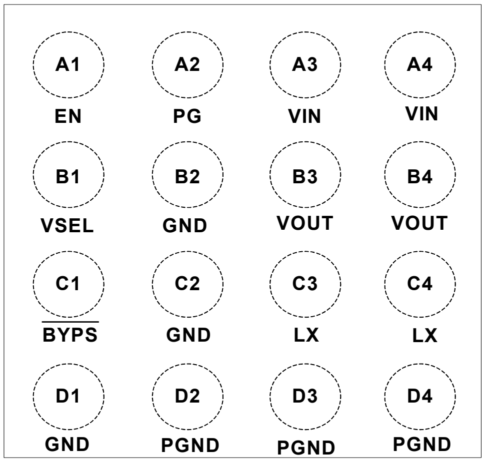


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

16 BALL WLCSP
TOP VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
B3, B4	VOUT	Boost output; connect a 2x22µF capacitor to PGND.
C3, C4	LX	Inductor connection
D2, D3, D4	PGND	Power ground for high switching current.
A3, A4	VIN	Power input; Range: 2.35V to 5.4V. Connect a 22µF capacitor to PGND.
B1	VSEL	Output selection between LO and HI. While operating at boost mode, pull this pin HI to select the high output level. To select the low output level, pull this pin to LO.
A2	PG	Open-drain output; provides output power-good status.
A1	EN	Logic input; drive HIGH to enable device.
C1	$\overline{BYPS}$	Force bypass input; Pull this pin LO to activate forced bypass mode, where both Q2 and Q3 are turned on, the rest of the IC is disabled. When this pin is HI, auto bypass mode is activated.
B2, C2, D1	GND	Analog ground pin

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	V_{OUT} (V)	TEMP RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE TAPE AND REEL (RoHS Compliant)	PKG. DWG. #
ISL91133IILZ-T	133L	3.15/3.3	-40 to +85	3k	16 Ball WLCSP	W4x4.16E
ISL91133IIMZ-T	133M	3.3/3.5	-40 to +85	3k	16 Ball WLCSP	W4x4.16E
ISL91133IINZ-T	133N	3.5/3.7	-40 to +85	3k	16 Ball WLCSP	W4x4.16E
ISL91133IIOZ-T	133O	3.7/3.77	-40 to +85	3k	16 Ball WLCSP	W4x4.16E
ISL91133IIPZ-T	133P	4.5/4.76	-40 to +85	3k	16 Ball WLCSP	W4x4.16E
ISL91133IIQZ-T	133Q	5.0/5.2	-40 to +85	3k	16 Ball WLCSP	W4x4.16E
ISL91133IIL-EVZ	Evaluation Board for ISL91133IILZ					
ISL91133IIM-EVZ	Evaluation Board for ISL91133IIMZ					
ISL91133IIN-EVZ	Evaluation Board for ISL91133IINZ					
ISL91133IIO-EVZ	Evaluation Board for ISL91133IIOZ					
ISL91133IIP-EVZ	Evaluation Board for ISL91133IIPZ					
ISL91133IIQ-EVZ	Evaluation Board for ISL91133IIQZ					

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL91133 product information page. For more information about MSL, see TB363.

Absolute Maximum Ratings

VIN . . . . -0.3V to 6.5V
LX . . . . -0.3V to 6.5V
GND, PGND . . . . -0.3V to 0.3V
All Other Pins . . . . -0.3V to 6.5V
ESD Rating
  Human Body Model (Tested per JESD22-A114F). 3kV
  Machine Model (Tested per JESD22-A115-C) 225V
  Charge Device Model (Tested per JESD22-C101F). 2kV
Latch-up (Tested per JESD-78D; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
16 Ball WLCSP Package (Notes 4, 5)	70	14

Maximum Junction Temperature . . . . +125°C
Storage Temperature Range. . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . .-40°C to +85°C
Supply Voltage Range (Boost Only) . . . . 2.35V to 5.5V
Max Load Current (V_{IN} = 2.5V, V_{OUT} = 3.3V). .2.3A DC
Max Load Current (V_{IN} = 2.5V, V_{OUT} = 3.3V, t_{ON} = 600µs, T = 4.6ms). .2.5A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JB}, the board temp is taken on the board near the edge of the package, on a trace at the middle of one side. See TB379.

Electrical Specifications

V_{IN} = V_{EN} = 3V, L_1 = 0.47µH, C_1 = C_2 = 22µF, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
POWER SUPPLY						
Input Voltage Range	V_{IN}		**2.35**		**5.4**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		2.2	**2.35**	V
		Falling	**1.9**	2.0		V
V_{IN} Supply Current in Boost Mode	I_{VIN_BOOST}	PFM mode, no external load on V_{OUT}		108	**150**	µA
V_{IN} Supply Current in Auto Bypass Mode	I_{VIN_BYP1}	V_{IN} = 4.2V, V_{OUT} < 4.2V		80	**120**	µA
V_{IN} Supply in Forced Bypass Mode	I_{VIN_BYP2}	V_{IN} = 3.5V		45	**70**	µA
V_{IN} Supply Current, Shutdown	I_{SD}	EN = GND, V_{IN} = 3.6V		1.3	**5**	µA
OUTPUT VOLTAGE REGULATION						
Output Voltage Range, Boost Mode	V_{OUT}	I_{OUT} = 100mA	**3.15**		**5.20**	V
Output Voltage Accuracy		V_{IN} = 3.6V	**-2**		**+4**	%
Output Voltage Clamp	V_{CLAMP}	V_{OUT} Rising	**5.4**		**5.7**	V
Output Voltage Clamp Hysteresis	V_{CLAMP_HS}			170		mV
INDUCTOR VALLEY CURRENT LIMIT						
Inductor Valley Current Limit	I_{PK_LMT}	V_{IN} = 2.6V	**3.6**	4	**4.6**	A
During Soft-Start	$I_{PK\_LMT\_SU}$			1.5		A
DC/DC SWITCHING SPECIFICATIONS						
Oscillator Frequency	f_{SW}		**2.1**	2.50	**2.9**	MHz
BOOST ON-RESISTANCE						
P-Channel MOSFET (Q2) ON-Resistance	r_{DSON_P}	V_{IN} = 3.5V, I_O = 200mA		0.04		Ω
N-Channel MOSFET (Q1) ON-Resistance	r_{DSON_N}	V_{IN} = 3.5V, I_O = 200mA		0.045		Ω
PFM/PWM TRANSITION						
Load Current Threshold, PFM to PWM		V_{IN} = 3.0V, V_{OUT} = 3.3V		500		mA
Load Current Threshold, PWM to PFM		V_{IN} = 3.0V, V_{OUT} = 3.3V		300		mA

Electrical Specifications $V_{IN} = V_{EN} = 3V$, $L_1 = 0.47\mu H$, $C_1 = C_2 = 22\mu F$, $T_A = +25°C$. Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
THERMAL SHUTDOWN						
Thermal Warning				120		°C
Thermal Shutdown				150		°C
Thermal Shutdown and Thermal Warning Hysteresis				20		°C
LEAKAGE CURRENT						
VO To VIN Reverse Leakage	I_{LEAK}	$V_{IN} = 3V$, $V_{OUT} = 5V$, EN = 0		0.3	**1.0**	µA
VIN to VOUT Leakage		$V_{IN} = 3V$, $V_{OUT} = 0V$, EN = 0		0.05	**1.0**	µA
LX Pin Leakage Current	$I_{NFETLEAK}$	$V_{LX} = 5V$, EN = 0	**-1**		**1**	µA
SOFT-START						
Level 1 Linear Start-up Current, Fast	I_{LIN1}	ISL91133IILZ, ISL91133IIMZ, ISL91133IINZ, ISL91133IIOZ		1300		mA
Level 1 Linear Start-up Current, Slow		ISL91133IIPZ, ISL91133IIQZ		350		
Level 2 Linear Start-up Current, Fast	I_{LIN2}	ISL91133IILZ, ISL91133IIMZ, ISL91133IINZ, ISL91133IIOZ		2400		mA
Level 1 Linear Start-up Current, Slow		ISL91133IIPZ, ISL91133IIQZ		700		
Soft-Start Time EN Hi to Regulation	t_{SS}	ISL91133IILZ, ISL91133IIMZ, ISL91133IINZ, ISL91133IIOZ, 50Ω load		600		µs
		ISL91133IIPZ, ISL91133IIQZ, 50Ω load		1200		µs
BYPASS MODE						
Bypass P-Channel MOSFET (Q3) ON-Resistance	r_{DSON_BP}	$I_{OUT} = 600mA$, $V_{IN} = 3.5V$		0.038		Ω
Auto Bypass Hysteresis	V_{BYP_Hys}			100		mV
Bypass Mode Current Limit (for ISL91133IIPZ and ISL91133IIQZ only)	V_{OCP_BYP}	$V_{IN} = 5V$, measured by V_{IN}-V_{OUT}		150		mV
LOGIC INPUTS/OUTPUT (PG, EN, VSEL, $\overline{BYPS}$)						
Input Leakage, PG	I_{PG_LEAK}	PG = HIGH		0.05	**1**	µA
Input HIGH Voltage, EN, VSEL, $\overline{BYPS}$	V_{IH}		**1.2**			V
Input LOW Voltage, EN, VSEL, $\overline{BYPS}$	V_{IL}				**0.4**	V
Pull-down Resistance, EN, VSEL, $\overline{BYPS}$	R_{PD}			1.5		MΩ
FAULT Reset Timer	t_{FRST}			20		ms

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for $T_A = +25°C$ and $V_{IN} = 3V$.

Typical Performance Curves

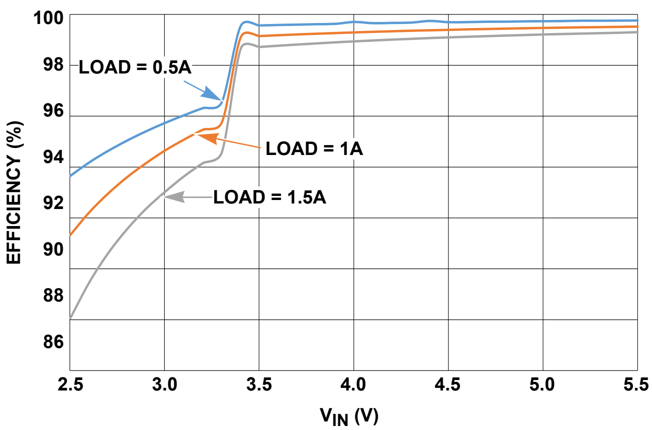


FIGURE 4. EFFICIENCY vs V_{IN}, V_{OUT} = 3.3V

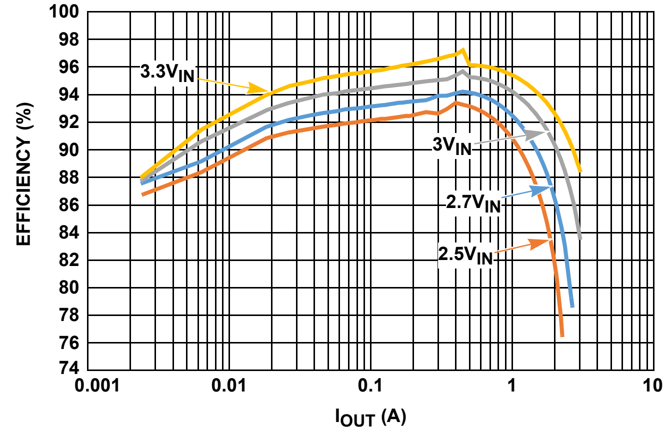


FIGURE 5. EFFICIENCY vs LOAD CURRENT, V_{OUT} = 3.5V

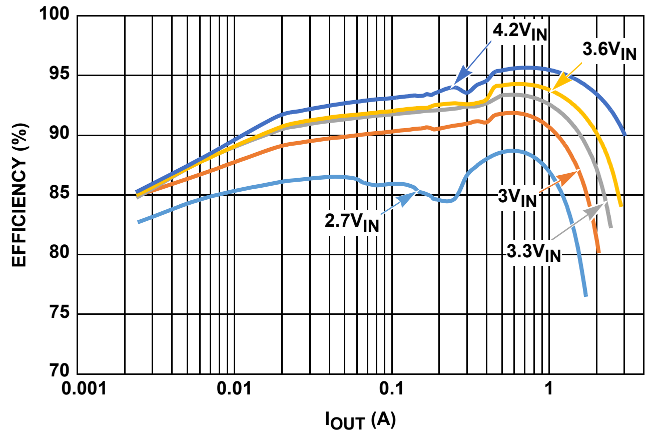


FIGURE 6. EFFICIENCY vs LOAD CURRENT, V_{OUT} = 5V

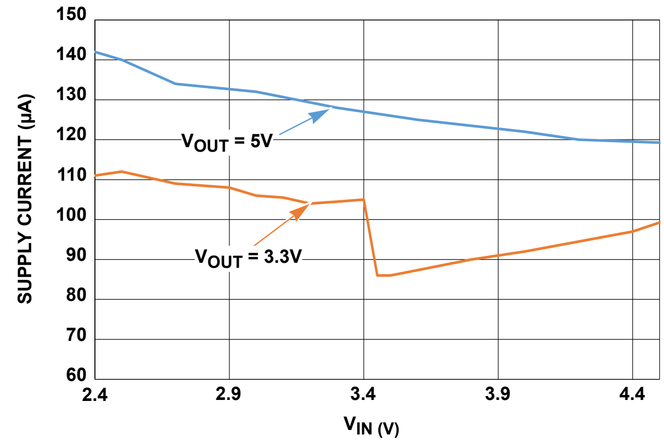


FIGURE 7. SUPPLY CURRENT vs V_{IN}

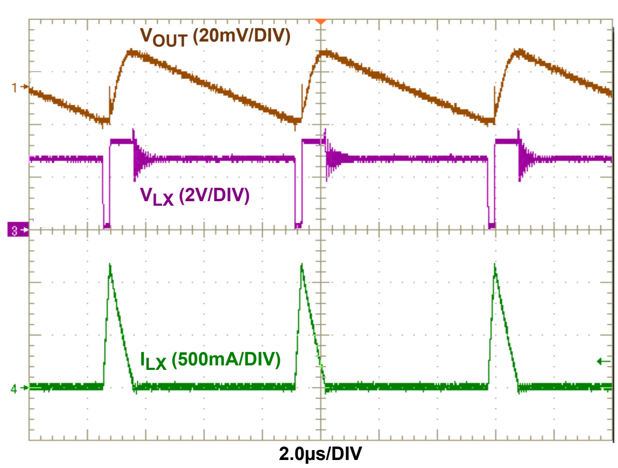


FIGURE 8. SWITCHING WAVEFORM PFM MODE, V_{IN} = 2.7V, I_{LOAD} = 50Ω, V_{OUT} = 3.3V

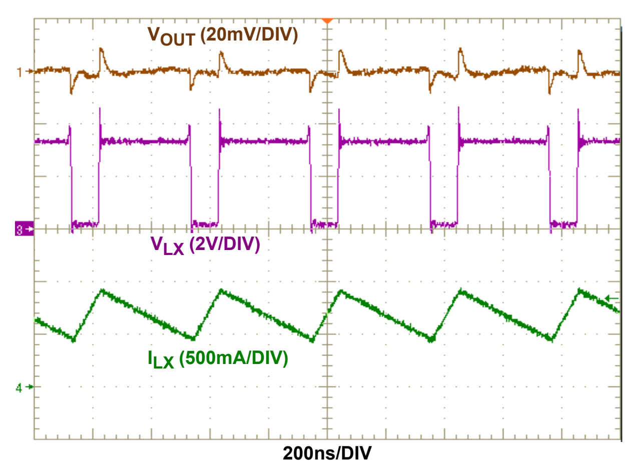


FIGURE 9. SWITCHING WAVEFORM PWM MODE, V_{IN} = 2.7V, I_{OUT} = 500mA, V_{OUT} = 3.3V

Typical Performance Curves (Continued)

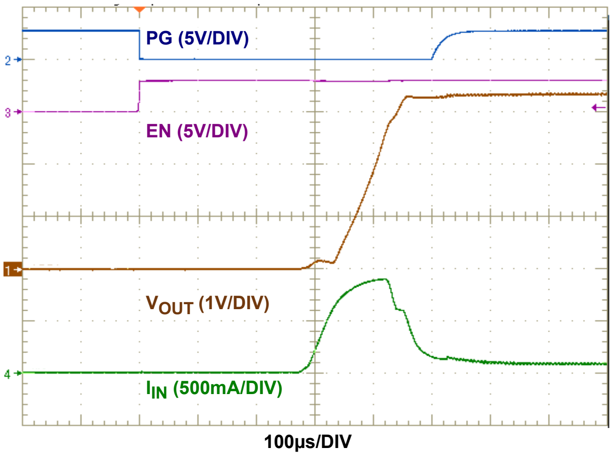


FIGURE 10. START-UP WAVEFORM 50Ω LOAD, V_{IN} = 3V, V_{OUT} = 3.3V

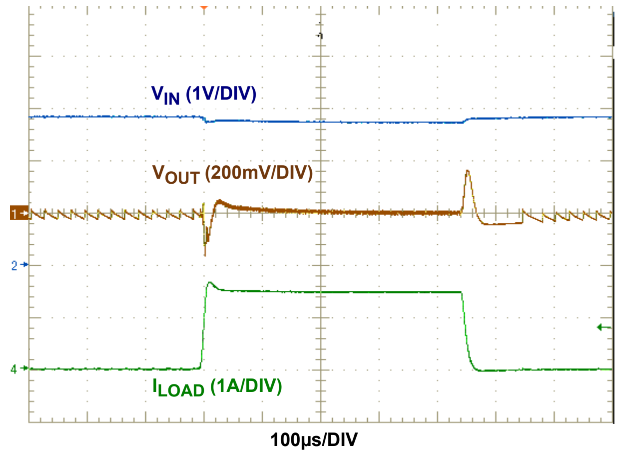


FIGURE 11. LOAD STEP RESPONSE, V_{IN} = 2.7V, I_{LOAD} = 10mA -> 1500mA -> 10mA

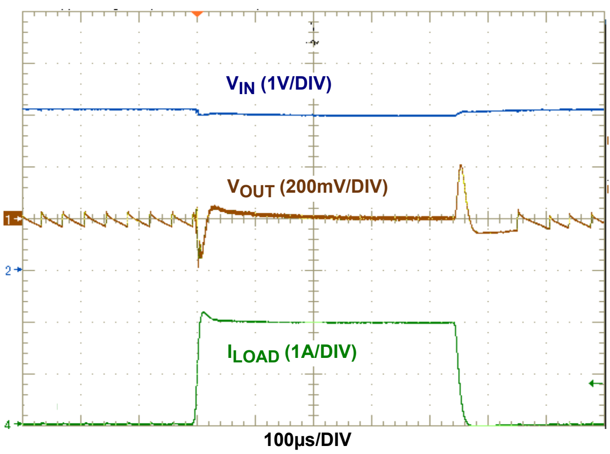


FIGURE 12. LOAD STEP RESPONSE, V_{IN} = 3V, I_{OUT} = 10mA -> 1500mA -> 10mA

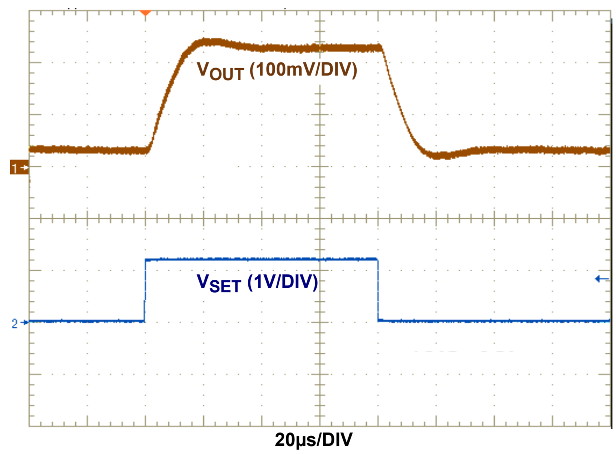


FIGURE 13. V_{SET} TOGGLE RESPONSE, V_{IN} = 3V, V_{OUT} = 3.3V, LOAD = 0.5A

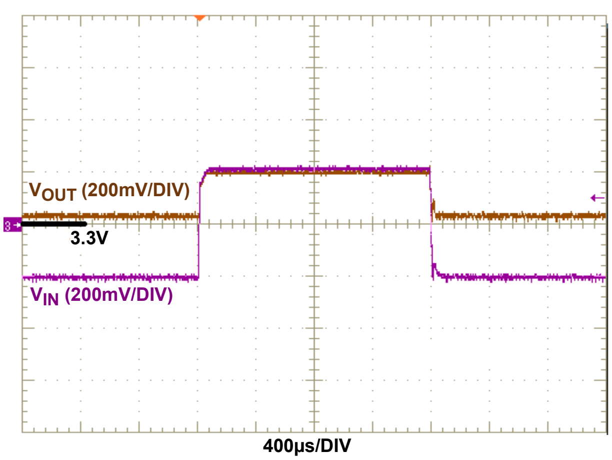


FIGURE 14. V_{SET} TOGGLE RESPONSE, V_{IN} = 3.1V -> 3.5V -> 3.1V LOAD = 1A

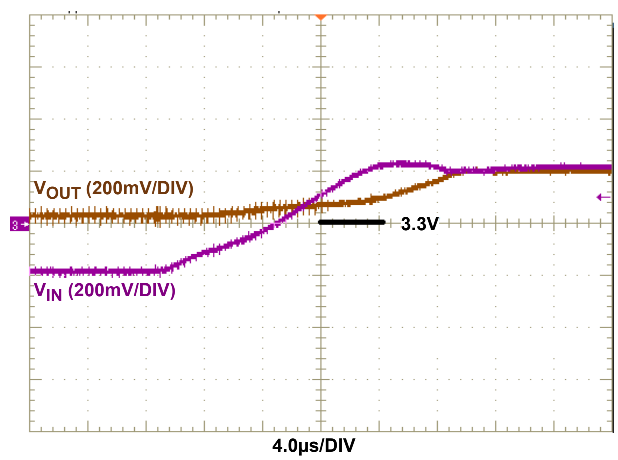


FIGURE 15. V_{SET} TOGGLE RESPONSE, V_{IN} = 3.1V -> 3.5V, LOAD = 1A

Typical Performance Curves (Continued)

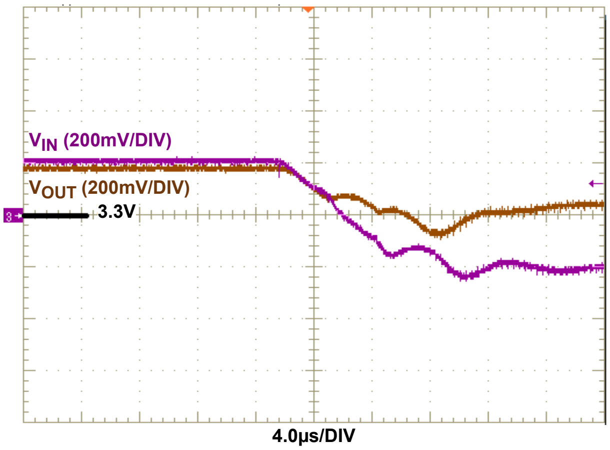


FIGURE 16. V_{SET} TOGGLE RESPONSE, V_{IN} = 3.5V -> 3.1V, LOAD = 1A

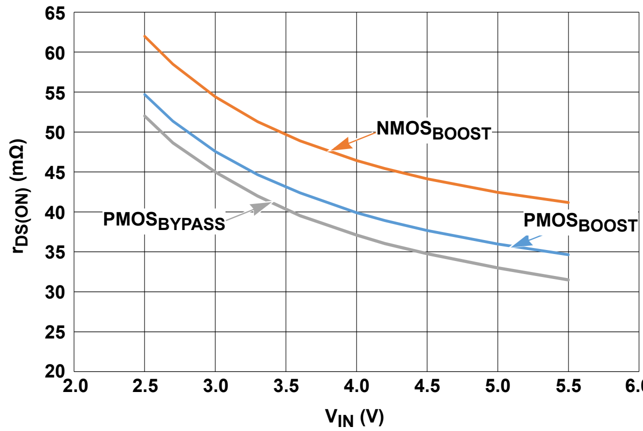


FIGURE 17. MOS $r_{DS(ON)}$ vs V_{IN}

Functional Description

Functional Overview

Refer to the “Block Diagram” on page 2. The ISL91133 implements a complete boost switching regulator with PWM controller, internal switches, references, protection circuitry, and bypass control.

Internal Supply and References

Referring to the “Block Diagram” on page 2, the ISL91133 provides a power input pin. The VIN pin provides an operating voltage source required for stable V_{REF} generation. During Bypass mode, the VIN pin also carries the input power to the output. Separate ground pins (GND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin, EN, allows the device to be enabled. Driving EN low invokes a power-down mode, where most internal device functions, including input and output power-good detection, are disabled.

POR Sequence and Soft-start

Bringing the EN pin high allows the device to power up. A number of events occur during the start-up sequence. The internal voltage reference powers up, and stabilizes. The device then starts operating.

When the device is enabled, the start-up cycle starts in the Linear mode. During the linear phase, the bypass FET Q3 is controlled as a constant current source, delivering a fixed current I_{LIN1} as shown in the “Electrical Specifications” table on page 5. If the output voltage has not reached the V_{IN} - 300mV threshold within the 512µs time interval during the I_{LIN1} mode, the ISL91133 enters a level 2 Linear mode, where the bypass MOSFET Q3 is controlled as a constant current source, delivering a fixed current I_{LIN2} as shown in the “Electrical Specifications” table on page 5. If V_{OUT} still has not reached the V_{IN} - 300mV threshold within 1024µs in the I_{LIN2} current, a fault condition is triggered.

When V_{OUT} successfully rises to within 300mV from V_{IN} within either the I_{LIN2} or I_{LIN2} period, the boost operation starts. The boost operation begins with a fixed duty-cycle of 75% with a reduced current limit ($I_{PK\_LMT\_SU}$) as shown in the “Electrical Specifications” on page 4. The fixed duty-cycle operation continues until the output voltage reaches 2.3V, then the closed-loop current mode PWM loop overrides the duty cycle to regulate the output voltage.

If the output has not reached the target regulation voltage after 64µs, a FAULT condition is triggered.

Due to the soft-start current limits and time constraints, it is recommended that the output current be limited to below 500mA at power-up, especially when the output capacitor value is large. If the output current exceeds the start-up capability, a fault condition is triggered. The regulator shuts down for 20ms, then soft-start repeats. This Hiccup mode continues until the output current is reduced to reach the regulated output voltage.

Boost Mode Overcurrent Protection

When the inductor peak current in the N-channel MOSFET reaches the current limit for 16 consecutive switching cycles, the internal protection circuit is triggered, and switching is stopped for approximately 20ms. The device then performs a soft-start cycle. If the external output overcurrent condition exists after the soft-start cycle, the device again detects 16 consecutive switching cycles reaching the valley current threshold. The process repeats as long as the external overcurrent condition is present. This behavior is called ‘Hiccup mode’.

Short-Circuit Protection

The ISL91133 provides short-circuit protection by monitoring the output voltage. When output voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The N-channel MOSFET peak current limit remains active during this state.

Boost Conversion Topology

The ISL91133 integrates one N-channel MOSFET (Q1 in the block diagram on page 2) and one P-channel MOSFET (Q2) to implement a synchronous boost converter. A body switch scheme is employed in Q2 to implement the true shutdown function when the device is disabled. Otherwise the step-up converter has a conduction path from the input to the output via the body diode of the P-channel MOSFET.

PWM Operation

The control scheme of the device is based on the valley current mode control, and the control loop is compensated internally. The valley current of the P-channel MOSFET switch is sensed to limit the maximum current flowing through the switch and the inductor. The typical current limit is set to 4A.

The control circuit includes a ramp generator, a slope compensator, an error amplifier and a PWM comparator. The ramp signal is derived from the inductor current. This ramp signal is then compared to the error amplifier output to generate the PWM gating signals for both the N-channel and the P-channel MOSFETs. The PWM operation is initialized by the clock from the internal oscillator (typical 2.5MHz). The P-channel MOSFET is turned on at the beginning of a PWM cycle, the N-channel MOSFET remains off, and the current starts ramping down. When the sum of the ramp and the slope compensator output reaches the error amplifier output voltage, the PWM comparator outputs a signal to turn off the P-channel MOSFET. At this time, both MOSFETs remain off during the dead-time interval. After the dead time, the N-channel MOSFET is turned on and remains on until the end of this PWM cycle. During this time, the inductor current ramps up until the next clock. Following a short dead time, the P-channel MOSFET is turned on again, repeating as previously described.

PFM Operation

The boost converter is capable of operating in two different modes. When the inductor current is sensed to cross zero for eight consecutive times, the converter enters PFM mode. In PFM mode, each pulse cycle is still synchronized by the PWM clock. The N-channel MOSFET is turned on at the rising edge of the clock and turned off when the inductor valley current reaches typically 20% of the current limit. Then the P-channel MOSFET is turned on, and it stays on until its current goes to zero. Subsequently, both N-channel and P-channel MOSFETs are turned off until the next clock cycle starts, at which time the N-channel MOSFET is turned on again. When V_{OUT} is 1.5% higher than the nominal output voltage, the N-channel MOSFET is immediately turned off and the P-channel MOSFET is turned on until the inductor current goes to zero. The N-channel MOSFET resumes operation when V_{OUT} falls back to its nominal value, repeating the previous operation. The converter returns to 2.5MHz PWM mode operation when V_{OUT} drops to 1.5% below its nominal voltage.

Based on this PFM mode algorithm, the average value of the output voltage is approximately 0.75% higher than the nominal output voltage under PWM operation. This positive offset improves the load transient response when switching from skip mode to PWM mode operation. The ripple on the output voltage is typically 1.5%*V_{OUT} (nominal) when input voltage is sufficiently lower than output voltage, and it increases as input voltage approaches output voltage.

Bypass Operation

The ISL91133 is designed to allow bypass operation when the input voltage is within close proximity of the output voltage. The bypass operation is provided by a 38mΩ P-channel MOSFET Q3 connecting between VIN and VOUT. In the bypass mode, Q1 in the boost circuit is turned off and Q2 is turned on. Thus, the effective bypass resistance is the parallel combination of the r_{ON} of Q3, and the series of the inductor DCR and r_{ON} of Q2.

There are two ways to enter Bypass mode: Auto Bypass and Forced Bypass.

AUTO BYPASS

Auto bypass is enabled by pulling the $\overline{BYPS}$ pin HIGH. When V_{IN} is 1.5% higher than the target V_{OUT} regulation and no switching has occurred for 5µs, the device automatically enters the bypass mode. Figures 18 and 19 illustrate the time sequence of the auto bypass mode entry.

FORCED BYPASS

Forced Bypass mode can be activated by pulling the $\overline{BYPS}$ pin LOW. Figures 20 and 21 illustrate the time sequence of the forced bypass entry. If V_{OUT} is <V_{IN} when forced bypass is requested ($\overline{BYPS}$ is LOW), the bypass MOSFET Q3 is controlled as a current source to regulate V_{OUT}. If V_{OUT} is > V_{IN} when bypass is requested ($\overline{BYPS}$ is LOW), to prevent reverse current flowing from the output to the battery, the ISL91133 first stops the boost operation and activates an internal discharge circuit to discharge the output voltage to the V_{IN} level before bypass can take place.

FAULT MODE

The ISL91133 enters a FAULT mode if one of the following conditions are encountered:

1. During start-up, V_{OUT} does not reach the threshold from Linear mode to Boost mode within the preset time interval.
2. In Boost mode, peak current limit is reached for longer than 2ms.

PG FLAG

PG is an open-drain output, it provides a flag signal (Hi-Z) to the system when power-up is successful. The PG also provides an early warning flag for overcurrent and over-temperature conditions by turning on the open-drain FET. If a fault condition is encountered, the PG is deasserted.

To summarize, PG is deasserted if:

1. V_{OUT} drops below the PG low threshold (96% of V_{OUT}).
2. Die temperature has reached the thermal warning threshold (+120°C typ).
3. A fault condition is encountered.

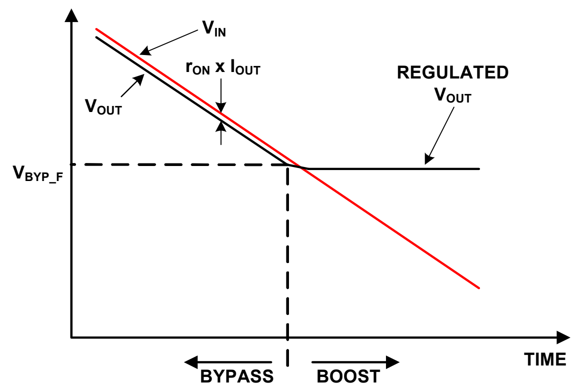


FIGURE 18. AUTO BYPASS WITH FALLING V_{IN}

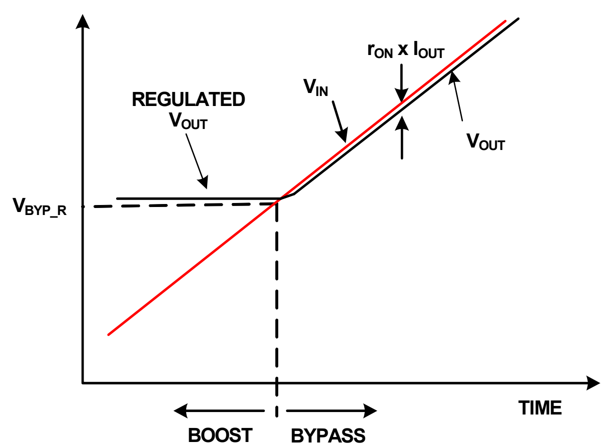


FIGURE 19. AUTO BYPASS WITH RISING V_{IN}

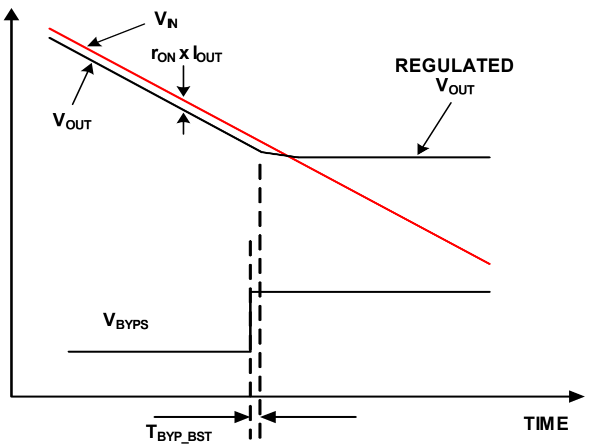


FIGURE 20. FORCED MODE, BYPASS TO BOOST

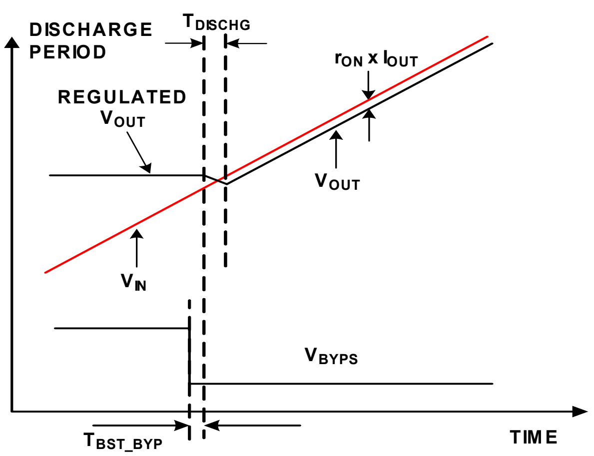


FIGURE 21. FORCED MODE, BOOST TO BYPASS

Thermal Shutdown

A built-in thermal protection feature protects the ISL91133, if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal-shutdown mode. When the die temperature falls to +120°C (typical), the device resumes normal operation.

Applications Information

Component Selection

Refer to the typical application circuit in Figure 1 on page 1, and the following component selection sections.

INDUCTOR SELECTION

An inductor with high frequency core material (for example, ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 0.47µH inductor with ≥3A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	INDUCTANCE (µH)	DIMENSION (mm)
TDK	TFM201610A	0.47	2.0x1.6x1.0
TOKO	DFE201610R	0.47	2.0x1.6x1.0
CYNTEC	PIFE32251B	0.47	3.2x2.5x1.2

V_{IN} AND V_{OUT} CAPACITOR SELECTION

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 22µF. The recommended V_{OUT} capacitor value is 10µF to 22µF.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91133. Position the input and output capacitors as close to the IC as possible. Keep the ground connections of the input and output capacitors as short as possible and on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

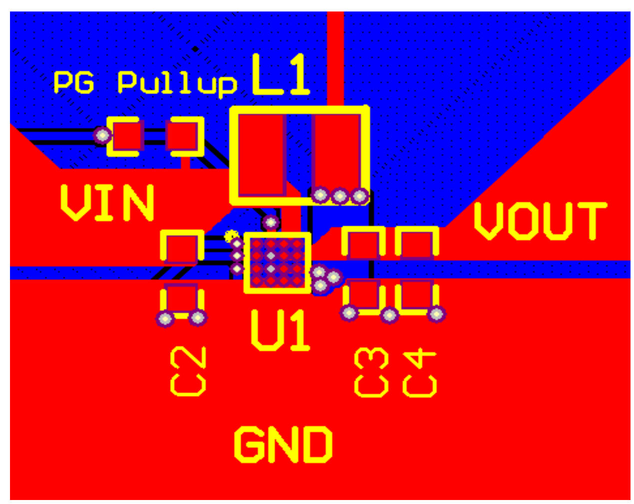


FIGURE 22. LAYOUT RECOMMENDATION

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jul 12, 2018	FN8680.1	Updated Related Literature section. Updated the ordering information table by adding Tape and Reel quantity column. Removed About Intersil section and updated Disclaimer.
Sep 5, 2014	FN8680.0	Initial Release

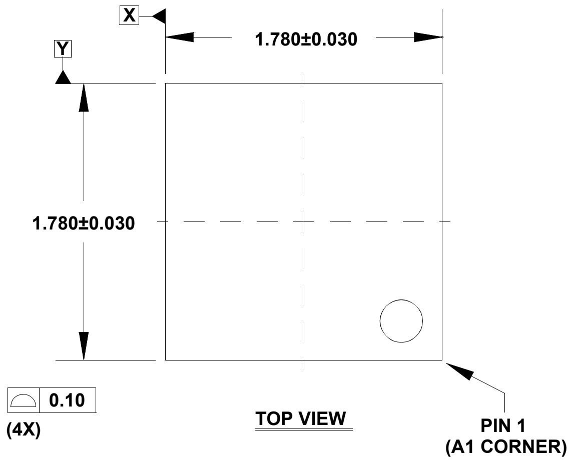
Package Outline Drawing

W4x4.16E

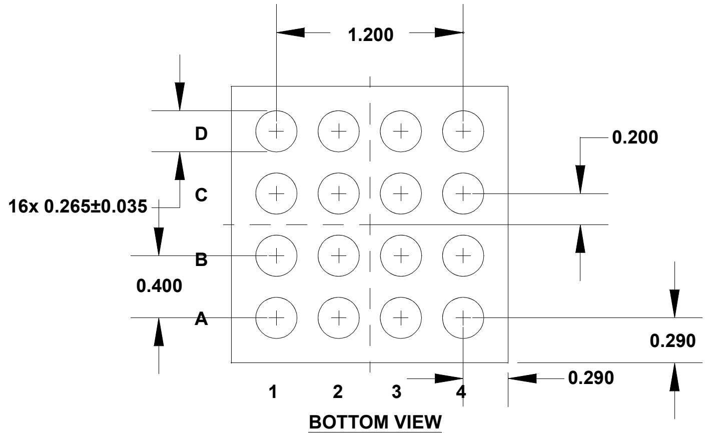
For the most recent package outline drawing, see W4x4.16E.

4X4 ARRAY 16 BALLS WITH 0.40 PITCH WAFER LEVEL CHIP SCALE PACKAGE

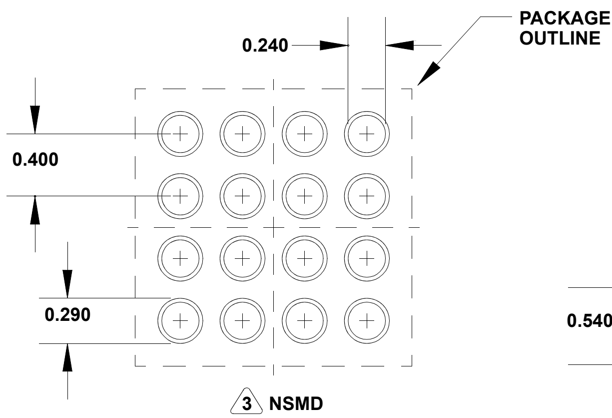
Rev 0, 2/13



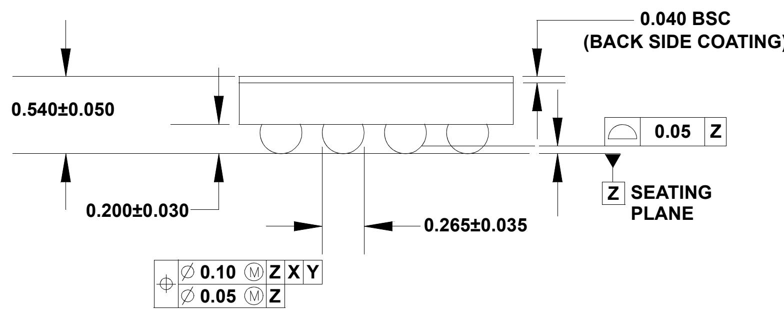
TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. All dimensions are in millimeters.
2. Dimension and tolerance conform to ASMEY14.5-1994, and JESD 95-1 SPP-010.
3. NSMD refers to non-solder mask defined pad design per TB451.

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(Rev.4.0-1 November 2017)

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