System Clock Chip for ATI RS/RD600 series chipsets using AMD CPUs

ICS9LPRS464

Description

ATI RD/RS600 series systems using AMD CPUs

Output Features

- Integrated Series Resistors on differential outputs
- Greyhound Compatible CPU outputs
- 2 - 0.7V Low Power differential CPU pairs
- 6 - 0.7V Low Power differential SRC pairs
- 2 - 0.7V Low Power differential ATIG pairs
- 1 - 66 MHz HyperTransport clock
- 2 - 48MHz USB clocks
- 3 - 14.318MHz Reference clocks

Key Specifications

- CPU outputs cycle-to-cycle jitter <150ps
- SRC outputs cycle-to-cycle jitter < 125ps
- ATIG outputs cycle-to-cycle jitter < 125ps
- +/- 100ppm frequency accuracy on all outputs if REF is tuned to +/-100ppm

Features/Benefits:

- 3 - Programmable Clock Request pins for SRC and ATIG clocks
- ATIGCLKs are programmable for frequency
- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal load capacitors for maximum frequency accuracy

Pin Configuration

9LPRS464

GNDREF	1	56	FS0/REF0
VDDREF	2	55	FS1/REF1
X1	3	54	FS2/REF2
X2	4	53	**PD
VDD48	5	52	VDDHTT
48MHz_0	6	51	HTTCLK0
48MHz_1	7	50	GNDHTT
GND48	8	49	*CLKREQA#
SMBCLK	9	48	CPUKG0T_LPR
SMBDAT	10	47	CPUKG0C_LPR
RESET_IN#	11	46	VDDCPU
SRC5T_LPR	12	45	GNDCPU
SRC5C_LPR	13	44	CPUKG1T_LPR
VDDSRC	14	43	CPUKG1C_LPR
GNDSRC	15	42	VDDA
SRC4T_LPR	16	41	GNDA
SRC4C_LPR	17	40	NC
SRC3T_LPR	18	39	SRC0T_LPR
SRC3C_LPR	19	38	SRC0C_LPR
SRC2T_LPR	20	37	GNDSRC
SRC2C_LPR	21	36	VDDSRC
GNDSRC	22	35	ATIG0T_LPR
VDDSRC	23	34	ATIG0C_LPR
SRC1T_LPR	24	33	VDDATIG
SRC1C_LPR	25	32	GNDATIG
VDDSRC	26	31	ATIG1T_LPR
GNDSRC	27	30	ATIG1C_LPR
*CLKREQB#	28	29	*CLKREQC#

56-Pin SSOP/TSSOP

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

Power Groups

Pin Number		Description
VDD	GND	
5	8	USB_48 outputs
14,23,26,36	15,22,27,37	SRCCLK outputs
33	32	ATIGCLK differential outputs
42	41	Analog, PLL
46	45	CPUCLK8 differential outputs
52	50	HTTCLK output
2	1	REF outputs

Funtionality

FS2	FS1	FS0	CPU MHz	HTT MHz	SRC MHz	ATIG MHz	USB MHz
0	0	0	Hi-Z	Hi-Z	100.00	100.00	48.00
0	0	1	X / 2	X / 3	100.00	100.00	48.00
0	1	0	230.00	76.67	100.00	100.00	48.00
0	1	1	240.00	80.00	100.00	100.00	48.00
1	0	0	100.00	66.66	100.00	100.00	48.00
1	0	1	133.33	66.66	100.00	100.00	48.00
1	1	0	166.67	66.66	100.00	100.00	48.00
1	1	1	200.00	66.66	100.00	100.00	48.00

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	GNDREF	GND	Ground pin for the REF outputs.
2	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
3	X1	IN	Crystal input, nominally 14.318MHz
4	X2	OUT	Crystal output, nominally 14.318MHz
5	VDD48	PWR	Power pin for the 48MHz outputs and core. 3.3V
6	48MHz_0	OUT	48MHz clock output.
7	48MHz_1	OUT	48MHz clock output.
8	GND48	GND	Ground pin for the 48MHz outputs
9	SMBCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
10	SMBDAT	I/O	Data pin for SMBus circuitry, 5V tolerant.
11	RESET_IN#	IN	Real Time falling edge triggered input, When asserted, the part initiates a power up reset with the SMBus being reset to it's power up values, and all PLL derived clocks stopped for the duration of Power up Stabilization. REF outputs continue to run.
12	SRC5T_LPR	OUT	True clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
13	SRC5C_LPR	OUT	Complement clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
14	VDDSRC	PWR	Supply for SRC, 3.3V nominal
15	GNDSRC	GND	Ground pin for the SRC outputs
16	SRC4T_LPR	OUT	True clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
17	SRC4C_LPR	OUT	Complement clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
18	SRC3T_LPR	OUT	True clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
19	SRC3C_LPR	OUT	Complement clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
20	SRC2T_LPR	OUT	True clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
21	SRC2C_LPR	OUT	Complement clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
22	GNDSRC	GND	Ground pin for the SRC outputs
23	VDDSRC	PWR	Supply for SRC, 3.3V nominal
24	SRC1T_LPR	OUT	True clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
25	SRC1C_LPR	OUT	Complement clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
26	VDDSRC	PWR	Supply for SRC, 3.3V nominal
27	GNDSRC	GND	Ground pin for the SRC outputs
28	*CLKREQB#	IN	Programmable Clock Request pin for SRC/ATIG/SB_SRC outputs. If output is selected for control, then that output is controlled as follows: 0 = Enabled, 1 = Tri-state

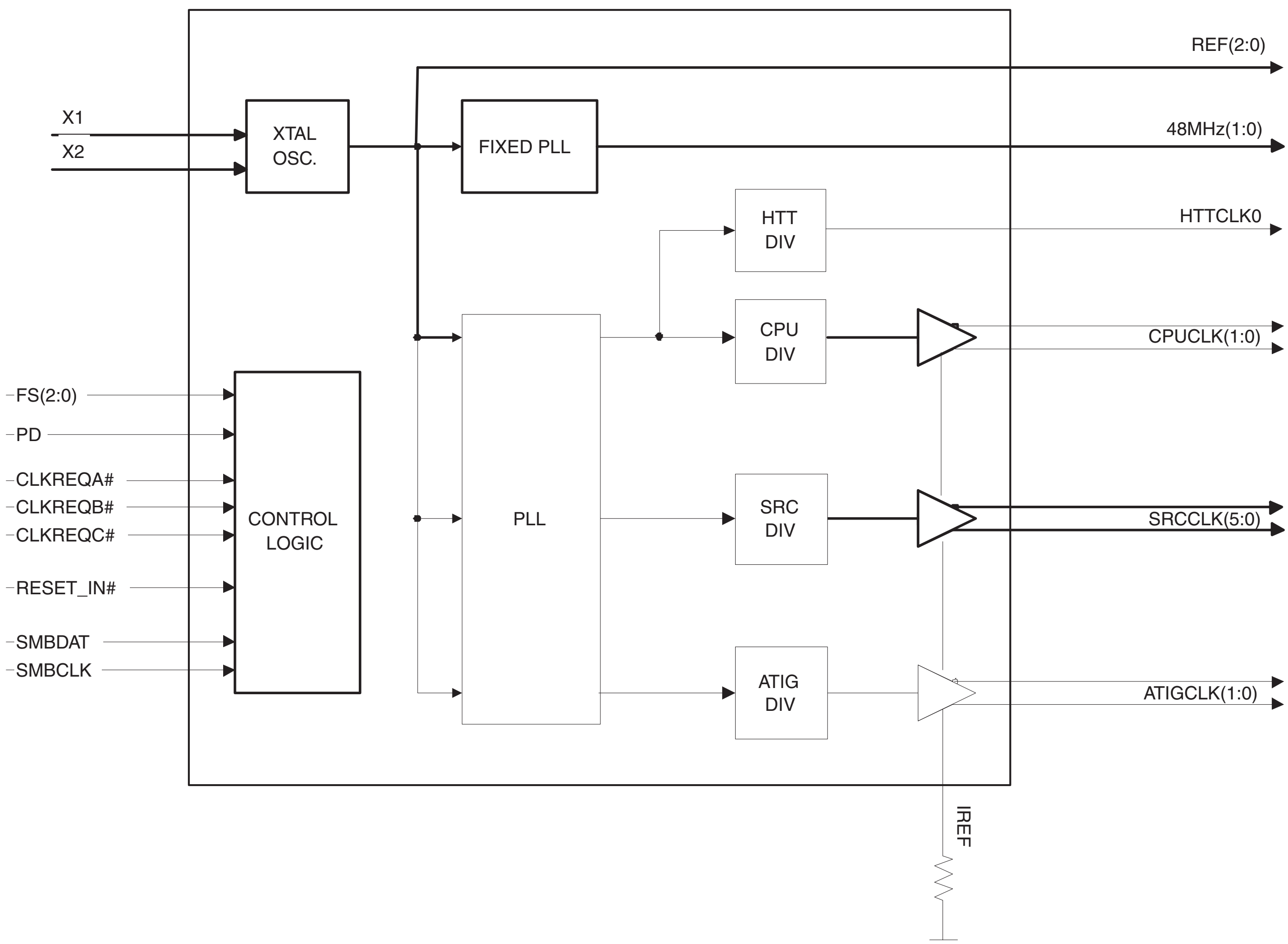
Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
29	*CLKREQC#	IN	Programmable Clock Request pin for SRC/ATIG/SB_SRC outputs. If output is selected for control, then that output is controlled as follows: 0 = Enabled, 1 = Tri-state
30	ATIG1C_LPR	OUT	Complementary clock of low-power differential push-pull PCI-Express pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
31	ATIG1T_LPR	OUT	True clock of low-power differential push-pull PCI-Express pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
32	GNDATIG	GND	Ground pin for the ATIG outputs
33	VDDATIG	PWR	Power supply for ATIG core, nominal 3.3V
34	ATIG0C_LPR	OUT	Complementary clock of low-power differential push-pull PCI-Express pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
35	ATIG0T_LPR	OUT	True clock of low-power differential push-pull PCI-Express pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
36	VDDSRC	PWR	Supply for SRC, 3.3V nominal
37	GNDSRC	GND	Ground pin for the SRC outputs
38	SRC0C_LPR	OUT	Complement clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
39	SRC0T_LPR	OUT	True clock of low power differential SRC clock pair with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
40	NC	NC	No Connect
41	GNDA	GND	Ground for the Analog Core
42	VDDA	PWR	3.3V Power for the Analog Core
43	CPUKG1C_LPR	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
44	CPUKG1T_LPR	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
45	GNDCPU	GND	Ground pin for the CPU outputs
46	VDDCPU	PWR	Supply for CPU, 3.3V nominal
47	CPUKG0C_LPR	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
48	CPUKG0T_LPR	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated 33 ohm series resistor. (no 50ohm shunt resistor to GND needed)
49	*CLKREQA#	IN	Programmable Clock Request pin for SRC/ATIG/SB_SRC outputs. If output is selected for control, then that output is controlled as follows: 0 = Enabled, 1 = Tri-state
50	GNDHTT	PWR	Ground pin for the HTT outputs
51	HTTCLK0	OUT	3.3V single ended 66MHz hyper transport clock
52	VDDHTT	PWR	Supply for HTT clocks, nominal 3.3V.
53	**PD	IN	Enter /Exit Power Down. 1 = Power Down, 0 = normal operation.
54	FS2/REF2	I/O	Frequency select latch input pin/ 3.3V 14.318MHz reference clock
55	FS1/REF1	I/O	Frequency select latch input pin/ 3.3V 14.318MHz reference clock
56	FS0/REF0	I/O	Frequency select latch input pin/ 3.3V 14.318MHz reference clock

General Description

The ICS9LPRS464 is a main clock synthesizer chip that provides all clocks required for ATI RD/RS600-based systems. An SMBus interface allows full control of the device.

Funtional Block Diagram



Absolute Max

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V_{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	9LPRS462, all outputs driven			200	mA	1
		9LPRS464, all outputs driven			180	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs low/low			21	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

AC Electrical Characteristics - Low-Power DIF Outputs: CPUKG and HTT

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement			140	mV	1,2,5
Frequency	f	Spread Specturm On	198.8		200	MHz	1,3
Long Term Accuracy	ppm	Spread Specturm Off	-300		+300	ppm	1,11
Rising Edge Slew Rate	S_{RISE}	Differential Measurement	0.5		10	V/ns	1,4
Falling Edge Slew Rate	S_{FALL}	Differential Measurement	0.5		10	V/ns	1,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
CPU, DIF HTT Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement			150	ps	1,6
Accumulated Jitter	t_{JACC}	See Notes			1	ns	1,7
Peak to Peak Differential Voltage	$V_{D(PK-PK)}$	Differential Measurement	400		2400	mV	1,8
Differential Voltage	V_D	Differential Measurement	200		1200	mV	1,9
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
Amplitude Variation	ΔV_D	Change in V_D DC cycle to cycle	-75		75	mV	1,10
CPU Skew	CPU_{SKEW10}	Differential Measurement			100	ps	1

Guaranteed by design and characterization, not 100% tested in production.

Single-ended measurement at crossing point. Value is maximum – minimum over all time. DC value of common mode is not important due to the blocking cap.

Minimum Frequency is a result of 0.5% down spread spectrum

Differential measurement through the range of ±100 mV, differential signal must remain monotonic and within slew rate spec when crossing through this region.

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] Max difference of t_{CYCLE} between any two adjacent cycles.

[7] Accumulated tjc.over a 10 µs time period, measured with JIT2 TIE at 50ps interval.

[8] VD(PK-PK) is the overall magnitude of the differential signal.

[9] VD(min) is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V VD. VD(max) is the largest amplitude allowed.

[10] The difference in magnitude of two adjacent VD_DC measurements. VD_DC is the stable post overshoot and ring-back part of the signal.

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

AC Electrical Characteristics - Low-Power DIF Outputs: SRC and ATIG

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.5		2	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.5		2	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot			1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300			mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300			mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
SRC, ATIG, Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement			125	ps	1
SRC[5:0] Skew	SRC_{SKEW}	Differential Measurement			250	ps	1
SB_SRC[1:0] Skew	SRC_{SKEW}	Differential Measurement			100	ps	1
ATIG[3:0] Skew	SRC_{SKEW}	Differential Measurement			100	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - USB - 48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8229		20.8344	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	9.3750		11.4580	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	9.3750		11.4580	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1.5	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1.5	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			130	ps	1,2

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 33Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]ICS recommended and/or chipset vendor layout guidelines must be followed to meet this specification

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270	69.84	69.8550	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	30.9290		37.9130	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	30.9290		37.9130	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		1.5	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		1.5	ns	1
Skew	t_{sk1}	V_T = 1.5 V			100	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			300	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 33Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Table1: CPU and HTT Frequency Selection Table

Byte 0					CPUCLK (2:0) (MHz)	HTT (MHz)	Spread %	Overclock %
Bit4	Bit3	Bit2	Bit1	Bit0				
CPU SS_EN	CPU FS3	CPU FS2	CPU FS1	CPU FS0				
0	0	0	0	0	Hi-Z	Hi-Z	None	
0	0	0	0	1	X / 2	X / 3	None	
0	0	0	1	0	230.00	76.67	None	**15%**
0	0	0	1	1	240.00	80.00	None	**20%**
0	0	1	0	0	100.00	66.67	None	**0%**
0	0	1	0	1	133.33	66.67	None	
0	0	1	1	0	166.67	66.67	None	
0	0	1	1	1	200.00	66.67	None	
0	1	0	0	0	250.00	83.33	None	**25%**
0	1	0	0	1	260.00	86.67	None	**30%**
0	1	0	1	0	270.00	90.00	None	**35%**
0	1	0	1	1	280.00	93.33	None	**40%**
0	1	1	0	0	102.00	68.00	None	**2%**
0	1	1	0	1	136.00	68.00	None	
0	1	1	1	0	170.00	68.00	None	
0	1	1	1	1	204.00	68.00	None	
1	0	0	0	0	210.00	70.00	-0.5%	**5%**
1	0	0	0	1	220.00	73.33	-0.5%	**10%**
1	0	0	1	0	230.00	76.67	-0.5%	**15%**
1	0	0	1	1	240.00	80.00	-0.5%	**20%**
1	0	1	0	0	100.00	66.67	-0.5%	**0%**
1	0	1	0	1	133.33	66.67	-0.5%	
1	0	1	1	0	166.67	66.67	-0.5%	
1	0	1	1	1	200.00	66.67	-0.5%	
1	1	0	0	0	250.00	83.33	-0.5%	**25%**
1	1	0	0	1	260.00	86.67	-0.5%	**30%**
1	1	0	1	0	270.00	90.00	-0.5%	**35%**
1	1	0	1	1	280.00	93.33	-0.5%	**40%**
1	1	1	0	0	102.00	68.00	-0.5%	**2%**
1	1	1	0	1	136.00	68.00	-0.5%	
1	1	1	1	0	170.00	68.00	-0.5%	
1	1	1	1	1	204.00	68.00	-0.5%	

Table2: SRC Frequency Selection Table

Byte 0	Byte 5				SRC(7:0) (MHz)	Spread %	SRC OverClock %
Bit 5	Bit3	Bit2	Bit1	Bit0			
SRC SS_EN	SRC FS3	SRC FS2	SRC FS1	SRC FS0			
0	0	0	0	0	100.00	0	0%
0	0	0	0	1	101.00	0	1%
0	0	0	1	0	102.00	0	2%
0	0	0	1	1	103.00	0	3%
0	0	1	0	0	104.00	0	4%
0	0	1	0	1	105.00	0	5%
0	0	1	1	0	106.00	0	6%
0	0	1	1	1	107.00	0	7%
0	1	0	0	0	100.00	0	0%
0	1	0	0	1	101.00	0	1%
0	1	0	1	0	102.00	0	2%
0	1	0	1	1	103.00	0	3%
0	1	1	0	0	104.00	0	4%
0	1	1	0	1	105.00	0	5%
0	1	1	1	0	106.00	0	6%
0	1	1	1	1	107.00	0	7%
1	0	0	0	0	100.00	-0.25%	0%
1	0	0	0	1	101.00	-0.25%	1%
1	0	0	1	0	102.00	-0.25%	2%
1	0	0	1	1	103.00	-0.25%	3%
1	0	1	0	0	104.00	-0.25%	4%
1	0	1	0	1	105.00	-0.25%	5%
1	0	1	1	0	106.00	-0.25%	6%
1	0	1	1	1	107.00	-0.25%	7%
1	1	0	0	0	100.00	-0.5%	0%
1	1	0	0	1	101.00	-0.5%	1%
1	1	0	1	0	102.00	-0.5%	2%
1	1	0	1	1	103.00	-0.5%	3%
1	1	1	0	0	104.00	-0.5%	4%
1	1	1	0	1	105.00	-0.5%	5%
1	1	1	1	0	106.00	-0.5%	6%
1	1	1	1	1	107.00	-0.5%	7%

Table3: ATIG Frequency Selection Table

Byte 0	Byte 9				ATIG(2:0) (MHz)	Spread %	ATIG OverClock %
Bit 6	Bit4	Bit3	Bit1	Bit0			
ATIG SS_EN	ATIG FS3	ATIG FS2	ATIG FS1	ATIG FS0			
0	0	0	0	0	100.00	0	0%
0	0	0	0	1	105.00	0	5%
0	0	0	1	0	110.00	0	10%
0	0	0	1	1	115.00	0	15%
0	0	1	0	0	120.00	0	20%
0	0	1	0	1	125.00	0	25%
0	0	1	1	0	130.00	0	30%
0	0	1	1	1	135.00	0	35%
0	1	0	0	0	100.00	0	0%
0	1	0	0	1	105.00	0	5%
0	1	0	1	0	110.00	0	10%
0	1	0	1	1	115.00	0	15%
0	1	1	0	0	120.00	0	20%
0	1	1	0	1	125.00	0	25%
0	1	1	1	0	130.00	0	30%
0	1	1	1	1	135.00	0	35%
1	0	0	0	0	100.00	-0.25%	0%
1	0	0	0	1	105.00	-0.25%	5%
1	0	0	1	0	110.00	-0.25%	10%
1	0	0	1	1	115.00	-0.25%	15%
1	0	1	0	0	120.00	-0.25%	20%
1	0	1	0	1	125.00	-0.25%	25%
1	0	1	1	0	130.00	-0.25%	30%
1	0	1	1	1	135.00	-0.25%	35%
1	1	0	0	0	100.00	-0.5%	0%
1	1	0	0	1	105.00	-0.5%	5%
1	1	0	1	0	110.00	-0.5%	10%
1	1	0	1	1	115.00	-0.5%	15%
1	1	1	0	0	120.00	-0.5%	20%
1	1	1	0	1	125.00	-0.5%	25%
1	1	1	1	0	130.00	-0.5%	30%
1	1	1	1	1	135.00	-0.5%	35%

Table 4: CPU Divider Ratios

B19b(7:4)	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	15	0111	30	1011	60	1111	120
	LSB	Address	Div	Address		Address	Div	Address	Div

Table 5: HTT Divider Ratios

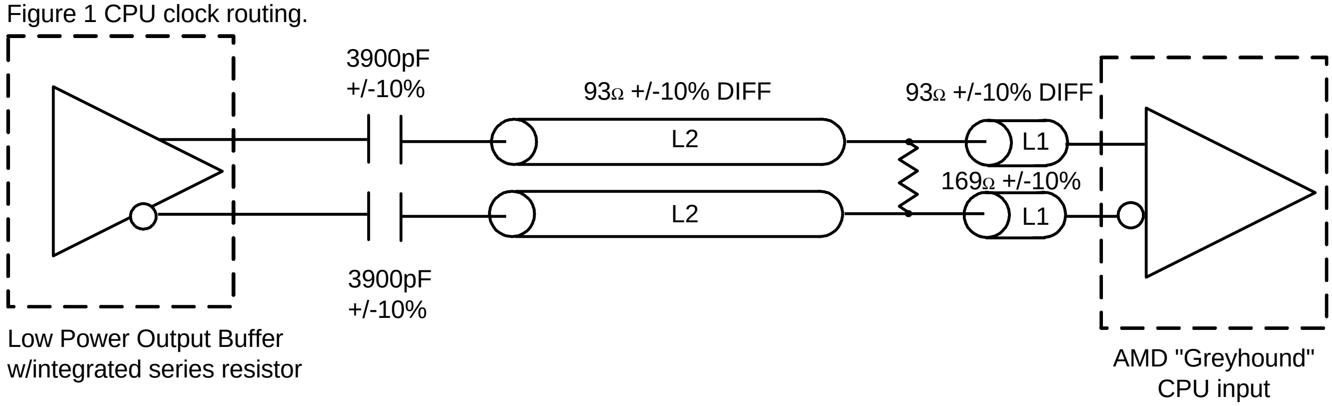
B20b(3:0)	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	4	0100	8	1000	16	1100	32
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	15	0111	30	1011	60	1111	120
	LSB	Address	Div	Address		Address	Div	Address	Div

Table 6: ATIG Divider Ratios

B19b(3:0)	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	7	0111	14	1011	28	1111	56
	LSB	Address	Div	Address		Address	Div	Address	Div

CPU Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, Route as coupled 93 ohm trace.	0.5 max	inch	1
L2 length, Route as coupled 93 ohm trace.	Contact AMD	inch	1

Figure 1 CPU clock routing.



SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch	2
L2 length, Route as non-coupled 50 ohm trace.	N/A	inch	2
L3 length, Route as non-coupled 50 ohm trace.	N/A	inch	2
Rs	33	ohm	2
Rt	49.9	ohm	2

Down Device Differential Routing	Dimension or Value	Unit	Figure
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	2 min to 16 max	inch	2
L4 length, Route as coupled **stripline** 100 ohm differential trace.	1.8 min to 14.4 max	inch	2

Differential Routing to PCI Express Connector	Dimension or Value	Unit	Figure
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	0.25 to 14 max	inch	3
L4 length, Route as coupled **stripline** 100 ohm differential trace.	0.225 min to 12.6 max	inch	3

Figure 2 Down device routing.

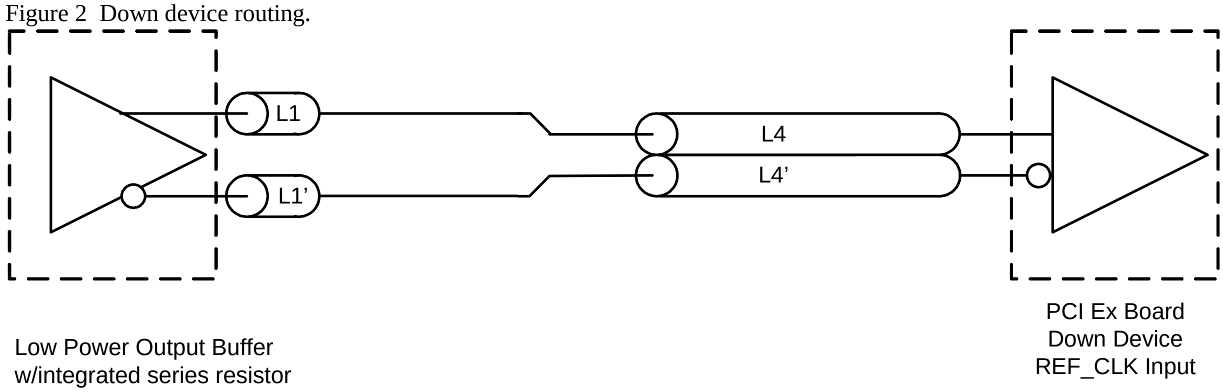


Figure 2

Figure 3 PCI Express Connector Routing.

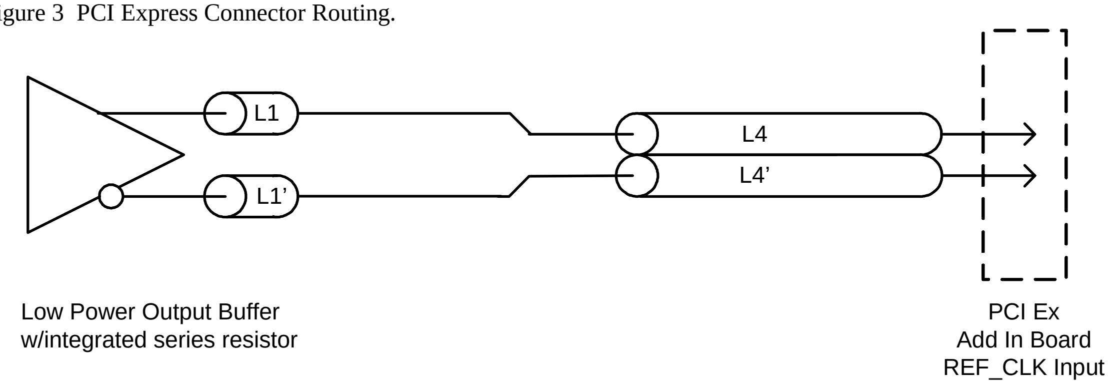


Figure 3

General SMBus serial interface information for the ICS9LPRS464

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3$_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Spread Spectrum Enable and CPU Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Latched Input or SMBus Frequency Select	RW	Latched Inputs	SMBus	0
Bit 6	-	ATIG SS_EN	ATIG Spread Spectrum Enable	RW	Disable	Enable	0
Bit 5	-	SRC SS_EN	SRC Spread Spectrum Enable	RW	Disable	Enable	0
Bit 4	-	CPU SS_EN	CPU Spread Spectrum Enable	RW	Disable	Enable	0
Bit 3	-	CPU FS3	CPU Freq Select Bit 3	RW	See Table 1: CPU Frequency Selection Table		0
Bit 2	-	CPU FS2	CPU Freq Select Bit 2	RW			Latch
Bit 1	-	CPU FS1	CPU Freq Select Bit 1	RW			Latch
Bit 0	-	CPU FS0	CPU Freq Select Bit 0	RW			Latch

Note: Each Spread Spectrum Enable bit is independent from the other.
Bit(6:4) must all set to "1" in order to enable spread for CPU, SRC and ATIG clocks.

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	7	48MHz_1	48MHz_1 Output Enable	RW	Disable	Enable	1
Bit 6	6	48MHz_0	48MHz_0 Output Enable	RW	Disable	Enable	1
Bit 5	54	REF2	REF2 Output Enable	RW	Disable	Enable	1
Bit 4	55	REF1	REF1 Output Enable	RW	Disable	Enable	1
Bit 3	56	REF0	REF0 Output Enable	RW	Disable	Enable	1
Bit 2	51	HTTCLK0	HTTCLK0 Output Enable	RW	Disable	Enable	1
Bit 1	44,43	CPUCLK1	CPUCLK1 Output Enable	RW	Disable	Enable	1
Bit 0	48,47	CPUCLK0	CPUCLK0 Output Enable	RW	Disable	Enable	1

SMBus Table: ATIGCLK and CLKREQB# Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	31,30	ATIGCLK1	ATIGCLK1 Output Enable	RW	Disable	Enable	1
Bit 4	35,34	ATIGCLK0	ATIGCLK0 Output Enable	RW	Disable	Enable	1
Bit 3	20,21	REQBSRC2	CLKREQB# Controls SRC2	RW	Does not control	Controls	0
Bit 2	Reserved						0
Bit 1	24,25	REQBSRC1	CLKREQB# Controls SRC1	RW	Does not control	Controls	0
Bit 0	Reserved						0

SMBus Table: SRCCLK Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12,13	SRCCLK5	Master Output control. Enables or disables output, regardless of CLKREQ# inputs.	RW	Disable	Enable	1
Bit 6	16,17	SRCCLK4		RW	Disable	Enable	1
Bit 5	18,19	SRCCLK3		RW	Disable	Enable	1
Bit 4	20,21	SRCCLK2		RW	Disable	Enable	1
Bit 3		Reserved		-	-	-	1
Bit 2	24,25	SRCCLK1		RW	Disable	Enable	1
Bit 1		Reserved		-	-	-	1
Bit 0	39,38	SRCCLK0		RW	Disable	Enable	1

SMBus Table: CLKREQB# and CLKREQC# Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12,13	REQASRC5	CLKREQA# Controls SRC5	RW	Does not control	Controls	0
Bit 6	16,17	REQASRC4	CLKREQA# Controls SRC4	RW	Does not control	Controls	0
Bit 5	18,19	REQASRC3	CLKREQA# Controls SRC3	RW	Does not control	Controls	0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	31,30	REQCATIG1	CLKREQC# Controls ATIG1	RW	Does not control	Controls	0
Bit 1	35,34	REQCATIG0	CLKREQC# Controls ATIG0	RW	Does not control	Controls	0
Bit 0	39,38	REQCSRC0	CLKREQC# Controls SRC0	RW	Does not control	Controls	0

SMBus Table: CPU Stop Control and SRC Frequency Select Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 8: V_IO Selection (Default is 0.8V)		1
Bit 6		IO_VOUT1	IO Output Voltage Select	RW			0
Bit 5		IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1
Bit 4	Reserved						0
Bit 3	-	SRC FS3	SRC Freq Select Bit 3	RW	See Table 2: SRC Frequency Selection Table		0
Bit 2	-	SRC FS2	SRC Freq Select Bit 2	RW			0
Bit 1	-	SRC FS1	SRC Freq Select Bit 1	RW			0
Bit 0	-	SRC FS0	SRC Freq Select Bit 0	RW			0

SMBus Table: Device ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID7 (MSB)	DEVICE ID	R	-	-	0
Bit 6	-	Device ID6		R	-	-	1
Bit 5	-	Device ID5		R	-	-	1
Bit 4	-	Device ID4		R	-	-	0
Bit 3	-	Device ID3		R	-	-	0
Bit 2	-	Device ID2		R	-	-	1
Bit 1	-	Device ID1		R	-	-	0
Bit 0	-	Device ID0 (LSB)		R	-	-	0

SMBus Table: Revision and Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will congiure how many bytes will be read back, default is 9 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			1

SMBus Table: REF2, 48MHz Output Strength Control and ATIG Frequency Select Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	54	REF2Str	REF2 Strength Control	RW	1X	2X	1
Bit 6	7	48MHz_1Str	48MHz_1 Strength Control	RW	1X	2X	1
Bit 5	6	48MHz_0Str	48MHz_0 Strength Control	RW	1X	2X	1
Bit 4	Reserved						0
Bit 3	-	ATIG FS3	ATIG Freq Select Bit 3	RW	See Table 3: ATIG Frequency Selection Table		0
Bit 2	-	ATIG FS2	ATIG Freq Select Bit 2	RW			0
Bit 1	-	ATIG FS1	ATIG Freq Select Bit 1	RW			0
Bit 0	-	ATIG FS0	ATIG Freq Select Bit 0	RW			0

SMBus Table: PLLs M/N Programming Enable and REF1, REF0 Output Strength Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLLs M/N Programming Enable	RW	Disable	Enable	0
Bit 6	55	REF1Str	REF1 Strength Control	RW	1X	2X	1
Bit 5	56	REF0Str	REF0 Strength Control	RW	1X	2X	1
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div 9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: ATIG PLL VCO Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: ATIG PLL VCO Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: ATIG PLL Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: ATIG PLL Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: CPU and ATIG Divider Ratio Programming Bits Select Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPU_Div3	CPU_Divider Ratio Programming Bits	RW	See Table 4: CPU Divider Ratios		X
Bit 6	-	CPU_Div2		RW			X
Bit 5	-	CPU_Div1		RW			X
Bit 4	-	CPU_Div0		RW			X
Bit 3	-	ATIG_Div3	ATIG_Divider Ratio Programming Bits	RW	See Table 5: ATIG Divider Ratios		X
Bit 2	-	ATIG_Div2		RW			X
Bit 1	-	ATIG_Div1		RW			X
Bit 0	-	ATIG_Div0		RW			X

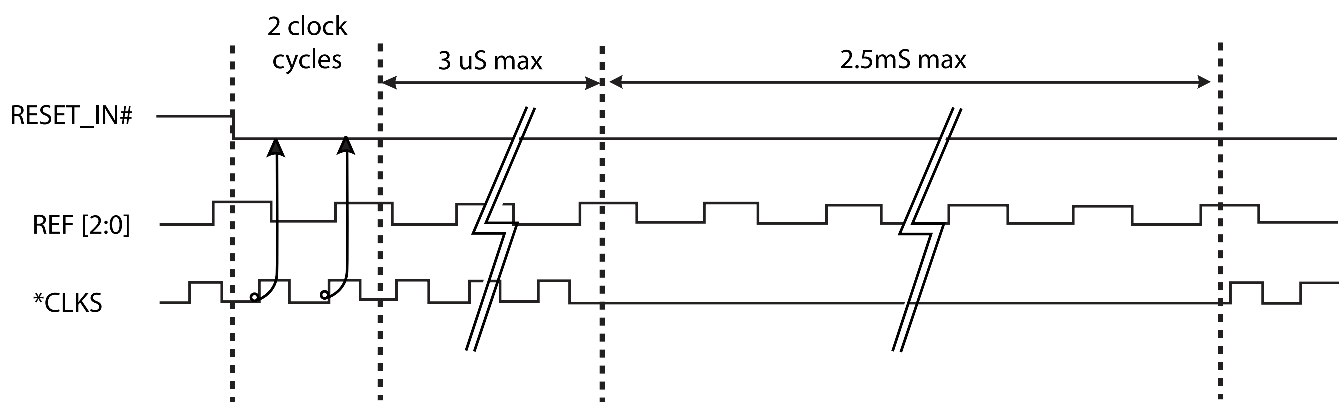
SMBus Table: HTT Divider Ratio Programming Bits Select Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	-	HTT_Div3	HTT_Divider Ratio Programming Bits	RW	See Table 6: HTT Divider Ratios		X
Bit 2	-	HTT_Div2		RW			X
Bit 1	-	HTT_Div1		RW			X
Bit 0	-	HTT_Div0		RW			X

RESET_IN# - Assertion (transition from '1' to '0')

Asserting RESET_IN pin stops all the outputs including CPU, SRC, ATIG, PCI and USB with the REF[2:0] running. The pin is a Schmitt trigger input with debouncing. After it is triggered, REF clocks will wait for two clock cycle to ensure the RESET_IN is asserted. Then, it will take 3uS for the clocks to stop without glitches. The clock chip will be power down and re-power up, and SMBus will be reloaded. It will take no more than 2.5mS for the clocks to come out with correct frequencies and no glitches.

**** Deassertion of RESET_IN# (transition from '0' to '1') has NO effect on the clocks.**



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS9LPRS464** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.
Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

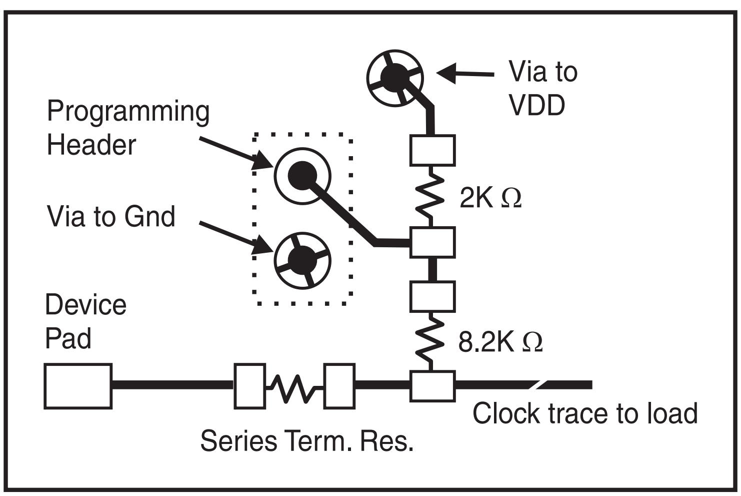
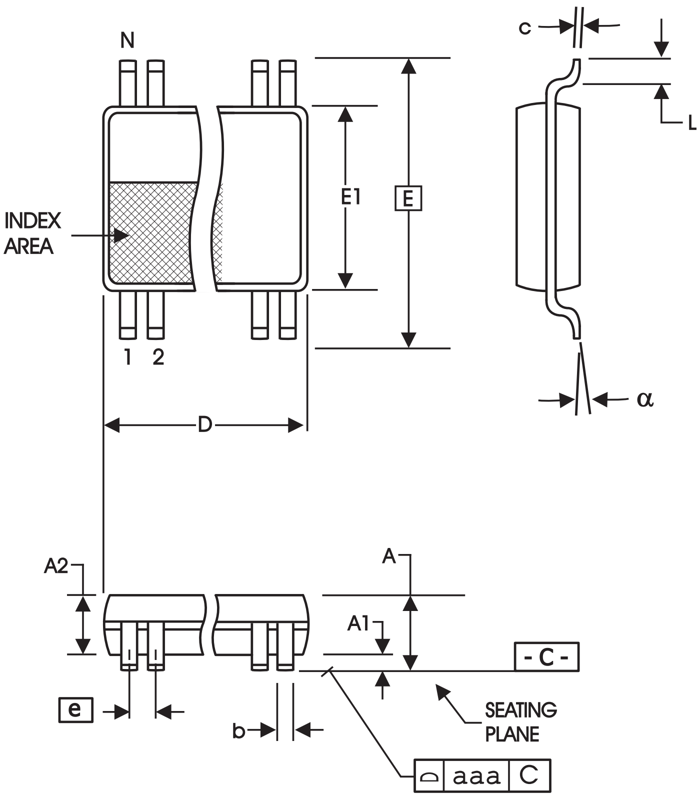


Fig. 1



56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS 9LPRS464yGLFT

Example:

ICS XXXX y G LF T

- **T** — **Designation for tape and reel packaging**
- **LF** — **Lead Free, RoHS Compliant**
- **G** — **Package Type**
  G = TSSOP
- **y** — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type**

Revision History

Rev.	Issue Date	Description	Page #
A	4/7/2008	1. Updated IDD current. 2. Added Down device routing Diagram and PCI Express Connector Routing Diagram. 3. Going to Release. 4. Updated Rs on REF & USB to 33ohm. 5. Corrected REF ppm to +/- 100ppm.	5,7-8,13

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