

Description

The 9ZML1233E / 9ZML1253E are second generation enhanced performance DB1200ZL derivatives. The parts are pin-compatible upgrades to the 9ZML1232B, while offering much improved phase jitter performance. A fixed external feedback maintains low drift for critical QPI/UPI applications, while each input channel has software adjustable input-to-output delay to ease transport delay management for today's more complex server topologies. The 9ZML1233E and 9ZML1253E have an SMBus Write Lockout pin for increased device and system security.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- Storage
- Networking
- SSDs

Output Features

- 12 Low-Power (LP) HCSL output pairs (1233E)
- 12 Low-Power (LP) HCSL output pairs with 85Ω Zout (1253E)

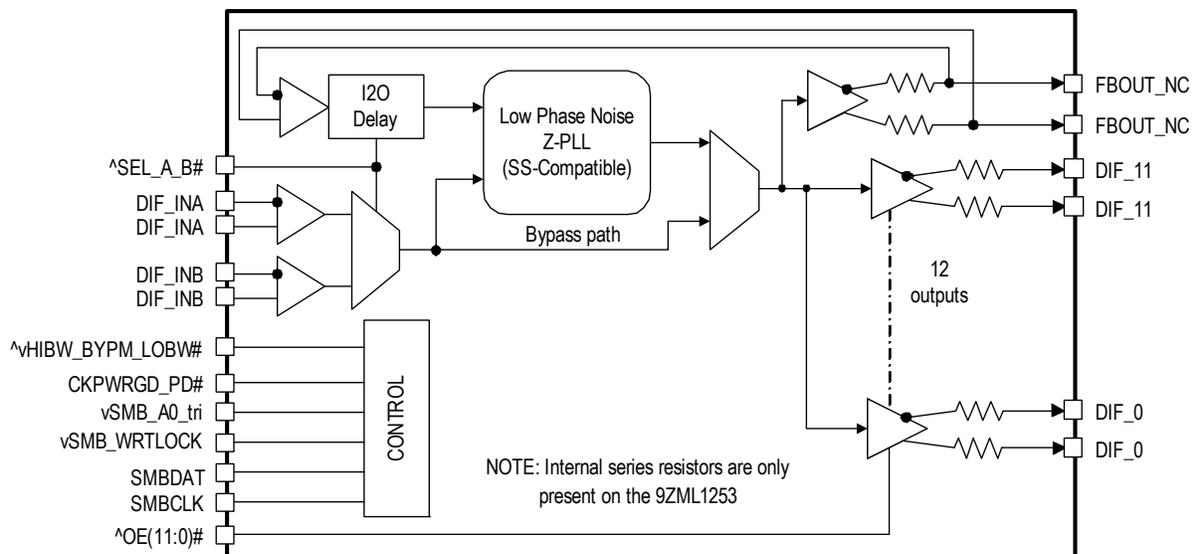
Features

- SMBus write lock feature; increases system security
- 2 software-configurable input-to-output delay lines; manage transport delay for complex topologies
- LP-HCSL outputs; eliminate 24 resistors, save 41mm² of area (1233E)
- LP-HCSL outputs with 85Ω Zout; eliminate 48 resistors, save 82mm² of area (1253E)
- 12 OE# pins; hardware control of each output
- 3 selectable SMBus addresses; multiple devices can share same SMBus segment
- Selectable PLL bandwidths; minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of PLL bandwidth and bypass; change mode without power cycle
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- 100MHz PLL Mode; UPI support
- 10 x 10 mm 72-VFQFPN package; small board footprint

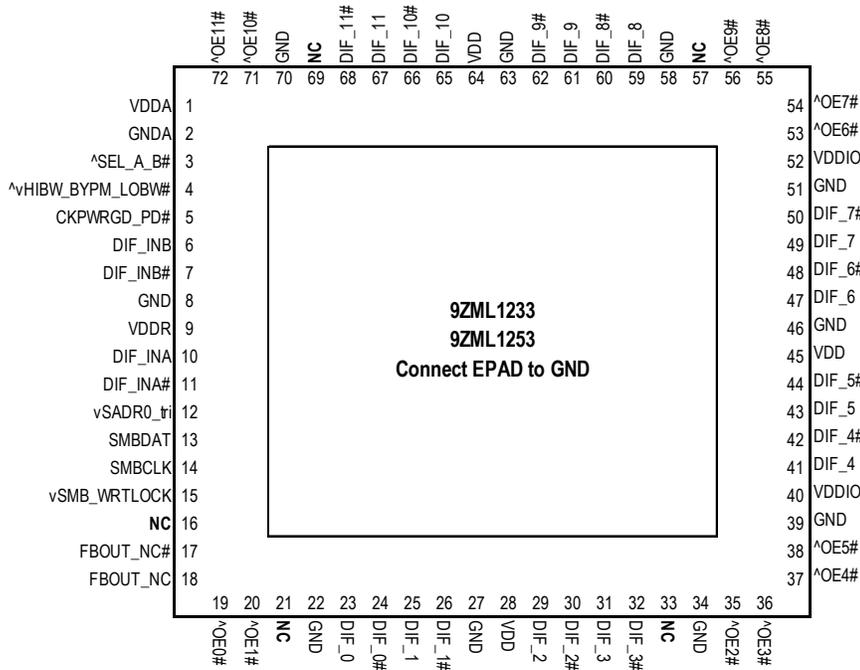
Key Specifications

- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps
- Input-to-output delay: 0ps default
- Input-to-output delay variation < 50ps
- Phase jitter: PCIe Gen4 < 0.5ps rms
- Phase jitter: UPI > 9.6GB/s < 0.1ps rms
- Phase jitter: IF-UPI < 1.0ps rms

Block Diagram



Pin Assignments



^ prefix indicates internal 120kohm pull-up
 v prefix indicates internal 120kohm pull-down
 10 x 10 mm 72-VFQFPN 0.5mm pin pitch

Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|--------|-------------------|------------|--|
| 1 | V _{DDA} | Power | Power supply for PLL core. |
| 2 | GNDA | GND | Ground pin for the PLL core. |
| 3 | ^SEL_A_B# | Input | Input to select differential input clock A or differential input clock B. This input has an internal 120kΩ pull-up resistor. 0 = input B selected, 1 = input A selected. |
| 4 | ^vHIBW_BYPM_LOBW# | Latched In | Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to V _{DD} /2 (Bypass Mode) with internal pull-up/pull-down resistors. See <i>PLL Operating Mode</i> table for details. |
| 5 | CKPWRGD_PD# | Input | 3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 6 | DIF_INB | Input | True input of differential clock. |
| 7 | DIF_INB# | Input | Complement input of differential clock. |
| 8 | GND | GND | Ground pin. |
| 9 | V _{DDR} | Power | Power supply for differential input clock (receiver). This V _{DD} should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. |
| 10 | DIF_INA | Input | True input of differential clock. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|--------------|--------|---|
| 11 | DIF_INA# | Input | Complement input of differential clock. |
| 12 | vSADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal 120kΩ pull-down resistor. See the <i>SMBus Addressing</i> table. |
| 13 | SMBDAT | I/O | Data pin of SMBUS circuitry. |
| 14 | SMBCLK | Input | Clock pin of SMBUS circuitry. |
| 15 | vSMB_WRTLOCK | Input | This pin prevents SMBus writes when asserted. SMBus reads are not affected. This pin has an internal 120kΩ pull-down. 0 = SMBus writes allows, 1 = SMBus writes blocked. |
| 16 | NC | — | No connection. |
| 17 | FBOUT_NC# | Output | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 18 | FBOUT_NC | Output | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 19 | ^OE0# | Input | Active low input for enabling output 0. This pin has an internal 120kΩ pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 20 | ^OE1# | Input | Active low input for enabling output 1. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 21 | NC | — | No connection. |
| 22 | GND | GND | Ground pin. |
| 23 | DIF_0 | Output | HCSL true clock output. |
| 24 | DIF_0# | Output | HCSL complementary clock output. |
| 25 | DIF_1 | Output | HCSL true clock output. |
| 26 | DIF_1# | Output | HCSL complementary clock output. |
| 27 | GND | GND | Ground pin. |
| 28 | VDD | Power | Power supply, nominally 3.3V. |
| 29 | DIF_2 | Output | HCSL true clock output. |
| 30 | DIF_2# | Output | HCSL complementary clock output. |
| 31 | DIF_3 | Output | HCSL true clock output. |
| 32 | DIF_3# | Output | HCSL complementary clock output. |
| 33 | NC | — | No connection. |
| 34 | GND | GND | Ground pin. |
| 35 | ^OE2# | Input | Active low input for enabling output 2. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 36 | ^OE3# | Input | Active low input for enabling output 3. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|-------------------|--------|---|
| 37 | ^OE4# | Input | Active low input for enabling output 4. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 38 | ^OE5# | Input | Active low input for enabling output 5. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 39 | GND | GND | Ground pin. |
| 40 | V _{DDIO} | Power | Power supply for differential outputs. |
| 41 | DIF_4 | Output | HCSL true clock output. |
| 42 | DIF_4# | Output | HCSL complementary clock output. |
| 43 | DIF_5 | Output | HCSL true clock output. |
| 44 | DIF_5# | Output | HCSL complementary clock output. |
| 45 | V _{DD} | PWR | Power supply, nominally 3.3V. |
| 46 | GND | GND | Ground pin. |
| 47 | DIF_6 | Output | HCSL true clock output. |
| 48 | DIF_6# | Output | HCSL complementary clock output. |
| 49 | DIF_7 | Output | HCSL true clock output. |
| 50 | DIF_7# | Output | HCSL complementary clock output. |
| 51 | GND | GND | Ground pin. |
| 52 | V _{DDIO} | Power | Power supply for differential outputs. |
| 53 | ^OE6# | Input | Active low input for enabling output 6. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 54 | ^OE7# | Input | Active low input for enabling output 7. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 55 | ^OE8# | Input | Active low input for enabling output 8. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 56 | ^OE9# | Input | Active low input for enabling output 9. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 57 | NC | — | No connection. |
| 58 | GND | GND | Ground pin. |
| 59 | DIF_8 | Output | HCSL true clock output. |
| 60 | DIF_8# | Output | HCSL complementary clock output. |
| 61 | DIF_9 | Output | HCSL true clock output. |
| 62 | DIF_9# | Output | HCSL complementary clock output. |
| 63 | GND | GND | Ground pin. |
| 64 | V _{DD} | Power | Power supply, nominally 3.3V. |
| 65 | DIF_10 | Output | HCSL true clock output. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|---------|--------|---|
| 66 | DIF_10# | Output | HCSL complementary clock output. |
| 67 | DIF_11 | Output | HCSL true clock output. |
| 68 | DIF_11# | Output | HCSL complementary clock output. |
| 69 | NC | — | No connection. |
| 70 | GND | GND | Ground pin. |
| 71 | ^OE10# | Input | Active low input for enabling output 10. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 72 | ^OE11# | Input | Active low input for enabling output 11. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs. |
| 73 | EPAD | GND | Connect to ground. |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZML1233E / 9ZML1253E. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|----------------------|-------------|-----------------------------|---------|---------|----------------|-------|-------|
| Supply Voltage | V_{DDx} | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V_{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V_{IH} | Except for SMBus interface. | | | $V_{DD} + 0.5$ | V | 1,3 |
| Input High Voltage | V_{IHSMB} | SMBus clock and data pins. | | | 5.5 | V | 1 |
| Storage Temperature | T_s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T_j | | | | 125 | °C | 1 |
| Input ESD Protection | ESD prot | Human Body Model. | 2000 | | | V | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 4.6V.

Electrical Characteristics

Over specified temperature and voltage ranges unless otherwise indicated; see Test Loads for loading conditions.

Table 3. SMBus Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---------------------------|--------------|---|---------|---------|-------------|-------|-------|
| SMBus Input Low Voltage | V_{ILSMB} | | | | 0.8 | V | |
| SMBus Input High Voltage | V_{IHSMB} | | 2.1 | | V_{DDSMB} | V | |
| SMBus Output Low Voltage | V_{OLSMB} | At I_{PULLUP} . | | | 0.4 | V | |
| SMBus Sink Current | I_{PULLUP} | At V_{OL} . | 4 | | | mA | |
| Nominal Bus Voltage | V_{DDSMB} | | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | t_{RSMB} | (Max $V_{IL} - 0.15V$) to (Min $V_{IH} + 0.15V$). | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t_{FSMB} | (Min $V_{IH} + 0.15V$) to (Max $V_{IL} - 0.15V$). | | | 300 | ns | 1 |
| SMBus Operating Frequency | f_{MAXMB} | Maximum SMBus operating frequency. | | | 400 | kHz | 5 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

⁵ The differential input clock must be running for the SMBus to be active.

Table 4. DIF_IN Clock Input Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------------|-------------|---|---------|---------|---------|---------|-------|
| Input Crossover Voltage | V_{CROSS} | Cross over voltage. | 150 | | 900 | mV | 1 |
| Input Swing – DIF_IN | V_{SWING} | Differential value. | 300 | | | mV | 1 |
| Input Slew Rate – DIF_IN | dv/dt | Measured differentially. | 0.35 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{DD}$, $V_{IN} = GND$. | -5 | | 5 | μA | |
| Input Duty Cycle | d_{tin} | Measurement from differential waveform. | 45 | | 55 | % | 1 |
| Input Jitter –Cycle to Cycle | J_{DIFIn} | Differential measurement. | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through $\pm 75mV$ window centered around differential zero.

Table 5. Input/Supply/Common Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------------------|-----------------|---|-----------|------------|----------------|--------|-------|
| Supply Voltage | V_{DDX} | Supply voltage for core and analog. | 3.135 | 3.3 | 3.465 | V | |
| | V_{DDIO} | Supply voltage for differential outputs. | 3.135 | 3.3 | 3.465 | V | |
| Ambient Operating Temperature | T_{AMB} | Industrial range. | -40 | | 85 | °C | |
| Input High Voltage | V_{IH} | Single-ended inputs, except SMBus, tri-level inputs. | 2 | | $V_{DD} + 0.3$ | V | |
| Input Low Voltage | V_{IL} | Single-ended inputs, except SMBus, tri-level inputs. | GND - 0.3 | | 0.8 | V | |
| Input High Voltage | V_{IH} | Tri-level inputs (“_tri” suffix). | 2.2 | | $V_{DD} + 0.3$ | V | |
| Input Mid Voltage | V_{IM} | Tri-level inputs (“_tri” suffix). | 1.2 | $V_{DD}/2$ | 1.8 | V | |
| Input Low Voltage | V_{IL} | Tri-level inputs (“_tri” suffix). | GND - 0.3 | | 0.8 | V | |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DDX}$. | -5 | | 5 | μA | |
| | I_{INP} | Single-ended inputs $V_{IN} = 0$ V; Inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; Inputs with internal pull-down resistors. | -100 | | 100 | μA | |
| Input Frequency | F_{IBYP} | $V_{DD} = 3.3$ V, Bypass Mode. | 1 | | 400 | MHz | |
| | F_{IPLL} | $V_{DD} = 3.3$ V, 100MHz PLL Mode. | 98.5 | 100.00 | 102 | MHz | 5 |
| Pin Inductance | L_{pin} | | | | 7 | nH | 1 |
| Capacitance | C_{IN} | Logic Inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| | C_{INDIF_IN} | DIF_IN differential clock inputs. | 1.5 | | 2.7 | pF | 1,4 |
| | C_{OUT} | Output pin capacitance. | | | 6 | pF | 1 |
| Clk Stabilization | t_{STAB} | From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock. | | 1.2 | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable frequency for PCIe applications (triangular modulation). | 30 | 31.6 | 33 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion. DIF stop after OE# deassertion. | 4 | 5 | 10 | clocks | 1,2,3 |
| Tdrive_PD# | t_{DRVPD} | DIF output enable after PD# deassertion. | | 85 | 300 | μs | 1,3 |
| Tfall | t_F | Fall time of control inputs. | | | 5 | ns | 2 |
| Trise | t_R | Rise time of control inputs. | | | 5 | ns | 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV, PLL Mode.

⁴ DIF_IN input.

⁵ This parameter reflects the operating range after locking to a 100MHz input.

Table 6. Current Consumption

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|-------------|---|---------|---------|---------|-------|-------|
| Operating Supply Current | I_{DDx} | All other V_{DD} pins, all outputs at 100MHz, $C_L = 2pF$; $Z_o = 85\Omega$. | | 22 | 30 | mA | |
| | I_{DDA+R} | $V_{DDA} + V_{DDR}$ pins, all outputs at 100MHz, $C_L = 2pF$; $Z_o = 85\Omega$. | | 56 | 65 | mA | 1 |
| | I_{DDO} | V_{DDIO} pins, all outputs at 100MHz, $C_L = 2pF$; $Z_o = 85\Omega$. | | 84 | 100 | mA | |
| Power Down Current | I_{DDx} | All other V_{DD} pins, all outputs Low/Low. | | 0.9 | 2 | mA | 1 |
| | I_{DDA+R} | $V_{DDA} + V_{DDR}$ pins, all outputs Low/Low. | | 4.3 | 6 | mA | 1 |
| | I_{DDO} | V_{DDIO} pins, all outputs Low/Low. | | 0.1 | 0.2 | mA | 1 |

¹ Includes V_{DDR} if applicable.

Table 7. Skew and Differential Jitter Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------|-----------------|---|---------|---------|---------|-------|-------------|
| CLK_IN, DIF[x:0] | t_{SKEW_PLL} | Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage. | -100 | -4 | 100 | ps | 1,2,4,5,6,8 |
| CLK_IN, DIF[x:0] | t_{PD_BYP} | Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage. | 2.2 | 2.9 | 3.6 | ns | 1,2,3,8 |
| CLK_IN, DIF[x:0] | t_{DSPO_PLL} | Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature. | -50 | 0.0 | 50 | ps | 1,2,3,8 |
| CLK_IN, DIF[x:0] | t_{DSPO_BYP} | Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, $T_{AMB} = 0$ to $70^\circ C$, default slew rate. | -250 | 0.0 | 250 | ps | 1,2,3,8 |
| | | Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, $T_{AMB} = -40$ to $85^\circ C$, default slew rate. | -350 | 0.0 | 350 | ps | 1,2,3,8 |
| DIF[x:0] | t_{SKEW_ALL} | Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz, default slew rate. | | 30 | 50 | ps | 1,2,3,8 |
| PLL Jitter Peaking | $j_{peak-hibw}$ | LOBW#_BYPASS_HIBW = 1. | 0 | 1.3 | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | $j_{peak-lobw}$ | LOBW#_BYPASS_HIBW = 0. | 0 | 1.3 | 2 | dB | 7,8 |
| PLL Bandwidth | pll_{HIBW} | LOBW#_BYPASS_HIBW = 1. | 2 | 2.6 | 4 | MHz | 8,9 |
| PLL Bandwidth | pll_{LOBW} | LOBW#_BYPASS_HIBW = 0. | 0.7 | 1.0 | 1.4 | MHz | 8,9 |
| Duty Cycle | t_{DC} | Measured differentially, PLL Mode. | 45 | 50 | 55 | % | 1 |
| Duty Cycle Distortion | t_{DCD} | Measured differentially, Bypass Mode at 100MHz. | -1 | -0.2 | 0 | % | 1,10 |
| Jitter, Cycle to Cycle | $t_{jyc-cyc}$ | PLL Mode. | | 13 | 50 | ps | 1,11 |
| | | Additive jitter in Bypass Mode. | | 0.2 | 5 | ps | 1,11 |

- ¹ Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
- ² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
- ³ All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
- ⁴ This parameter is deterministic for a given device.
- ⁵ Measured with scope averaging on to find mean value.
- ⁶ This value is programmable.
- ⁷ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- ⁸ Guaranteed by design and characterization, not 100% tested in production.
- ⁹ Measured at 3db down or half power point.
- ¹⁰ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.
- ¹¹ Measured from differential waveform.

Table 8. DIF HCSL/LP-HCSL Outputs

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------|------------------------------|--|---------|---------|---------|-----------------|-------|---------|
| Slew Rate | dV/dt | Scope averaging on. | 2.0 | 2.8 | 4.0 | 0.6 – 4.0 | V/ns | 1,2,3 |
| Slew Rate Matching | Δ dV/dt | Slew rate matching, scope averaging on. | | 4 | 15 | 20 | % | 1,2,4,7 |
| Maximum Voltage | V _{MAX} | Measurement on single-ended signal using absolute value (scope averaging off). | 660 | 794 | 870 | 1150 | mV | 7,8 |
| Minimum Voltage | V _{MIN} | | -111 | -49 | | -300 | | 7,8 |
| Crossing Voltage (abs) | V _{CROSS_ABS} | Scope averaging off. | 302 | 367 | 453 | 250 – 550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ -V _{CROSS} | Scope averaging off. | | 32 | 74 | 140 | mV | 1,6,7 |

- ¹ Guaranteed by design and characterization, not 100% tested in production.
- ² Measured from differential waveform.
- ³ Slew rate is measured through the V_{SWING} voltage range centered around differential 0 V. This results in a \pm 150mV window around differential 0V.
- ⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a \pm 75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
- ⁵ V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
- ⁶ The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS_MIN/MAX} (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting Δ -V_{CROSS} to be smaller than V_{CROSS} absolute.
- ⁷ At default SMBus settings.
- ⁸ If driving a receiver with input terminations, the V_{MAX} and V_{MIN} values will be halved.

Table 9. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------------------|--------------------|---|---------|---------|---------|-----------------|----------|---------------|
| Phase Jitter, PLL Mode | $t_{jphPCIeG1-CC}$ | PCIe Gen 1. | | 13 | 30 | 86 | ps (p-p) | 1, 2, 3, 6 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 0.25 | 0.7 | 3 | ps (rms) | 1, 2, 6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 1.00 | 1.5 | 3.1 | ps (rms) | 1, 2, 6 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.24 | 0.35 | 1 | ps (rms) | 1, 2, 6 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen 4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.24 | 0.35 | 0.5 | ps (rms) | 1, 2, 6 |
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG1-CC}$ | PCIe Gen 1. | | 0.0 | 0.05 | Not Applicable | ps (p-p) | 1, 2, 3, 4, 6 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 0.00 | 0.05 | | ps (rms) | 1, 2, 3, 4, 6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 0.00 | 0.05 | | ps (rms) | 1, 2, 3, 4, 6 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.00 | 0.05 | | ps (rms) | 1, 2, 3, 4, 6 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen 4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.00 | 0.05 | | ps (rms) | 1, 2, 3, 4, 6 |

Table 10. Filtered Phase Jitter Parameters - PCIe Independent Reference (IR) Architectures

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------------------|----------------------|--|---------|---------|---------|-----------------|----------|---------|
| Phase Jitter, PLL Mode | $t_{jphPCIeG2-SRIS}$ | PCIe Gen 2 (PLL BW of 16MHz, CDR = 5MHz). | | 0.8 | 1.2 | 2 | ps (rms) | 1, 2, 5 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen 3 (PLL BW of 2–4MHz, CDR = 10MHz). | | 0.64 | 0.68 | 0.7 | ps (rms) | 1, 2, 5 |
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG2-SRIS}$ | PCIe Gen 2 (PLL BW of 16MHz, CDR = 5MHz). | | 0.00 | 0.02 | Not Applicable | ps (rms) | 2, 4, 5 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen 3 (PLL BW of 2–4MHz, CDR = 10MHz). | | 0.00 | 0.02 | | ps (rms) | 2, 4, 5 |

Notes for PCIe Filtered Phase Jitter tables:

- ¹ Applies to all differential outputs when driven by 9SQL495x or equivalent, guaranteed by design and characterization.
- ² Calculated from Intel-supplied clock jitter tool, when driven by 9SQL495x or equivalent with spread on and off.
- ³ Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12} .
- ⁴ For RMS values, additive jitter is calculated by solving the following equation for b [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.
- ⁵ IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

Table 11. Filtered Phase Jitter Parameters – QPI/UPI

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------|-------------------|--|---------|-------------|-------------|-----------------|----------|------------|
| Phase Jitter, PLL Mode | t_{jphQPI_UPI} | QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI). | | 0.15 | 0.3 | 0.5 | ps (rms) | 1, 2 |
| | | QPI & UPI (100MHz, 8.0Gb/s, 12UI). | | 0.08 | 0.1 | 0.3 | ps (rms) | 1, 2 |
| | | QPI & UPI (100MHz, \geq 9.6Gb/s, 12UI). | | 0.07 | 0.1 | 0.2 | ps (rms) | 1, 2 |
| | t_{jphIF_UPI} | IF-UPI. | | 0.1 0.17 | 0.15 0.2 | 1 | ps (rms) | 1, 4, 5 |

Table 11. Filtered Phase Jitter Parameters – QPI/UPI (Cont.)

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------------------|-------------------------|---|---------|---------|---------|-----------------|----------|---------|
| Additive Phase Jitter, Bypass Mode | t _{jphQPI_UPI} | QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI). | | 0.00 | 0.03 | Not Applicable | ps (rms) | 1, 2, 3 |
| | | QPI & UPI (100MHz, 8.0Gb/s, 12UI). | | 0.02 | 0.07 | | ps (rms) | 1, 2, 3 |
| | | QPI & UPI (100MHz, ≥ 9.6Gb/s, 12UI). | | 0.02 | 0.06 | | ps (rms) | 1, 2, 3 |
| | t _{jphIF-UPI} | IF-UPI. | | 0.06 | 0.08 | | ps (rms) | 1, 4 |

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Calculated from Intel-supplied clock jitter tool, when driven by 9SQL495x or equivalent with spread on and off.

³ Additive jitter for RMS values is calculated by solving for b [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.

⁴ Calculated from phase noise analyzer when driven by Wenzel Associates source with Intel-specified brick-wall filter applied.

⁵ Top number is when the buffer is in Low BW mode, bottom number is when the buffer is in High BW mode.

Table 12. Unfiltered Phase Jitter Parameters – 12kHz to 20MHz

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------------------|----------------------------|-------------------------------|---------|---------|---------|-----------------|----------|-------|
| Phase Jitter, PLL Mode | t _{jph12k-20MHi} | PLL High BW, SSC Off, 100MHz. | | 171 | 250 | Not applicable | fs (rms) | 1,2 |
| Phase Jitter, PLL Mode | t _{jph12k-20MLo} | PLL Low BW, SSC Off, 100MHz. | | 183 | 250 | | fs (rms) | 1,2 |
| Additive Phase Jitter, Bypass Mode | t _{jph12k-20MByP} | Bypass Mode, SSC Off, 100MHz. | | 109 | 150 | | fs (rms) | 1,2,3 |

¹ Applies to all outputs when driven by Wenzel clock source.

² 12kHz to 20MHz brick wall filter.

³ For RMS values, additive jitter is calculated by solving for b [$a^2 + b^2 = c^2$] where “a” is rms input jitter and “c” is rms total jitter.

Power Management

| Inputs | | Control Bits | Outputs | | PLL State |
|-------------|---------|--------------|---------|----------|-----------|
| CKPWRGD_PD# | DIF_IN | SMBus EN bit | DIF_x | FBOUT_NC | |
| 0 | X | X | Low/Low | Low/Low | Off |
| 1 | Running | 0 | Low/Low | Running | On |
| | | 1 | Running | Running | On |

Power Connections (9ZML12xxE)

| Pin Number | | | Description |
|-----------------|-------------------|------------------------------------|--------------|
| V _{DD} | V _{DDIO} | GND | |
| 1 | | 2 | Analog PLL |
| 9 | | 8 | Analog input |
| 28, 45, 64 | 40, 52 | 22, 27, 34, 39, 46, 51, 58, 63, 70 | DIF clocks |

Power Connections (for pin-compatibility with 9ZML12xxB)

| Pin Number | | | Description |
|-----------------|------------------------|--|--------------|
| V _{DD} | V _{DDIO} | GND | |
| 1 | | 2 | Analog PLL |
| 9 | | 8 | Analog input |
| 28, 45, 64 | 21, 33, 40, 52, 57, 69 | 16, 22, 27, 34, 39, 46, 51, 58, 63, 70 | DIF clocks |

PLL Operating Mode

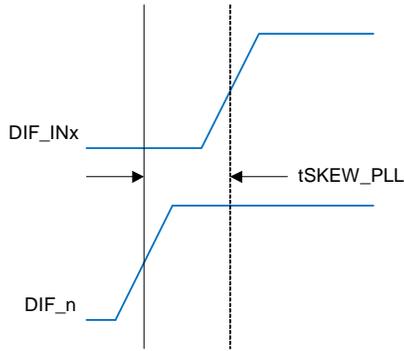
| HIBW_BYPM_LOBW# | Byte0[7:6] |
|--------------------|------------|
| Low (PLL Low BW) | 00 |
| Mid (Bypass) | 01 |
| High (PLL High BW) | 11 |

Note: PLL is off in Bypass Mode.

Skew Programming

| Skew[2:0] | Skew Steps | Skew (ps) |
|-----------|------------|-----------|
| 000 | 0 | 0 |
| 001 | 1 | -416.67 |
| 010 | 2 | -833.33 |
| 011 | 3 | -1250.00 |
| 100 | 4 | -1666.67 |
| 101 | 5 | -2083.33 |
| 110 | 6 | -2500.00 |
| 111 | 7 | -2916.67 |

Figure 1. Skew Diagram



Test Loads

Low-Power HCSL Output Test Load
(standard PCIe source-terminated test load)

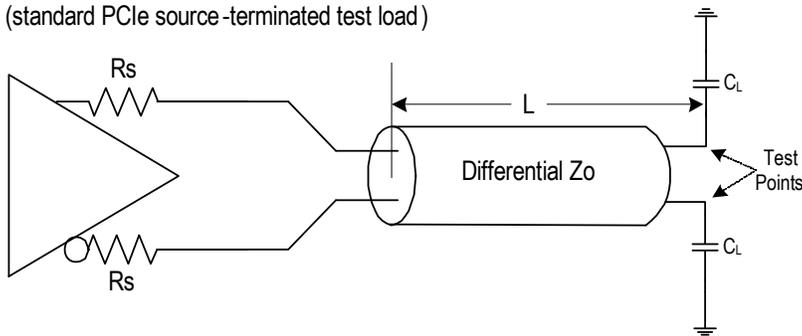


Table 13: Parameters for Low-Power HCSL Output Test Load

| Device | R_s (Ω) | Z_o (Ω) | L (inches) | C_L (pF) |
|------------|--------------------|--------------------|------------|------------|
| 9ZML123x | 27 | 85 | 12 | 2 |
| 9ZML123x | 33 | 100 | 12 | 2 |
| 9ZML125x * | Internal | 85 | 12 | 2 |
| 9ZML125x * | 7.5 | 100 | 12 | 2 |

* Contact factory for versions of this device with $Z_o=100\Omega$.

Alternate Terminations

The LP-HCSL can easily drive other logic families. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT’s “Universal” Low-Power HCSL Outputs”](#) for details.

Clock Periods

Table 14: Clock Periods – Differential Outputs with Spread Spectrum Disabled

| SSC On | Center Frequency MHz | Measurement Window | | | | | | | Units | Notes |
|--------|----------------------|--------------------------|---------------------------------|--------------------------------|----------------------|--------------------------------|---------------------------------|--------------------------|-------|-------|
| | | 1 Clock | 1µs | 0.1s | 0.1s | 0.1s | 1µs | 1 Clock | | |
| | | -c2jitter AbsPer Minimum | -SSC Short-Term Average Minimum | -ppm Long-Term Average Minimum | 0 ppm Period Nominal | +ppm Long-Term Average Maximum | +SSC Short-Term Average Maximum | +c2jitter AbsPer Maximum | | |
| DIF | 100.00 | 9.94900 | — | 9.99900 | 10.00000 | 10.00100 | — | 10.05100 | ns | 1,2,3 |

Table 15: Clock Periods – Differential Outputs with Spread Spectrum Enabled

| SSC On | Center Frequency MHz | Measurement Window | | | | | | | Units | Notes |
|--------|----------------------|--------------------------|---------------------------------|--------------------------------|----------------------|--------------------------------|---------------------------------|--------------------------|-------|-------|
| | | 1 Clock | 1µs | 0.1s | 0.1s | 0.1s | 1µs | 1 Clock | | |
| | | -c2jitter AbsPer Minimum | -SSC Short-Term Average Minimum | -ppm Long-Term Average Minimum | 0 ppm Period Nominal | +ppm Long-Term Average Maximum | +SSC Short-Term Average Maximum | +c2jitter AbsPer Maximum | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (+/-100ppm). The buffer itself does not contribute to ppm error.

³ Driven by SRC output of main clock, 100MHz PLL Mode or Bypass Mode.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | | | |
|-----------------------------|-----------|--------|----------------------|-----|
| Controller (Host) | | X Byte | IDT (Slave/Receiver) | |
| T | starT bit | | | |
| Slave Address | | | | |
| WR | WRite | | | |
| | | | | ACK |
| Beginning Byte = N | | | | |
| | | | | ACK |
| Data Byte Count = X | | | | |
| | | | | ACK |
| Beginning Byte N | | | | |
| | | | | ACK |
| O | | | | O |
| O | | | | O |
| O | | | O | |
| Byte N + X - 1 | | | | |
| | | | ACK | |
| P | stoP bit | | | |

9ZML1233E / 9ZML1253E SMBus Addressing

| SMB_A0_tri | SMBus Address (Read/Write bit = 0) |
|------------|------------------------------------|
| 0 | D8 |
| M | DA |
| 1 | DE |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | | |
|----------------------------|-----------------|--------|----------------------|-------------------|
| Controller (Host) | | X Byte | IDT (Slave/Receiver) | |
| T | starT bit | | | |
| Slave Address | | | | |
| WR | WRite | | | |
| | | | | ACK |
| Beginning Byte = N | | | | |
| | | | | ACK |
| RT | Repeat starT | | | |
| Slave Address | | | | |
| RD | ReaD | | | |
| | | | | ACK |
| | | | | Data Byte Count=X |
| | | | | ACK |
| | | | Beginning Byte N | |
| | | | O | |
| | | | O | |
| | | | O | |
| | | | Byte N + X - 1 | |
| N | Not acknowledge | | | |
| P | stoP bit | | | |

SMBus Table: PLL Mode and Frequency Select Register

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|---|------|---|---------------|---------|
| Bit 7 | PLL Mode bit [1] | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode table | | Latch |
| Bit 6 | PLL Mode bit [0] | PLL Operating Mode Rd back 0 | R | | | Latch |
| Bit 5 | SEL_A_B# | Input Select Readback | R | DIF_INB | DIF_INA | Real |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | PLL_InSEL_SW_EN | Enable S/W control of PLL BW and Input select | RW | Pin Control | SMBus Control | 0 |
| Bit 2 | PLL Mode bit [1] | PLL Operating Mode 1 | RW | See PLL Operating Mode table ¹ | | 1 |
| Bit 1 | PLL Mode bit [0] | PLL Operating Mode 1 | RW | | | 1 |
| Bit 0 | Reserved | | | | | 1 |

Note: Changing the PLL operating mode between HiBW or LoBW and Bypass mode or between Bypass mode and HiBW or LoBW requires a system reset. Changing the PLL operating mode between HiBW and LoBW or between LoBW and HiBW does not require a system reset.

SMBus Table: Output Disable Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|----------------------------------|------|---------|-------------|---------|
| Bit 7 | DIF_7_En | Output Control overrides OE# pin | RW | Low/Low | Pin Control | 1 |
| Bit 6 | DIF_6_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 5 | DIF_5_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 4 | DIF_4_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 3 | DIF_3_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 2 | DIF_2_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 1 | DIF_1_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | DIF_0_En | Output Control overrides OE# pin | RW | | | 1 |

SMBus Table: Output Control Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-----------|----------------------------------|------|---------|-------------|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | DIF_11_En | Output Control overrides OE# pin | RW | Low/Low | Pin Control | 1 |
| Bit 2 | DIF_10_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 1 | DIF_9_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | DIF_8_En | Output Control overrides OE# pin | RW | | | 1 |

SMBus Table: Reserved Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|---|---|---------|
| Bit 7 | | Reserved | | | | 0 |
| Bit 6 | | Reserved | | | | 0 |
| Bit 5 | | Reserved | | | | 0 |
| Bit 4 | | Reserved | | | | 0 |
| Bit 3 | | Reserved | | | | 0 |
| Bit 2 | | Reserved | | | | 0 |
| Bit 1 | | Reserved | | | | 0 |
| Bit 0 | | Reserved | | | | 0 |

SMBus Table: Reserved Register

| Byte 4 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|---|---|---------|
| Bit 7 | | Reserved | | | | 0 |
| Bit 6 | | Reserved | | | | 0 |
| Bit 5 | | Reserved | | | | 0 |
| Bit 4 | | Reserved | | | | 0 |
| Bit 3 | | Reserved | | | | 0 |
| Bit 2 | | Reserved | | | | 0 |
| Bit 1 | | Reserved | | | | 0 |
| Bit 0 | | Reserved | | | | 0 |

SMBus Table: Vendor & Revision ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|--------------|---|---------|
| Bit 7 | RID3 | REVISION ID | R | E rev = 0100 | | 0 |
| Bit 6 | RID2 | | R | | | 1 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 0 |
| Bit 3 | VID3 | VENDOR ID | R | — | — | 0 |
| Bit 2 | VID2 | | R | — | — | 0 |
| Bit 1 | VID1 | | R | — | — | 0 |
| Bit 0 | VID0 | | R | — | — | 1 |

SMBus Table: Device ID

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------------|------------------|------|----------------------------|---|---------|
| Bit 7 | Device ID 7 (MSB) | | R | 9ZML1233=ED 9ZML1253=FD | | 1 |
| Bit 6 | Device ID 6 | | R | | | 1 |
| Bit 5 | Device ID 5 | | R | | | 1 |
| Bit 4 | Device ID 4 | | R | | | X |
| Bit 3 | Device ID 3 | | R | | | 1 |
| Bit 2 | Device ID 2 | | R | | | 1 |
| Bit 1 | Device ID 1 | | R | | | 0 |
| Bit 0 | Device ID 0 | | R | | | X |

SMBus Table: Byte Count Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|---|------|---|---|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

SMBus Table: Output Skew Register A (when Input Clock A is selected)

| Byte 8 | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------------|--|------|---|---|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | I2O_FB_ASkew2 | Channel A Output delay programming (early) | RW | Binary value of number of VCO periods that outputs will be pulled earlier than input. | | 0 |
| Bit 1 | I2O_FB_ASkew1 | | RW | | | 0 |
| Bit 0 | I2O_FB_ASkew0 | | RW | | | 0 |

Note: For example, at 2.4GHz, each VCO period is 416.7ps and there are 24 VCO periods in a 100MHz output. Each write to bits [2:0] will pull the output a early by that number of VCO periods. Writing "110" 4 times would pull the output back in phase with the input. Writing "001" twice will accomplish the same result as writing "010" once - pulling the output 2 VCO periods earlier.

SMBus Table: Output Skew Register A (when Input Clock B is selected)

| Byte 9 | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------------|--|------|--|---|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | I2O_FB_BSkew2 | Channel B Output delay programming (early) | RW | Binary value of number of VCO periods that outputs will be earlier than input. Default is 0. | | 0 |
| Bit 1 | I2O_FB_BSkew1 | | RW | | | 0 |
| Bit 0 | I2O_FB_BSkew0 | | RW | | | 0 |

Note: For example, at 2.4GHz, each VCO period is 416.7ps and there are 24 VCO periods in a 100MHz output. Each write to bits [2:0] will pull the output a early by that number of VCO periods. Writing "110" 4 times would pull the output back in phase with the input. Writing "001" twice will accomplish the same result as writing "010" once - pulling the output 2 VCO periods earlier.

Package Drawings

Figure 2. 10 x 10 mm 72-VFQFPN – page 1

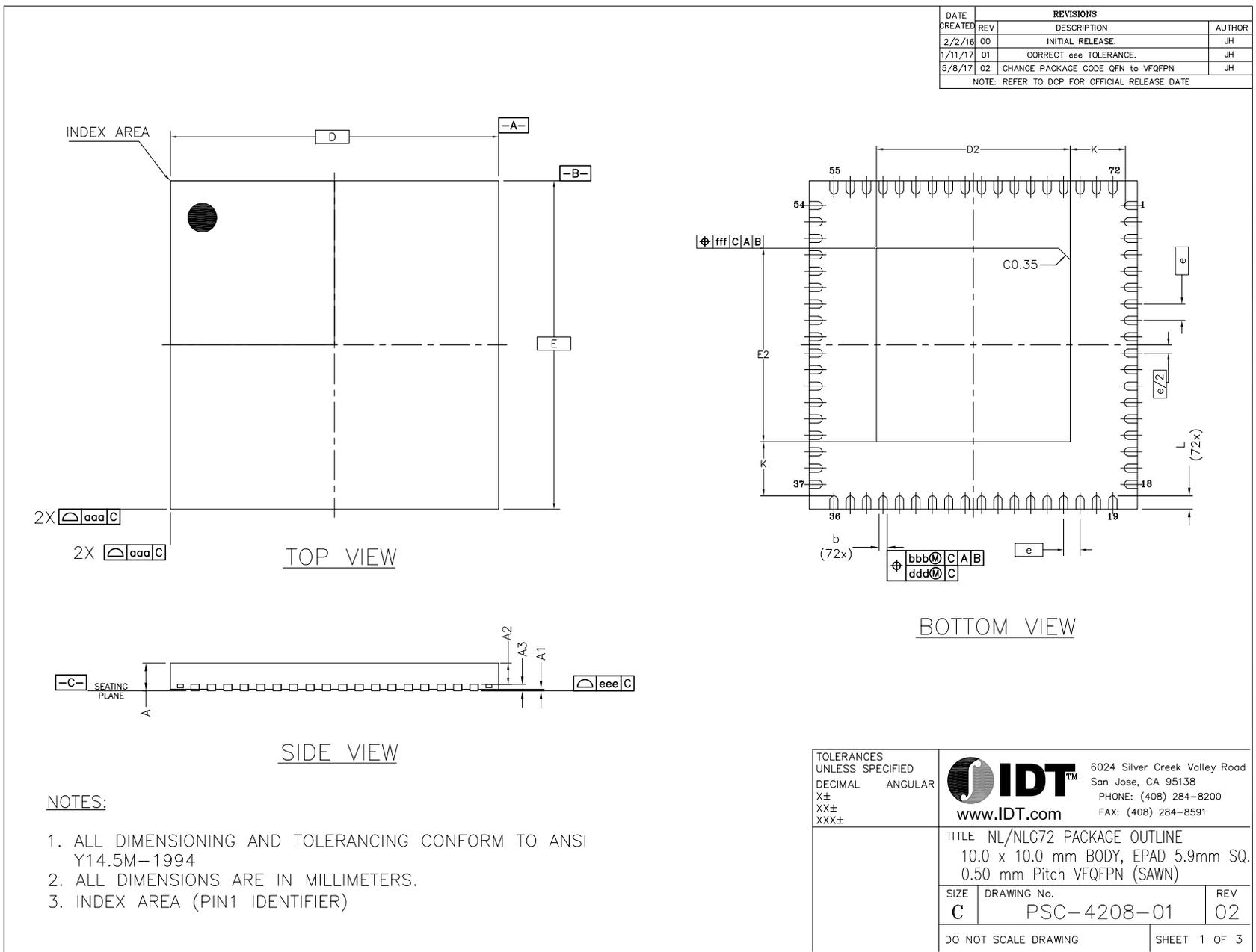


Figure 3. 10 x 10 mm 72-VFQFPN – page 2

| DATE | | REVISIONS | |
|---------|-----|-----------------------------------|--------|
| CREATED | REV | DESCRIPTION | AUTHOR |
| 2/2/16 | 00 | INITIAL RELEASE. | JH |
| 1/11/17 | 01 | CORRECT eee TOLERANCE. | JH |
| 5/8/17 | 02 | CHANGE PACKAGE CODE QFN to VFQFPN | JH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

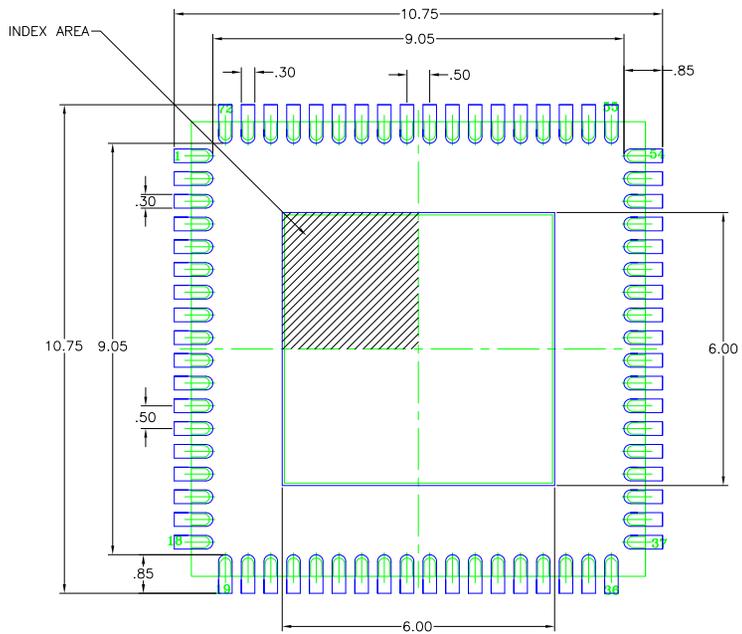
| SYMBOL | DIMENSIONS | | |
|------------|------------|------|------|
| | MIN. | NOM. | MAX. |
| D2 | 5.80 | 5.90 | 6.00 |
| E2 | 5.80 | 5.90 | 6.00 |
| A2 | 0.00 | 0.65 | 1.00 |
| L | 0.30 | 0.40 | 0.50 |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 ref. | | |
| b | 0.18 | 0.25 | 0.30 |
| Ⓢ | 0.50 BSC | | |
| D | 10.00 BSC | | |
| E | 10.00 BSC | | |
| K | 1.65 ref. | | |
| TOLERANCES | | | |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

| | | |
|--|---|--------------|
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± XX± XXX± | 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 | |
| | www.IDT.com | |
| TITLE NL/NLG72 PACKAGE OUTLINE 10.0 x 10.0 mm BODY, EPAD 5.9mm SQ. 0.50 mm Pitch VFQFPN (SAWN) | | |
| SIZE | DRAWING No. | REV |
| C | PSC-4208-01 | 02 |
| DO NOT SCALE DRAWING | | SHEET 2 OF 3 |

Figure 4. 10 x 10 mm 72-VFQFPN – page 3

| DATE | | REVISIONS | | |
|---------|-----|-----------------------------------|--|--------|
| CREATED | REV | DESCRIPTION | | AUTHOR |
| 2/2/16 | 00 | INITIAL RELEASE. | | JH |
| 1/11/17 | 01 | CORRECT eee TOLERANCE. | | JH |
| 5/8/17 | 02 | CHANGE PACKAGE CODE QFN to VFQFPN | | JH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X±
XX±
XXX±



6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE NL/NLG72 PACKAGE OUTLINE
10.0 x 10.0 mm BODY, EPAD 5.9mm SQ.
0.50 mm Pitch VFQFPN (SAWN)

| | | |
|------|-------------|-----|
| SIZE | DRAWING No. | REV |
| C | PSC-4208-01 | 02 |

DO NOT SCALE DRAWING SHEET 3 OF 3

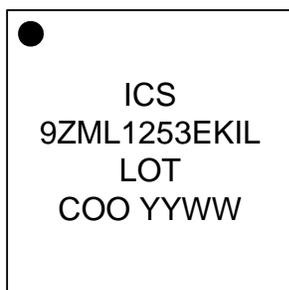
Ordering Information

| Orderable Part Number | Package | Carrier Type | Temperature |
|-----------------------|-----------------------------------|---------------|---------------|
| 9ZML1233EKILF | 10 x 10 mm, 0.5mm pitch 72-VFQFPN | Tray | -40° to +85°C |
| 9ZML1233EKILFT | 10 x 10 mm, 0.5mm pitch 72-VFQFPN | Tape and Reel | -40° to +85°C |
| 9ZML1253EKILF | 10 x 10 mm, 0.5mm pitch 72-VFQFPN | Tray | -40° to +85°C |
| 9ZML1253EKILFT | 10 x 10 mm, 0.5mm pitch 72-VFQFPN | Tape and Reel | -40° to +85°C |

“LF” designates PB-free configuration, RoHS compliant.

“E” is the device revision designator (will not correlate with the datasheet revision).

Marking Diagrams



1. “L” denotes RoHS compliant package.
2. “LOT” denotes the lot number.
3. “COO” denotes country of origin.
4. “YYWW” denotes the last two digits of the year and week the part was assembled.

Revision History

| Revision Date | Description of Change |
|------------------|---|
| December 1, 2017 | Removed “5V tolerant” reference in pins 13 and 14 descriptions. |
| May 19, 2017 | Corrected typos in orderable part numbers. |
| May 11, 2017 | <ul style="list-style-type: none"> ▪ Updated package outline drawings to latest version. ▪ Updated Byte 6 IDs. |
| April 27, 2017 | <ul style="list-style-type: none"> ▪ Updated Phase Jitter, PLL Mode IF-UPI typical and maximum values. |
| April 21, 2017 | <ul style="list-style-type: none"> ▪ Update Features and Key Specifications. ▪ Updated PCIe Common Clocked, PCIe Separate Clocked, and QPI/UPI to latest format, added IF-UPI spec to QPI/UPI tables. ▪ Updated Test Loads drawing to latest version. ▪ Corrected SMBus Addressing table for 1233/1253. |
| April 11, 2017 | <ul style="list-style-type: none"> ▪ Reverted back to original Device ID Scheme, byte 6 updated accordingly: 9ZML1233=ED 9ZML1253=FD |
| January 31, 2017 | Initial release. |



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

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