General Description

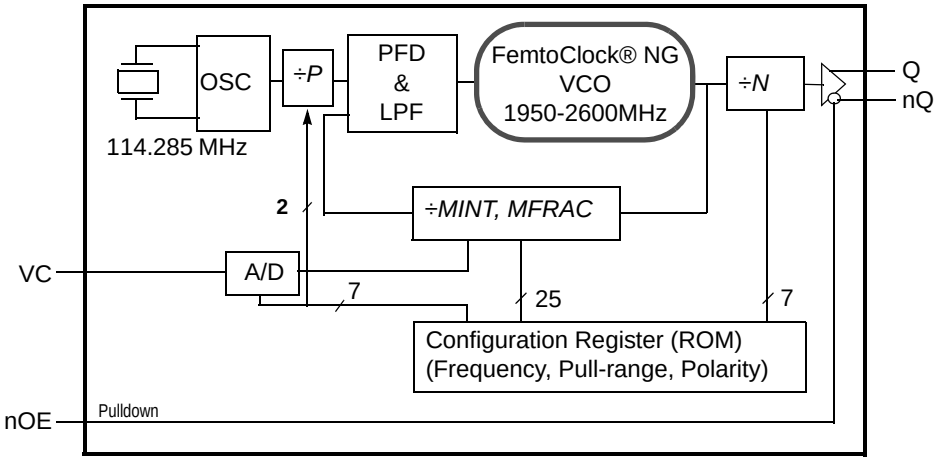
The IDT8CA3V76-0137 is a single output (155.52MHz) LVPECL VCXO. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance and (<0.5 ps RMS 12kHz - 20MHz). The device accepts 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

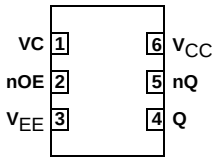
Features

- Fourth generation FemtoClock® NG technology
- Output Frequency 155.52MHz
- VCXO Absolute Pull Range (APR) ±200ppm
- One 3.3V LVPECL clock output
- Output enable control input, LVCMOS/LVTTL compatible
- RMS phase jitter @ 155.52MHz (12kHz - 20MHz): 0.5ps (typical)
- RMS phase jitter @ 155.52MHz (1kHz - 40MHz): 0.9ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package

Block Diagram



Pin Assignment



IDT8CA3V76-0137
6-lead ceramic 5mm x 7mm x 1.55mm package body
CD Package
Top View

Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	VC	Input		VCXO Control Voltage input.
2	nOE	Input	Pulldown	Output enable pin. See Table 3 for function. LVCMOS/LVTTL interface levels.
3	V_{EE}	Power		Negative power supply.
4, 5	Q, nQ	Output		Differential clock output. LVPECL interface levels.
6	V_{CC}	Power		Power supply pin.

NOTE: *Pulldown* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	nOE			5.5		pF
		VC			10		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ

Function Tables

Table 3. nOE Configuration

Input	
nOE	**Output Enable**
0 (default)	Q, nQ outputs are enabled
1	Q, nQ outputs are in high-impedance state

Principles of Operation

The IDT8CA3V76-0137 uses a fractional feedback-divider synthesizer core with a Delta-Sigma modulator for noise shaping and is very robust in its frequency synthesis capability. The output frequency is synthesized from an internal 114.285MHz third overtone crystal in order to minimize phase noise generation by frequency multiplication. The higher frequency reference crystal also allows more efficient “shaping” of noise by the Delta-Sigma modulator. The device contains a 25-bit PLL feedback divider with a 2-bit pre-scaler(P), a 7-bit integer portion (MINT), a 18-bit fractional portion (MFRAC) and a 7-bit output divider (N) for high-resolution frequency generation. The resolution (frequency increment for one MFRAC increment) is equal to 114.285MHz ÷ (2^{18} · N) or 435.9Hz ÷ N (N = 2 to 126).

This device is a digital VCXO. In a traditional, “analog” VCXO, variation of the output frequency is achieved by “pulling” the resonant frequency of the crystal. A digital VCXO operates with a fixed crystal frequency. Variation of the output frequency is achieved by modifying the fractional portion (MFRAC) of the PLL feedback loop divider. A fixed-frequency crystal features a comparatively higher Q factor than a pullable crystal, which enables better phase-noise performance.

The operating frequency and pull range of the 8CA3V76-0137 are factory-programmed by IDT to a center frequency of 155.52 MHz and a pull range of +/- 237 MHz. The data given in this datasheet are valid for this particular programming only.

More devices with different programming are available on request. Please refer to the FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information document and/or contact IDT.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I Other Inputs	 -0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	41.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current				148	mA

Table 4B. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.3		V_{CC} – 0.8	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V

Table 4C. LVCMOS/LVTTL DC Characteristic, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = V_{IN} = 3.465V	-0.3		0.8	V
			V_{CC} = V_{IN} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	nOE	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	nOE	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

AC Electrical Characteristics

Table 5A. VCXO Control Voltage Input (V_C) Characteristics, V_{CC} = 3.3V ± 5% , V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
K_V	Oscillator Gain, NOTE 1, 2,	V_{CC} = 3.3V	503.81	524.60	552.14	ppm/V
L_{VC}	Control Voltage Linearity; NOTE 4	BSL Variation	-1	±0.1	+1	%
BW	Modulation Bandwidth			100		kHz
Z_{VC}	VC Input Impedance			500		kΩ
VC_{NOM}	Nominal Control Voltage			V_{CC}/2		V
V_C	Control Voltage Tuning Range; NOTE 3		0		V_{CC}	V

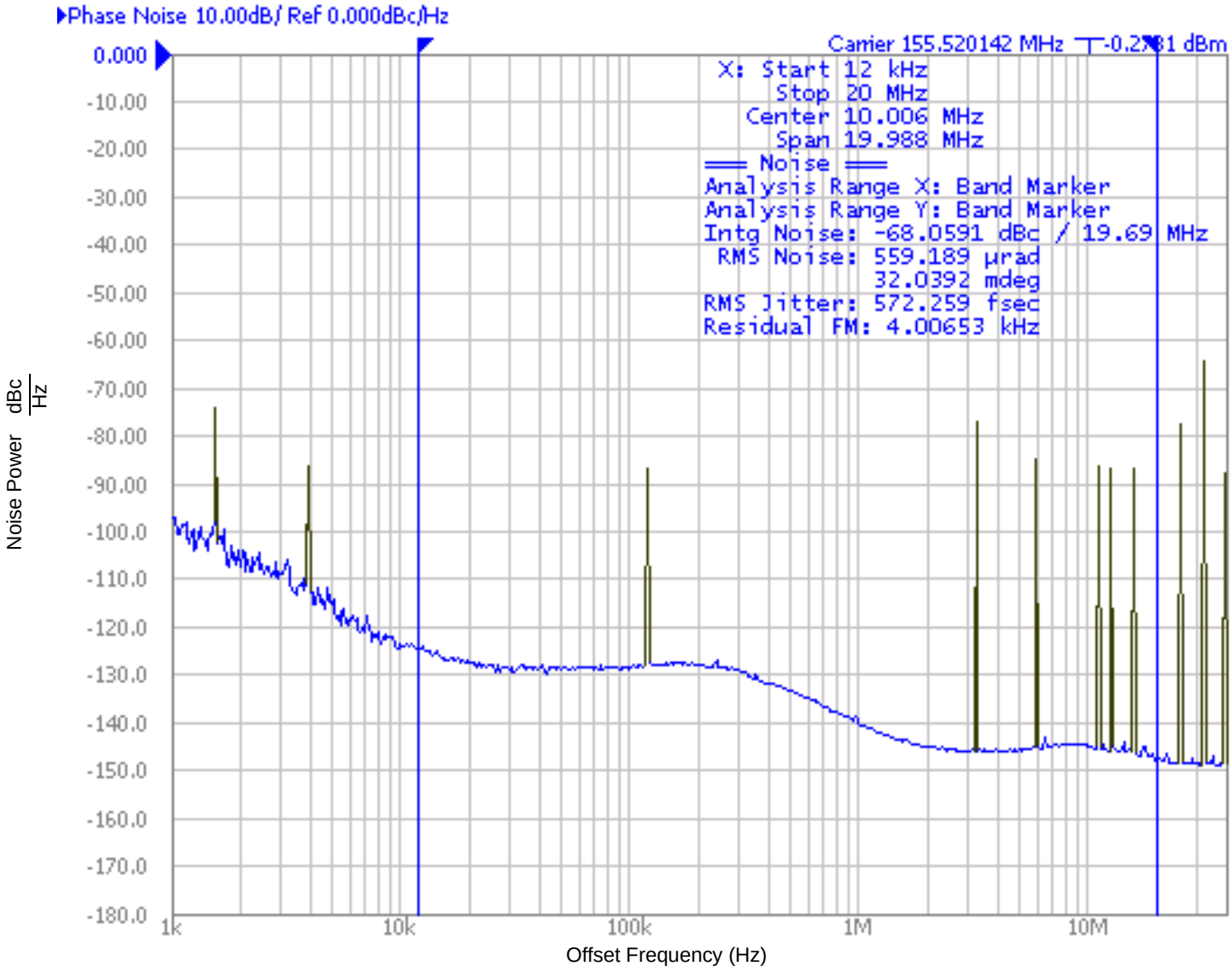
NOTE 1: V_C = 0V to V_{CC}.
NOTE 2: For best phase noise performance, use the lowest K_V that meets the requirements of the application.
NOTE 3: BSL = Best Straight Line Fit: Variation of the output frequency vs. control voltage V_C, in percent. V_C ranges from 10% to 90% V_{CC}.

Table 5B. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

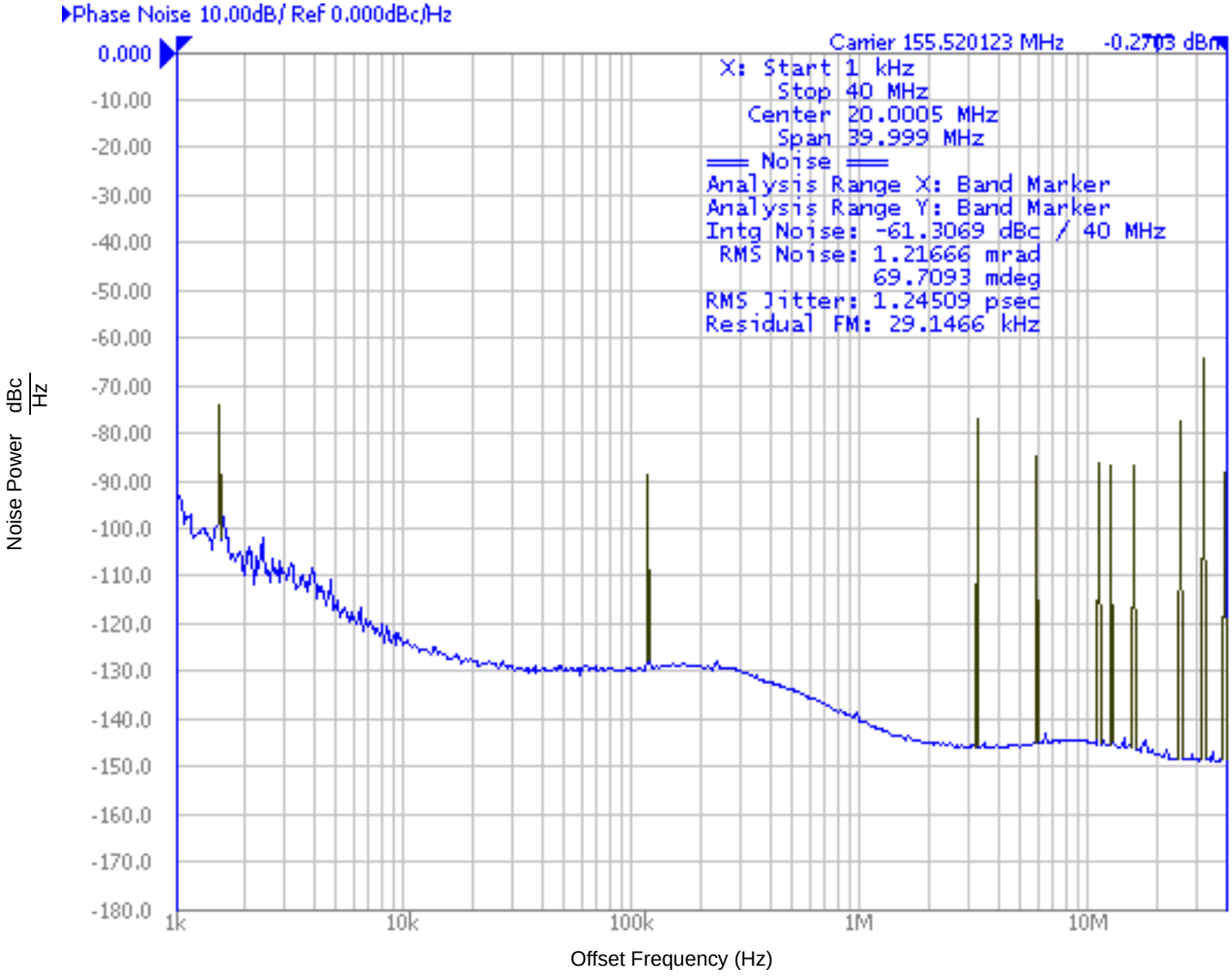
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Q, nQ			155.52		MHz
f_I	Initial Accuracy	Measured @ 25°C, $V_C = V_{CC}/2$			±10	ppm
f_S	Temperature Stability	Option code = E			±50	ppm
f_A	Aging	Frequency drift over 10 year life			±3	ppm
		Frequency drift over 15 year life			±5	ppm
f_T	Total Stability	Option code E (10 year life)			±63	ppm
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			7	13	ps
*t*jit(per)	Period Jitter; NOTE 1				4.0	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	155.52MHz, Integration Range: 12kHz - 20MHz		0.5	0.65	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	155.52MHz, Integration Range: 1kHz - 40MHz		0.87	1.30	ps
$\Phi_N(100)$	Single-side band phase noise, 100Hz from Carrier	155.52MHz		-70		dBc/Hz
$\Phi_N(1k)$	Single-side band phase noise, 1kHz from Carrier	155.52MHz		-110		dBc/Hz
$\Phi_N(10k)$	Single-side band phase noise, 10kHz from Carrier	155.52MHz		-124		dBc/Hz
$\Phi_N(100k)$	Single-side band phase noise, 100kHz from Carrier	155.52MHz		-128		dBc/Hz
$\Phi_N(1M)$	Single-side band phase noise, 1MHz from Carrier	155.52MHz		-142		dBc/Hz
$\Phi_N(10M)$	Single-side band phase noise, 10MHz from Carrier	155.52MHz		-145		dBc/Hz
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		400	ps
PSNR	Power Supply Noise Rejection	50mV Sinusoidal Noise 1kHz - 50MHz		-58		dbc
odc	Output Duty Cycle		48		52	%
$t_{STARTUP}$	Device startup time after power up				20	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Refer to the phase noise plot.

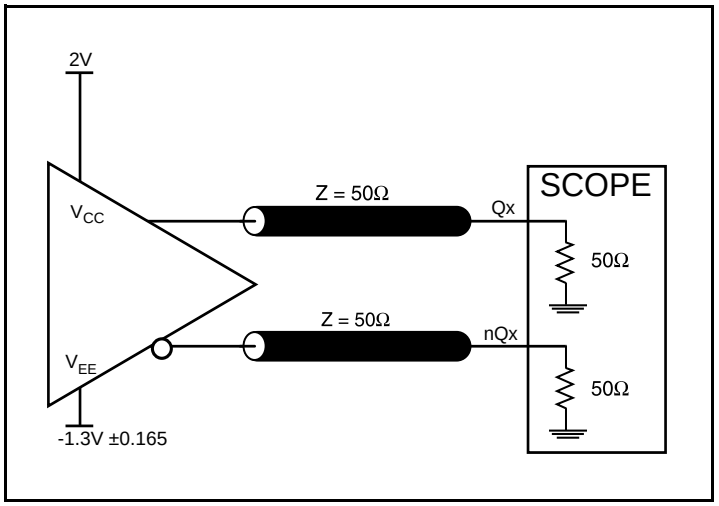
Typical phase noise, integration range of 12kHz - 20 MHz



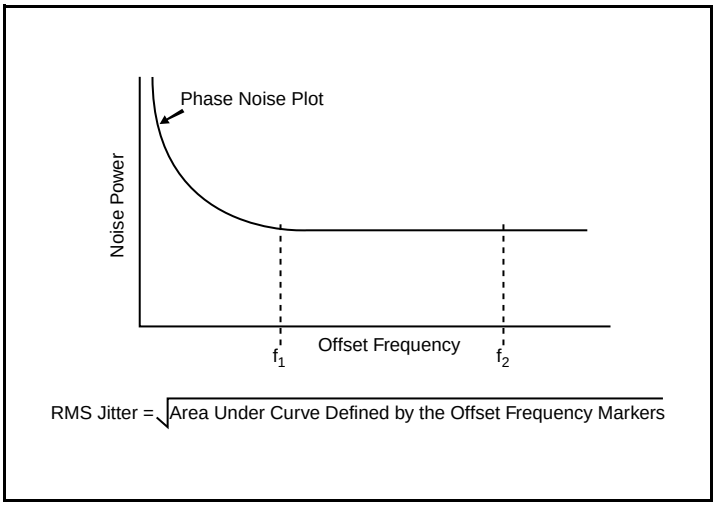
Typical phase noise, integration range of 1kHz - 40MHz



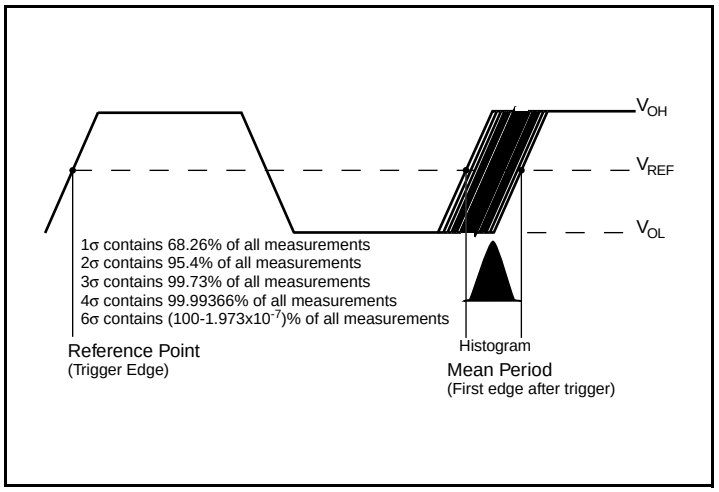
Parameter Measurement Information



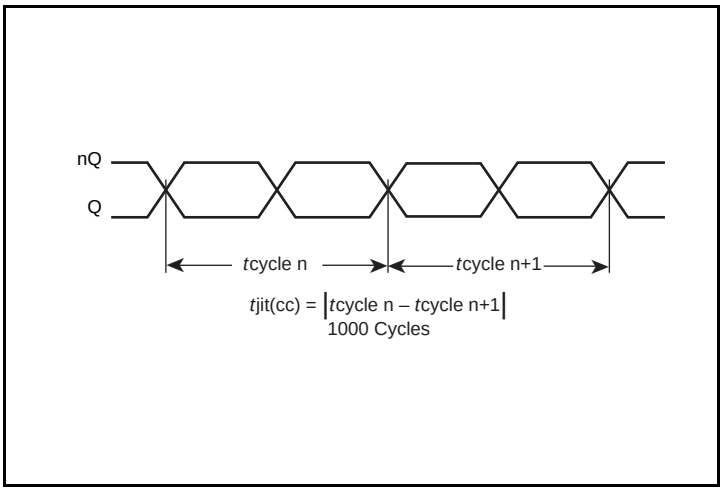
3.3V LVPECL Output Load AC Test Circuit



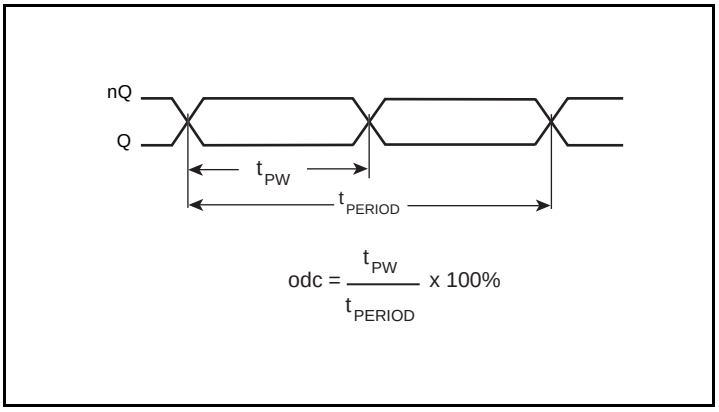
RMS Phase Jitter



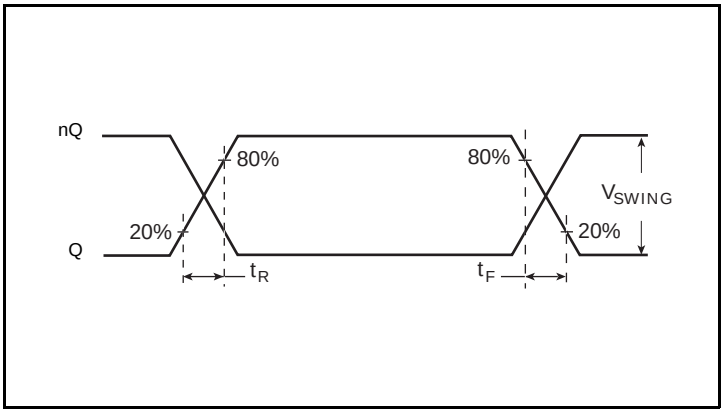
Period Jitter



Cycle-to-Cycle Jitter



LVPECL Output Duty Cycle



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

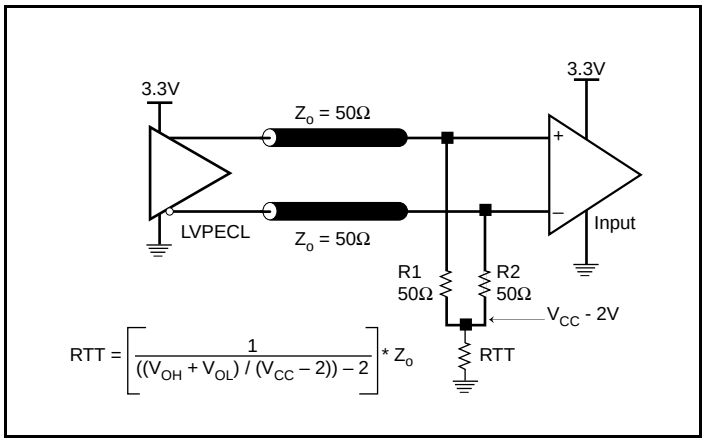


Figure 1A. 3.3V LVPECL Output Termination

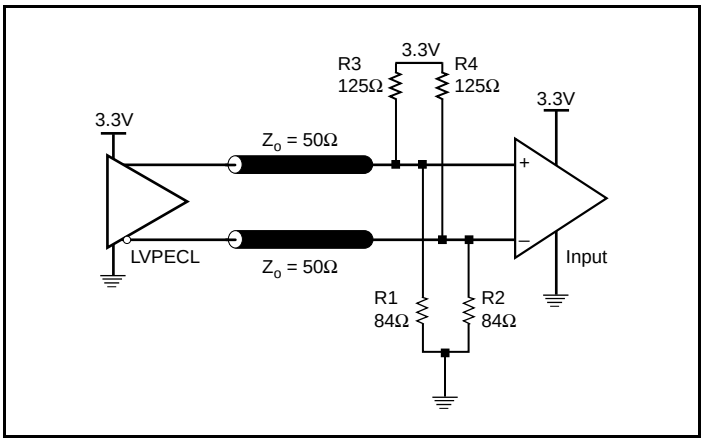


Figure 1B. 3.3V LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8CA3V76-0137.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8CA3V76-0137 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 480mA = **512.82mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 512.82mW + 32mW = **544.82mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 41.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.545W * 41.4°C/W = 107.56°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for a 6-lead Ceramic 5mm x 7mm Package

θ_{JA} **vs. Air Flow**	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	41.4°C/W

NOTE: For proper thermo dissipation, the PCB layout for the pin pad should be at minimum equal the package pin dimensions. The solder reflow specification should be that the entire pad is covered.

Reliability Information

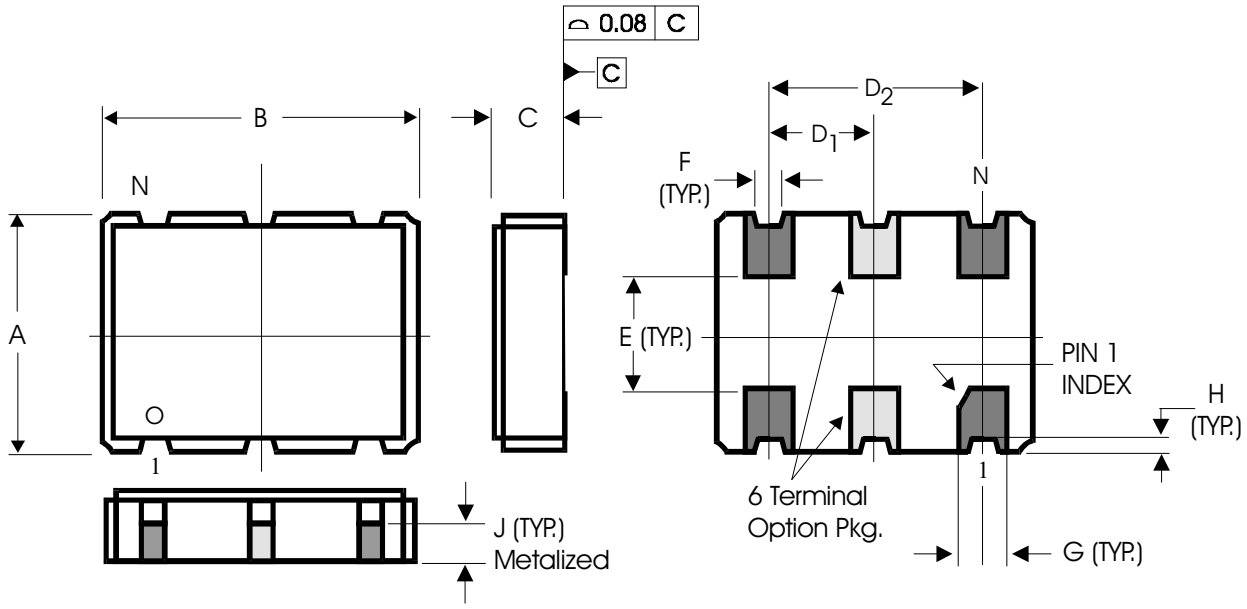
Table 7. θ_{JA} vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package

	θ_{JA} vs. Air Flow
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	41.4°C/W

Transistor Count

The transistor count for IDT8CA3V76-0137 is: 47,414

Package Outline and Package Dimensions



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	4.85	5.00	5.15
B	6.85	7.00	7.15
C	1.35	1.50	1.65
D_1	2.41	2.54	2.67
D_2	4.95	5.08	5.21
E	2.47	2.6	2.73
F	0.47	0.60	0.73
G	1.27	1.40	1.53
H	-	0.15 Ref.	-
J	-	0.65 Ref.	-

Table 8. Device Marking

	Industrial Temperature Range (T_A = -40°C to 85°C)	Commercial Temperature Range (T_A = 0°C to 70°C)
Marking	IDT8N3SV76EC-0137CDI	IDT8N3SV76EC-0137CD

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