FemtoClock® Zero Delay Buffer/ Clock Generator for PCI Express™ and Ethernet

ICS8714008I

DATASHEET

General Description

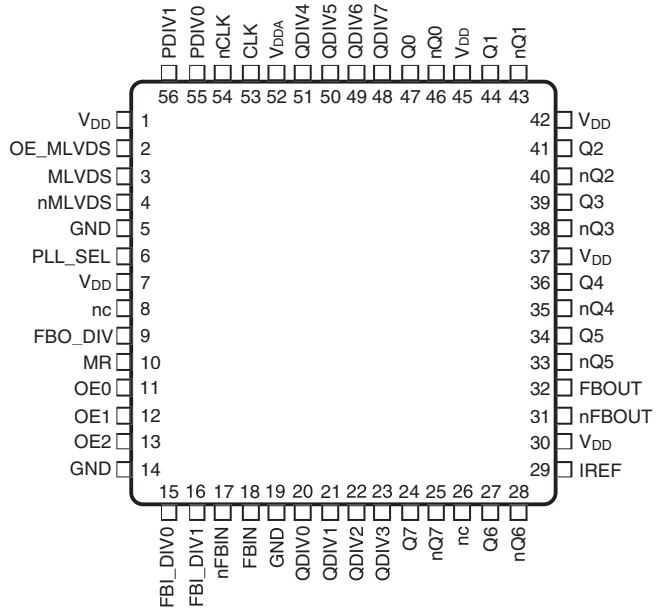
The ICS8714008I is Zero-Delay Buffer/Frequency Multiplier with eight differential HCSL output pairs, and uses external feedback (differential feedback input and output pairs) for “zero delay” clock regeneration. In PCI Express and Ethernet applications, 100MHz and 125MHz are the most commonly used reference clock frequencies and each of the eight output pairs can be independently set for either 100MHz or 125MHz. With an output frequency range of 98MHz to 165MHz, the device is also suitable for use in a variety of other applications such as Fibre Channel (106.25MHz) and XAUI (156.25MHz). The M-LVDS Input/Output pair is useful in backplane applications when the reference clock can either be local (on the same board as the ICS8714008I) or remote via a backplane connector. In output mode, an input from a local reference clock applied to the CLK, nCLK input pins is translated to M-LVDS and driven out to the MLVDS, nMLVDS pins. In input mode, the internal M-LVDS driver is placed in High-impedance state using the OE_MLVDS pin and MLVDS, nMLVDS pin then becomes an input (e.g. from a backplane).

The ICS8714008I uses very low phase noise FemtoClock technology, thus making it ideal for such applications as PCI Express Generation 1, 2 and 3 as well as for Gigabit Ethernet, Fibre Channel, and 10 Gigabit Ethernet. It is packaged in a 56-VFQFN package (8mm x 8mm).

Features

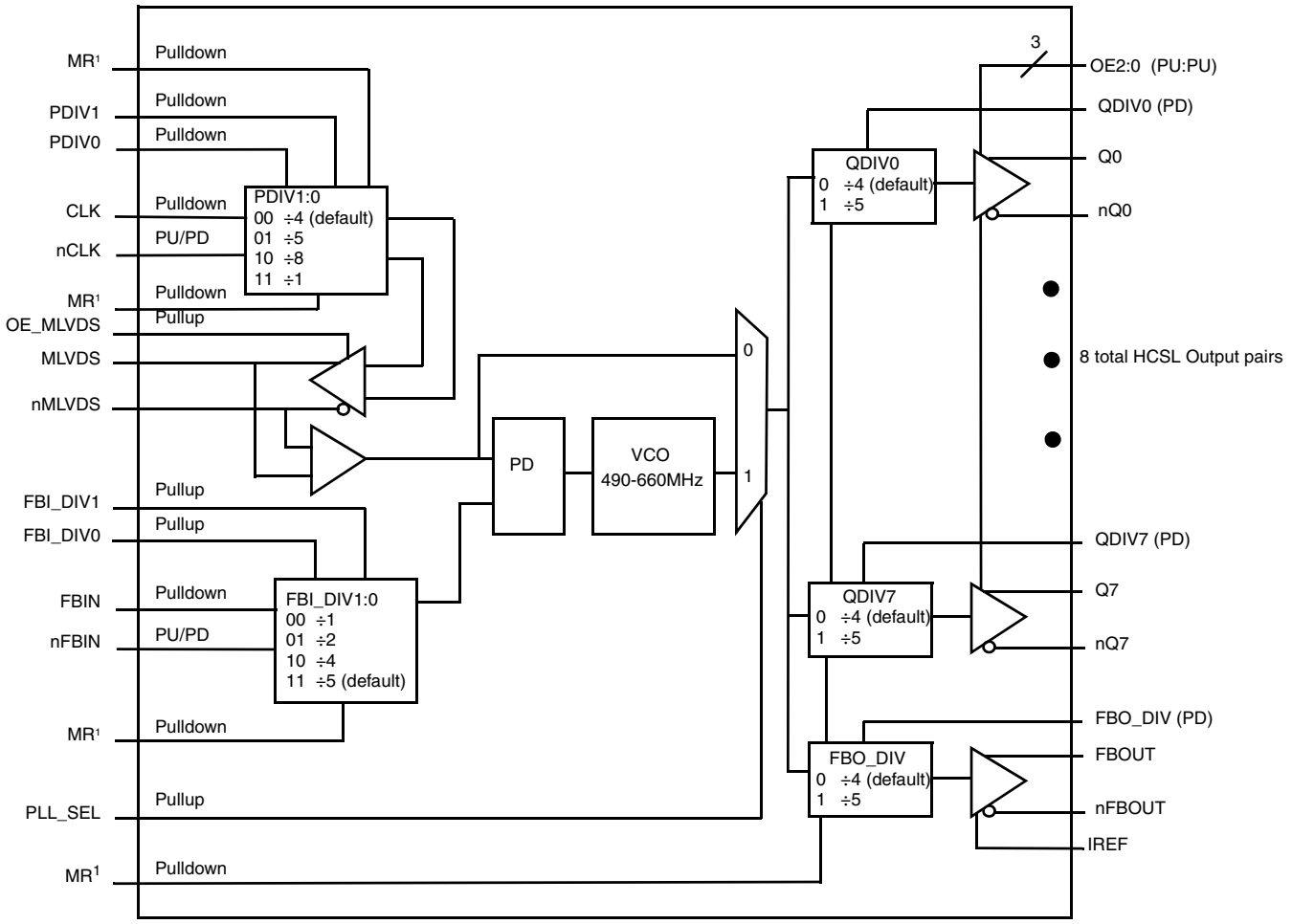
- Eight 0.7V differential HCSL output pairs, individually selectable for 100MHz or 125MHz for PCIe and Ethernet applications
- One differential clock input pair CLK, nCLK can accept the following differential input levels: LVPECL, LVDS, M-LVDS, LVHSTL, HCSL
- One M-LVDS I/O pair (MLVDS, nMLVDS)
- Output frequency range: 98MHz - 165MHz
- Input frequency range: 19.6MHz - 165MHz
- VCO range: 490MHz - 660MHz
- PCI Express (2.5 Gb/s), Gen 2 (5 Gb/s), and Gen 3 (8 Gb/s) jitter compliant
- External feedback for “zero delay” clock regeneration
- RMS phase jitter @ 125MHz (1.875MHz – 20MHz): 0.59ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHs 6) packaging

Pin Assignment



ICS8714008I
56-Lead VFQFN
8mm x 8mm x 0.925mm package body
4.5mm x 5.2mm ePad size
K Package
Top View

Block Diagram



[1]One Master Reset pin (MR) is used to reset all the internal dividers, but the MR lines are not drawn as all tied together to reduce control line clutter, making the block diagram easier to read.

PU means internal pull-up resistor on pin (power-up default is HIGH if not externally driven)
PD means internal pull-down resistor on pin (power-up default is LOW if not externally driven)

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 7, 30, 37, 42, 45	V_{DD}	Power		Core supply pins.
2	OE_MLVDS	Input	Pullup	Active High Output Enable. When HIGH, the M-LVDS output driver is active and provides a buffered copy of reference clock applied the CLK, nCLK input to the MLVDS, nMLVDS output pins. The MLVDS, nMLVDS frequency equals the CLK, nCLK frequency divided by the PDIV Divider value (selectable ÷1, ÷4, ÷5, ÷8). When LOW, the M-LVDS output driver is placed into a High-impedance state and the MLVDS, nMLVDS pins can accept a differential input. LVCMOS/LVTTL interface levels.
3	MLVDS	I/O		Non-Inverting M-LVDS input/output. The input/output state is determined by the OE_MLVDS pin. When OE_MLVDS = HIGH, this pin is an output and drives the non-inverting M-LVDS output. When OE_MLVDS = LOW, this pin is an input and can accept the following differential input levels: M-LVDS, LVDS, LVPECL, HSTL, HCSL.
4	nMLVDS	I/O		Inverting M-LVDS input/output. The input/output state is determined by the OE_MLVDS pin. When OE_MLVDS = HIGH, this pin is an output and drives the inverting M-LVDS output. When OE_MLVDS = LOW, this pin is an input and can accept the following differential input levels: M-LVDS, LVDS, LVPECL, HSTL, HCSL.
5, 14, 19	GND	Power		Power supply ground.
6	PLL_SEL	Input	Pullup	PLL select. Determines if the PLL is in bypass or enabled mode (default). In enabled mode, the output frequency = VCO frequency/QDIV divider. In bypass mode, the output frequency = reference clock frequency/(PDIV *QDIV). LVCMOS/LVTTL interface levels.
8, 26	nc	Unused		No internal connection.
9	FBO_DIV	Input	Pulldown	Output Divider Control for the feedback output pair, FBOUT, nFBOUT. Determines if the output divider = ÷4 (default), or ÷5. Refer to Table 3D. LVCMOS/LVTTL interface levels.
10	MR	Input	Pulldown	Active High master reset. When logic HIGH, the internal dividers are reset causing all the true outputs Qx to drive High-impedance. Note that assertion of MR overrides the OE[2:0] control pins and all outputs are disabled. When logic LOW, the internal dividers are enabled and the state of the outputs are determined by OE[2:0]. MR must be asserted on power-up to ensure outputs phase aligned. LVCMOS/LVTTL interface levels.
11	OE0	Input	Pullup	Output Enable. Together with OE1 and OE2, determines the output state of the outputs with the default state: all output pairs switching. It should also be noted that the feedback output pins (FBOUT, nFBOUT) are always switching and are not affected by the state of OE[2:0]. Refer to Table 3B for truth table. LVCMOS/LVTTL Interface levels.
12	OE1	Input	Pullup	Output Enable. Together with OE0 and OE2, determines the output state of the outputs with the default state: all output pairs switching. It should also be noted that the feedback output pins (FBOUT, nFBOUT) are always switching and are not affected by the state of OE[2:0]. Refer to Table 3B for truth table. LVCMOS/LVTTL Interface levels.
13	OE2	Input	Pullup	Output Enable. Together with OE0 and OE1, determines the output state of the outputs with the default state: all output pairs switching. It should also be noted that the feedback output pins (FBOUT, nFBOUT) are always switching and are not affected by the state of OE[2:0]. Refer to table 3B for truth table. LVCMOS/LVTTL Interface levels.

Table 1. Pin Descriptions

Number	Name	Type		Description
15	FBI_DIV0	Input	Pullup	Feedback Input Divide Select 0. Together with FBI_DIV1, determines the feedback input divider value. Refer to Table 3C. LVCMOS/LVTTL interface levels.
16	FBI_DIV1	Input	Pullup	Feedback Input Divide Select 1. Together with FBI_DIV0, determines the feedback input divider value. Refer to Table 3C. LVCMOS/LVTTL interface levels.
17	nFBIN	Input	Pullup/ Pulldown	Inverted differential feedback input to phase detector for regenerating clocks with “Zero Delay.”
18	FBIN	Input	Pulldown	Non-inverted differential feedback input to phase detector for regenerating clocks with “Zero Delay.”
20	QDIV0	Input	Pulldown	Output Divider Control for Q0, nQ0. Refer to Table 3E. LVCMOS/LVTTL interface levels.
21	QDIV1	Input	Pulldown	Output Divider Control for Q1, nQ1. Refer to Table 3E. LVCMOS/LVTTL interface levels.
22	QDIV2	Input	Pulldown	Output Divider Control for Q2, nQ2. Refer to Table 3E. LVCMOS/LVTTL interface levels.
23	QDIV3	Input	Pulldown	Output Divider Control for Q3, nQ3. Refer to Table 3E. LVCMOS/LVTTL interface levels.
24, 25	Q7, nQ7	Output		Differential output pair. HCSL interface levels.
27, 28	Q6, nQ6	Output		Differential output pair. HCSL interface levels.
29	IREF	Input		An external fixed resistor from this pin to ground is needed to provide a reference current for the differential HCSL outputs. A resistor value of 475Ω provides an HCSL voltage swing of approximately 700mV.
31, 32	nFBOUT, FBOUT	Output		Differential feedback output pair. The feedback output pair always switches independent of the output enable settings on the OE[2:0] pins. HCSL interface levels.
33, 34	nQ5, Q5	Output		Differential output pair. HCSL interface levels.
35, 36	nQ4, Q4	Output		Differential output pair. HCSL interface levels.
38, 39	nQ3, Q3	Output		Differential output pair. HCSL interface levels.
40, 41	nQ2, Q2	Output		Differential output pair. HCSL interface levels.
43, 44	nQ1, Q1	Output		Differential output pair. HCSL interface levels.
46, 47	nQ0, Q0	Output		Differential output pair. HCSL interface levels.
48	QDIV7	Input	Pulldown	Output Divider Control for Q7, nQ7. Refer to Table 3E. LVCMOS/LVTTL interface levels.
49	QDIV6	Input	Pulldown	Output Divider Control for Q6, nQ6. Refer to Table 3E. LVCMOS/LVTTL interface levels.
50	QDIV5	Input	Pulldown	Output Divider Control for Q5, nQ5. Refer to Table 3E. LVCMOS/LVTTL interface levels.
51	QDIV4	Input	Pulldown	Output Divider Control for Q4, nQ4. Refer to Table 3E. LVCMOS/LVTTL interface levels.
52	V_{DDA}	Power		Analog supply pin.
53	CLK	Input	Pulldown	Non-inverting differential clock input. Accepts LVPECL, HCSL, LVDS, M-LVDS and HSTL input levels.

Table 1. Pin Descriptions

Number	Name	Type		Description
54	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Accepts LVPECL, HCSL, LVDS, M-LVDS and HSTL input levels.
55	PDIV0	Input	Pulldown	Input Divide Select 0. Together with PDIV1 determines the input divider value. Refer to Table 3F. LVCMOS/LVTTL Interface levels.
56	PDIV1	Input	Pulldown	Input Divide Select 1. Together with PDIV0 determines the input divider value. Refer to Table 3F. LVCMOS/LVTTL Interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Common Configuration Table (not exhaustive)[NOTE 1]

Input Frequency	Output Frequency	Application	Frequency Mult. Factor	PDIV	FBI_DIV	FBO_DIV	QDIVx
100MHz	100MHz	PCIe Buffer	1	÷1	÷1	÷5	÷5
125MHz	125MHz	PCIe, Ethernet Buffer	1	÷1	÷1	÷4	÷4
100MHz	125MHz	PCIe Multiplier	5/4	÷1	÷1	÷5	÷4
125MHz	100MHz	PCIe Divider	4/5	÷1	÷1	÷4	÷5
25MHz	100MHz	PCIe Multiplier	4	÷1	÷4	÷5	÷5
25MHz	125MHz	PCIe, Ethernet Multiplier	5	÷1	÷4	÷5	÷4
25MHz	156.25MHz	XAUI Multiplier	25/4	÷1	÷5	÷5	÷4
62.5MHz	125MHz	Ethernet Multiplier	2	÷1	÷2	÷4	÷4
53.125MHz	106.25MHz	Fibre Channel Multiplier	2	÷1	÷2	÷5	÷5

NOTE 1: This table shows more common configurations and is not exhaustive. When using alternate configurations, the designer must ensure the VCO frequency is always within its range of 490MHz – 660MHz.

Table 3B. Output Enable Truth Table

Inputs			State
OE2	**OE1**	**OE0**	**Q[0:7], nQ[0:7]**
0	0	0	Q0, nQ0 switching; Q[1:7], nQ[1:7] = High-impedance
0	0	1	Q[0:1], nQ[0:1] switching; Q[2:7], nQ[2:7] = High-impedance
0	1	0	Q[0:2], nQ[0:2] switching; Q[3:7], nQ[3:7] = High-impedance
0	1	1	Q[0:3], nQ[0:3] switching; Q[4:7], nQ[4:7] = High-impedance
1	0	0	Q[0:4], nQ[0:4] switching; Q[5:7], nQ[5:7] = High-impedance
1	0	1	Q[0:5], nQ[0:5] switching; Q[6:7], nQ[6:7] = High-impedance
1	1	0	Q[0:6], nQ[0:6] switching; Q7, nQ7 = High-impedance
1	1	1	All output pairs switching (default)

Table 3C. Feedback Input Divider Control Table

Inputs		
FBI_DIV1	FBI_DIV0	Feedback Input Divider Values
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷5 (default)

Table 3D. Feedback Output Divider Control Table

Inputs	
FBO_DIV	Feedback Output Divider Value
0	÷4 (default)
1	÷5

Table 3E. Output Divider Control Control Table

Inputs	
QDIV[7:0]	Output Divider Value
0	÷4 (default)
1	÷5

Table 3F. Input Divide Select Control Table

Inputs		
PDIV1	PDIV0	Input Divider Values
0	0	÷4 (default)
0	1	÷5
1	0	÷8
1	1	÷1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	26.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	Outputs Unloaded		170	210	mA
I_{DDA}	Analog Supply Current	Outputs Unloaded		11	15	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	MR, PDIV[1:0], QDIV[7:0], FBO_DIV	V_{DD} = V_{IN} = 3.465V			150	µA
		PLL_SEL, OE_MLVDS, FBI_DIV[1:0], OE[2:0]	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	MR, PDIV[1:0], QDIV[7:0], FBO_DIV	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_SEL, OE_MLVDS, FBI_DIV[1:0], OE[2:0]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK, FBIN, nFBIN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK, FBIN	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK, nFBIN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. M-LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		370	410	470	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		0.3	2.1	2.3	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5A. PCI Express Jitter Specifications, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	f = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		20	30	86	ps
		f = 125MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		12	25	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, High Band: 1.5MHz - Nyquist (clock frequency/2)		2	3	3.1	ps
		f = 125MHz, High Band: 1.5MHz - Nyquist (clock frequency/2)		0.8	1.4	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, Low Band: 10kHz - 1.5MHz		0.10	0.30	3.0	ps
		f = 125MHz, Low Band: 10kHz - 1.5MHz		0.10	0.25	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	f = 100MHz Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.5	0.7	0.8	ps
		f = 125MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.2	0.3	0.8	ps

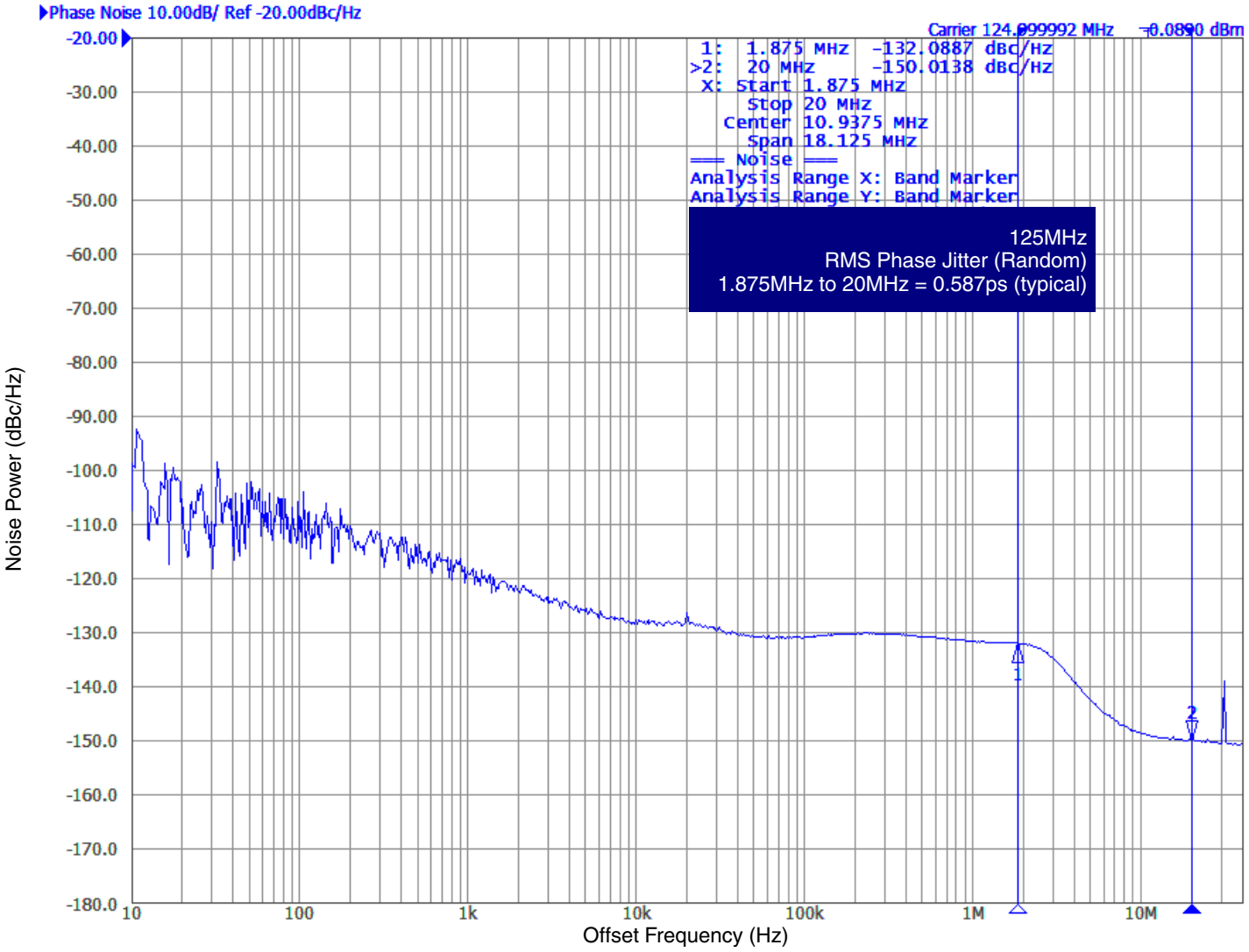
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 5B. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

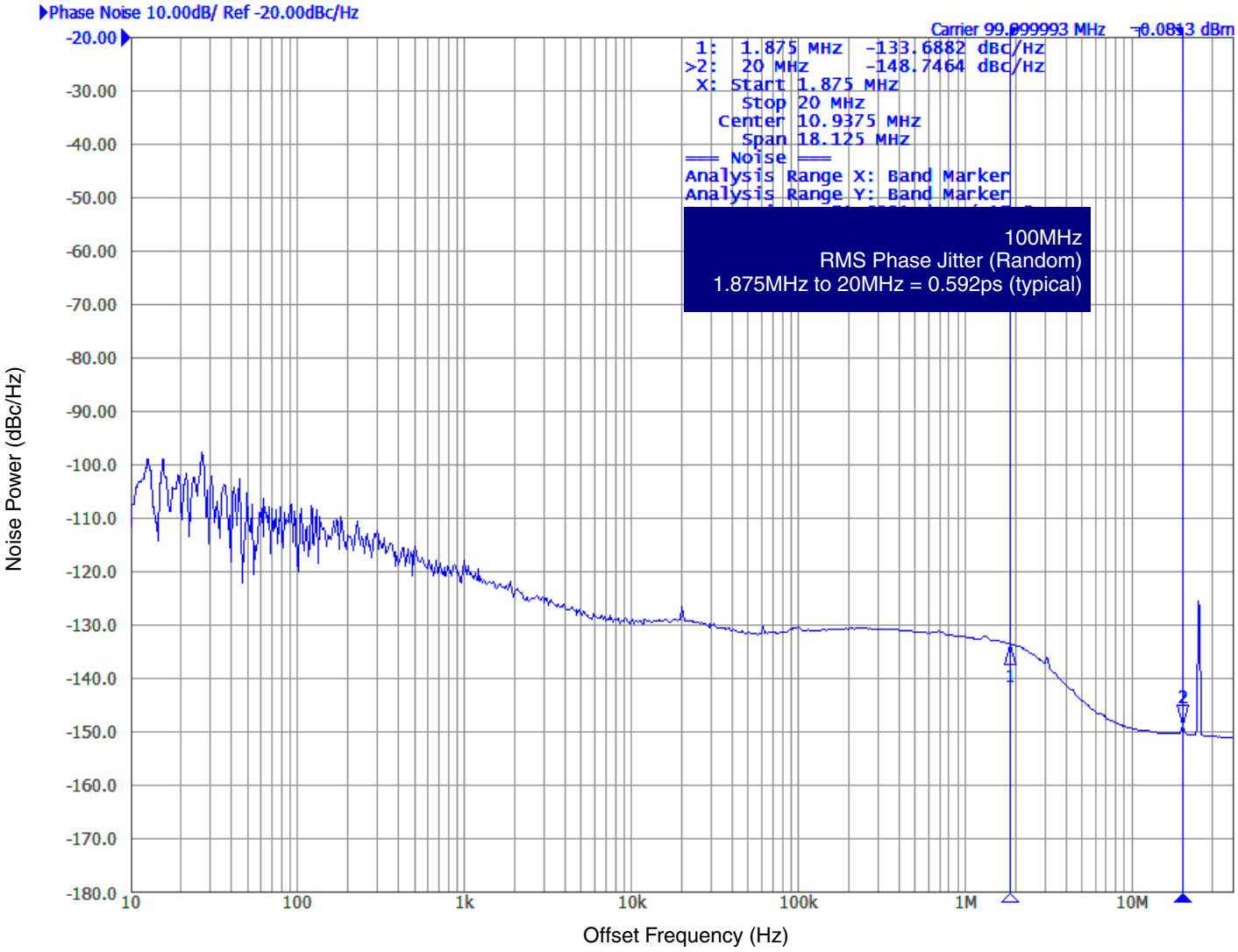
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		98		165	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			35	80	ps
*t*sk(o)	Output Skew; NOTE 1, 2	Outputs measured Q[0:7], nQ[0:7]		100	210	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3, 4	125MHz, Integration Range: 1.875MHz – 20MHz		0.587		ps
		100MHz, Integration Range: 1.875MHz – 20MHz		0.592		ps
t_L	PLL Lock Time				100	ms
V_{MAX}	Absolute Max Output Voltage; NOTE 5, 6				1150	mV
V_{MIN}	Absolute Min Output Voltage; NOTE 5, 7		-300			mV
V_{RB}	Ringback Voltage; NOTE 8, 9		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; NOTE 8, 9		500			ps
V_{CROSS}	Absolute Crossing Voltage; NOTE 5, 10, 11		150		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 5, 10, 12				140	mV
Rise/Fall Edge Rate	Rising/Falling Edge Rate; NOTE 8, 13	Measured between -150mV to +150mV	0.6		4	V/ns
odc	Output Duty Cycle; NOTE 14		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. Characterized with configurations in Table 3A.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: Refer to the Phase Noise plots.
NOTE 4: Measurements depend on input source used.
NOTE 5: Measurement taken from single-ended waveform.
NOTE 6: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 7: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 8: Measurement taken from a differential waveform.
NOTE 9: t_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range. See Parameter Measurement Information Section.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 12: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.
NOTE 14: Input duty cycle must be 50%.

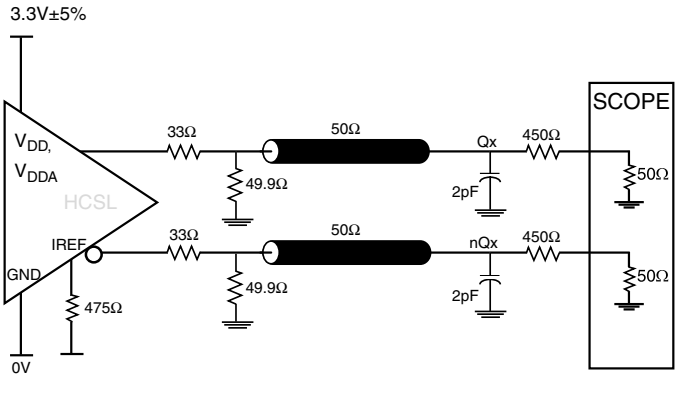
Typical Phase Noise at 125MHz



Typical Phase Noise at 100MHz

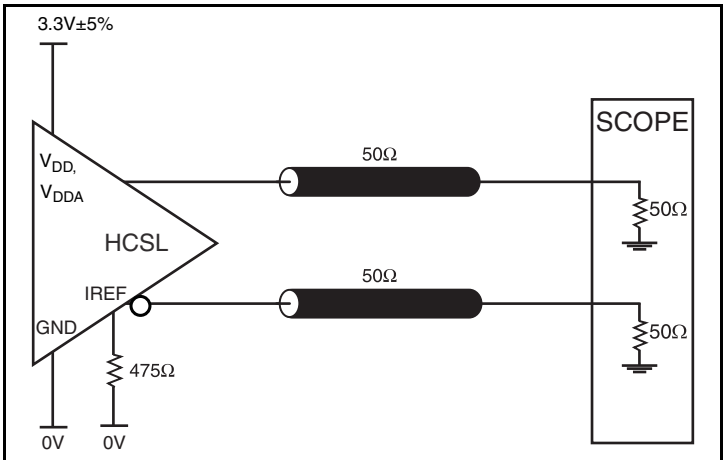


Parameter Measurement Information



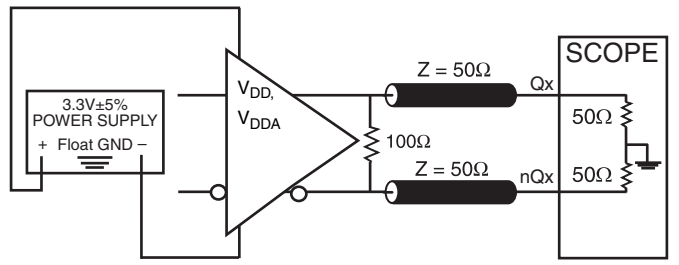
This load condition is used for V_{MAX}, V_{MIN}, V_{RB}, t_{STABLE}, V_{CROSS}, ΔV_{CROSS} and Rise/Fall Edge Rate measurements.

3.3V HCSL Output Load Test Circuit

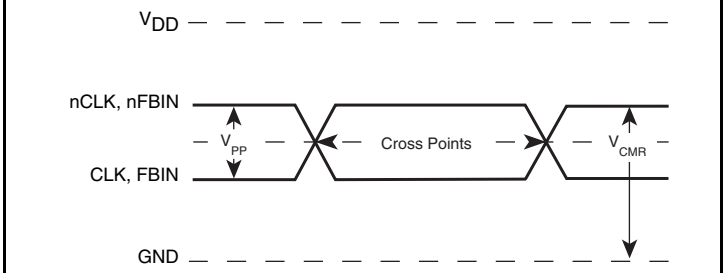


This load condition is used for tjit(cc), tjit(Ø) and tsk(o) measurements.

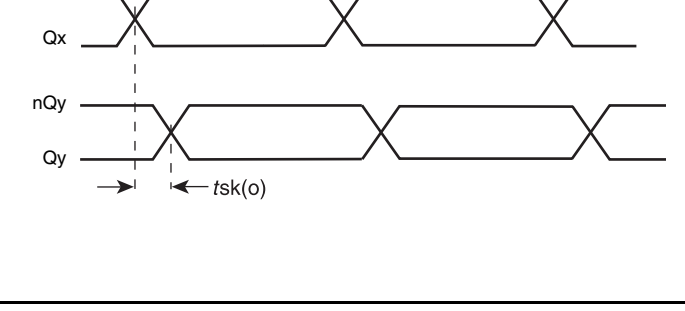
3.3V HCSL Output Load Test Circuit



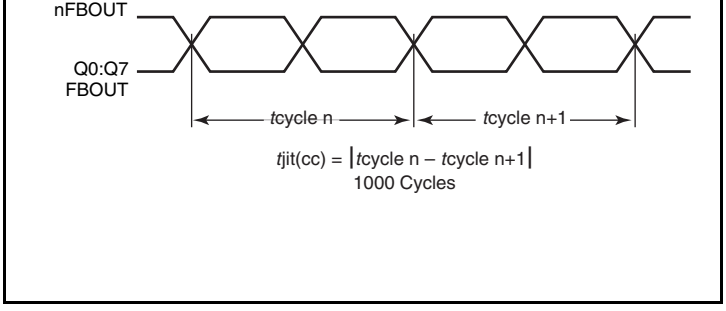
3.3V M-LVDS Output Load Test Circuit



Differential Input Level

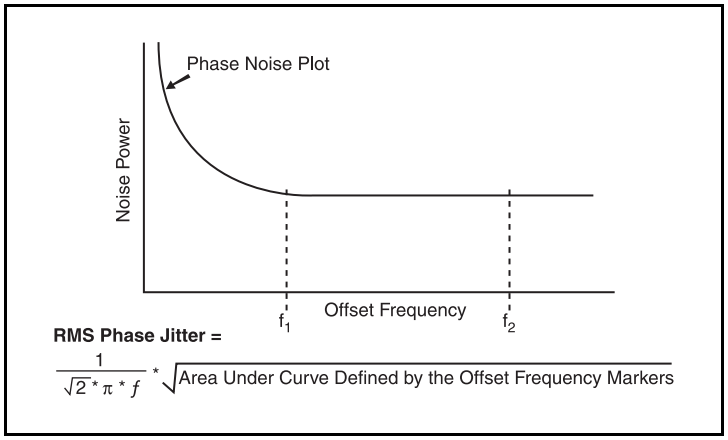


Output Skew

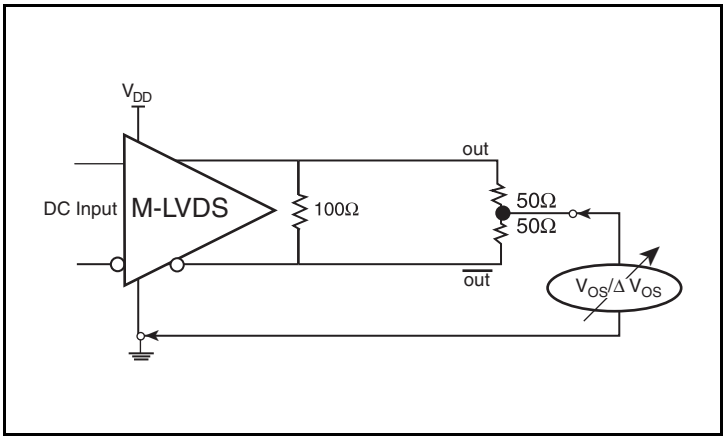


Cycle-to-Cycle Jitter

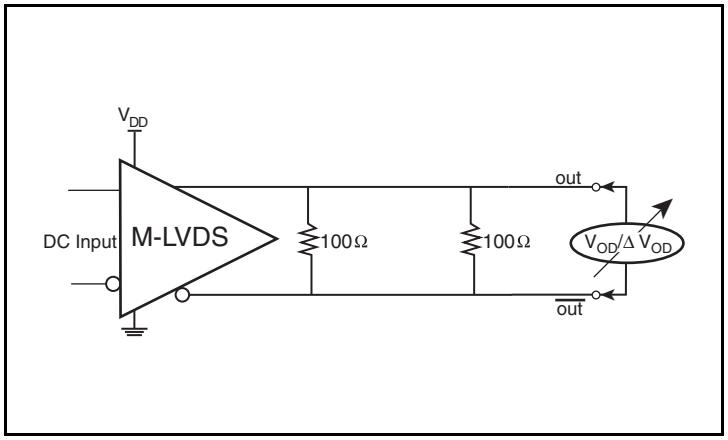
Parameter Measurement Information, continued



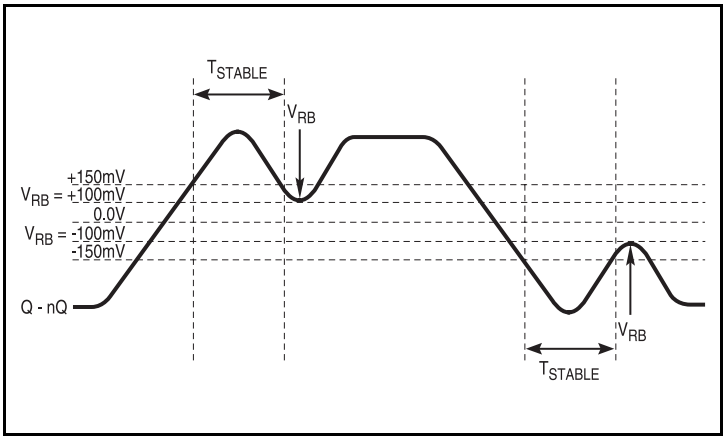
RMS Phase Jitter



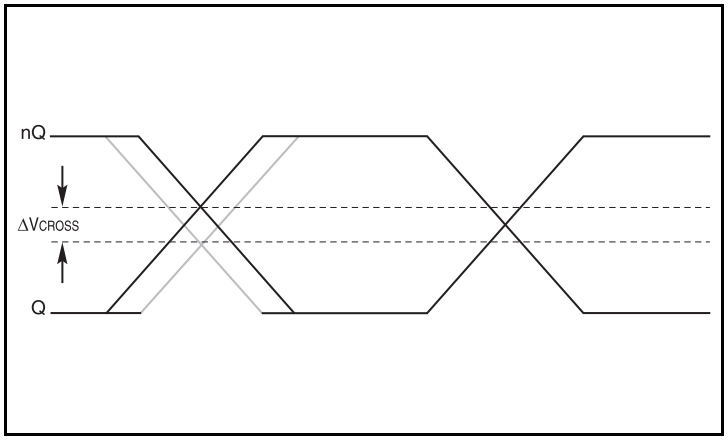
M-LVDS Offset Voltage Setup



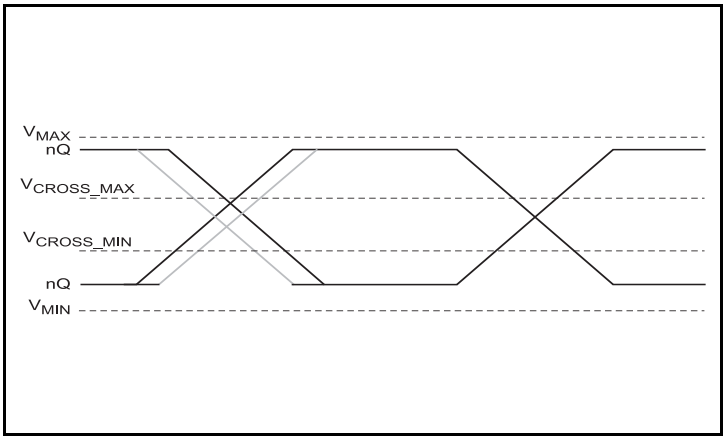
M-LVDS Differential Output Voltage Setup



Differential Measurement Points for Ringback

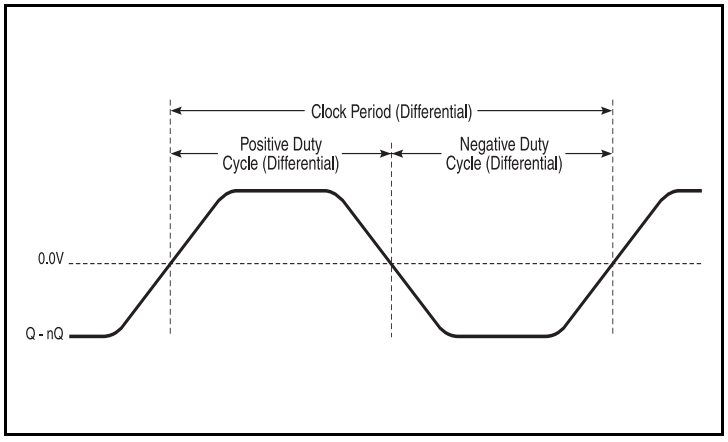


Single-ended Measurement Points for Delta Cross Point

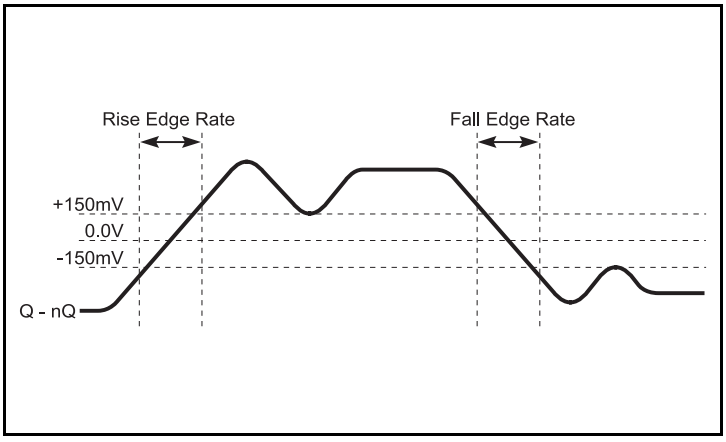


Single-ended Measurement Points for Absolute Cross Point/Swing

Parameter Measurement Information, continued



Differential Measurement Points for Duty Cycle/Period



Differential Measurement Points for Rise/Fall Time

Applications Information

Overview

The is a high performance FemtoClock Zero Delay Buffer/ Multiplier/Divider which uses external feedback for accurate clock regeneration and low static and dynamic phase offset. It can be used in a number different ways:

- Backplane clock multiplier. Many backplane clocks are relatively low frequency because of heavy electrical loading. The ICS8714008I can multiply a low frequency backplane clock (e.g. 25MHz) to an appropriate reference clock frequency for PCIe, Ethernet, 10G Ethernet: 100MHz, 125MHz, 156.25MHz. The device can also accept a high frequency local reference (100MHz or 125MHz, for example) and divide the frequency down to 25MHz M-LVDS to drive a backplane.
- PCIe frequency translator for PCIe add-in cards. In personal computers, the PCIe reference clock is 100MHz, but some 2.5G serdes used in PCI Express require a 125MHz reference. The ICS8714008I can perform the 100MHz → 125MHz and 125MHz → 100MHz frequency translation for a PCI Express add-in card while delivering low dynamic and static phase offset.
- General purpose, low phase noise Zero Delay Buffer

Configuration Notes and Examples

When configuring the output frequency, the main consideration is keeping the VCO within its range of 490MHz - 660MHz. The designer must ensure that the VCO will always be within its allowed range for the expected input frequency range by using the appropriate choice of feedback output and input dividers. There are two input modes for the device. In the first mode, a reference clock is provided to the CLK, nCLK frequency input and this reference clock is divided by the value of the PDIV divider (selectable ÷1, ÷4, ÷5, ÷8). In the second mode, a reference clock is provided to the MLVDS, nMLVDS input pair. OE_MLVDS determines the input mode. When OE_MLVDS = HIGH (default), the M-LVDS driver is active and provides an M-LVDS output to the MLVDS, nMLVDS pins and also the reference to the phase detector via the PDIV divider. When OE_MLVDS is LOW, the internal M-LVDS driver is in a High-impedance state and the MLVDS, nMLVDS pin pair becomes an input and the reference clock applied to this input is applied to the phase detector.

MLVDS, nMLVDS Output Mode

OE_MLVDS = HIGH (default)

VCO frequency =
CLK, nCLK frequency * FBI_DIV * FBO_DIV/ (PDIV value)

Allowed VCO frequency = 490MHz - 660MHz

Output frequency = VCO frequency/QDIVx value =
CLK, nCLK freq. * FBI_DIV * FBO_DIV/(PDIV*QDIVx)

Example: a frequency synthesizer provides a 125MHz reference clock to CLK, nCLK frequency input. The ICS8714008I must provide a 25MHz M-LVDS clock to the backplane and also provide two local clocks: one 100MHz HCSL output to an ASIC and one 125MHz output to the PCI Express serdes.

Solution: Since only two outputs are needed, the two unused outputs can be disabled. Set OE[2:0] = 001b so that only Q0, nQ0 and Q1, nQ1 are switching. Since a 25MHz backplane clock is needed from a 125MHz reference clock, set PDIV = ÷5 and OE_MLVDS = HIGH to enable the M-LVDS driver. 25MHz is applied to the MLVDS, nMLVDS pins and to the phase detector input. Set FBO_DIV = 4 and FBI_DIV = 5 which makes the VCO run at 500MHz (25MHz * 4 * 5 = 500MHz). Set QDIV0 = 0 (÷4) for 125MHz output and QDIV1 = 1 (÷5) for 100MHz output. To figure out what pins must pulled up or down externally with resistors, check the internal pullup or pulldown resistors on each pin in the pin description table or on the block diagram. PDIV[1:0] defaults to 00/÷4 and we need 01/÷5. So PDIV1 can be left floating (it has an internal pulldown resistor) and PDIV0 must be driven or pulled up via external pullup resistor to HIGH state. OE_MLVDS defaults to Logic 1 (active) and this is what we need, so that pin can be left floating. The FBO_DIV and FBIN dividers default to the desired values, so their respective control pins can be left floating (FBO_DIV and FBI_DIV[1:0]). QDIV0 needs to be ÷4, which is a default value so this pin can be left floating. QDIV1 must be HIGH for ÷5, so this pin must be pulled high or driven high externally. OE[2:0] = 001, so OE0 can Float and OE[2:1] must be pulled Low.

MLVDS, nMLVDS Input Mode

OE_MLVDS = LOW

VCO frequency = MLVDS, nMLVDS freq. * FBI_DIV * FBO_DIV

Output frequency = VCO frequency/QDIVx value = MLVDS, nMLVDS freq. * FBI_DIV * FBO_DIV/(QDIVx)

Example - backplane: The 8714008I sits on a backplane card and must multiply a 25MHz reference that comes from the backplane into one 125MHz reference clock for a Gigabit Ethernet serdes and one 100MHz reference clock for a PCI Express serdes.

Solution. Since only two outputs are needed, the two unused outputs can be disabled. Set OE[2:0] = 001b so that only Q0, nQ0 and Q1, nQ1 are switching. Set OE_MLVDS = 0 so the internal M-LVDS driver is in a High-impedance state, allowing the MLVDS, nMLVDS pins to function as an input for the 25MHz clock reference. Set FBO_DIV = 4 and FBI_DIV = 5 which makes the VCO run at 500MHz (25MHz * 4 * 5 = 500MHz). Set QDIV0 = 0 (÷4) for 125MHz output and QDIV1 = 1 (÷5) for 100MHz output. To figure out what pins must pulled up or down externally with resistors, check the internal pullup or pulldown resistors on each pin in the pin description table or on the block diagram. PDIV[1:0] defaults to 00/÷4 and we need 01/÷5. So PDIV1 can be left floating (it has an internal pulldown resistor) and PDIV0 must be driven or pulled up via external pullup resistor to HIGH state. OE_MLVDS defaults to Logic 1(active) and this is what we need, so that pin can be left floating. The FBO_DIV and FBIN dividers default to the desired values, so their respective control pins can be left floating (FBO_DIV and FBI_DIV[1:0]). QDIV0 needs to be ÷4, which is a default value so this pin can be left floating. QDIV1 must be HIGH for ÷5, so this pin must be pulled high or driven high externally.

OE[2:0] = 001, so OE0 can Float and OE[2:1] must be pulled Low.

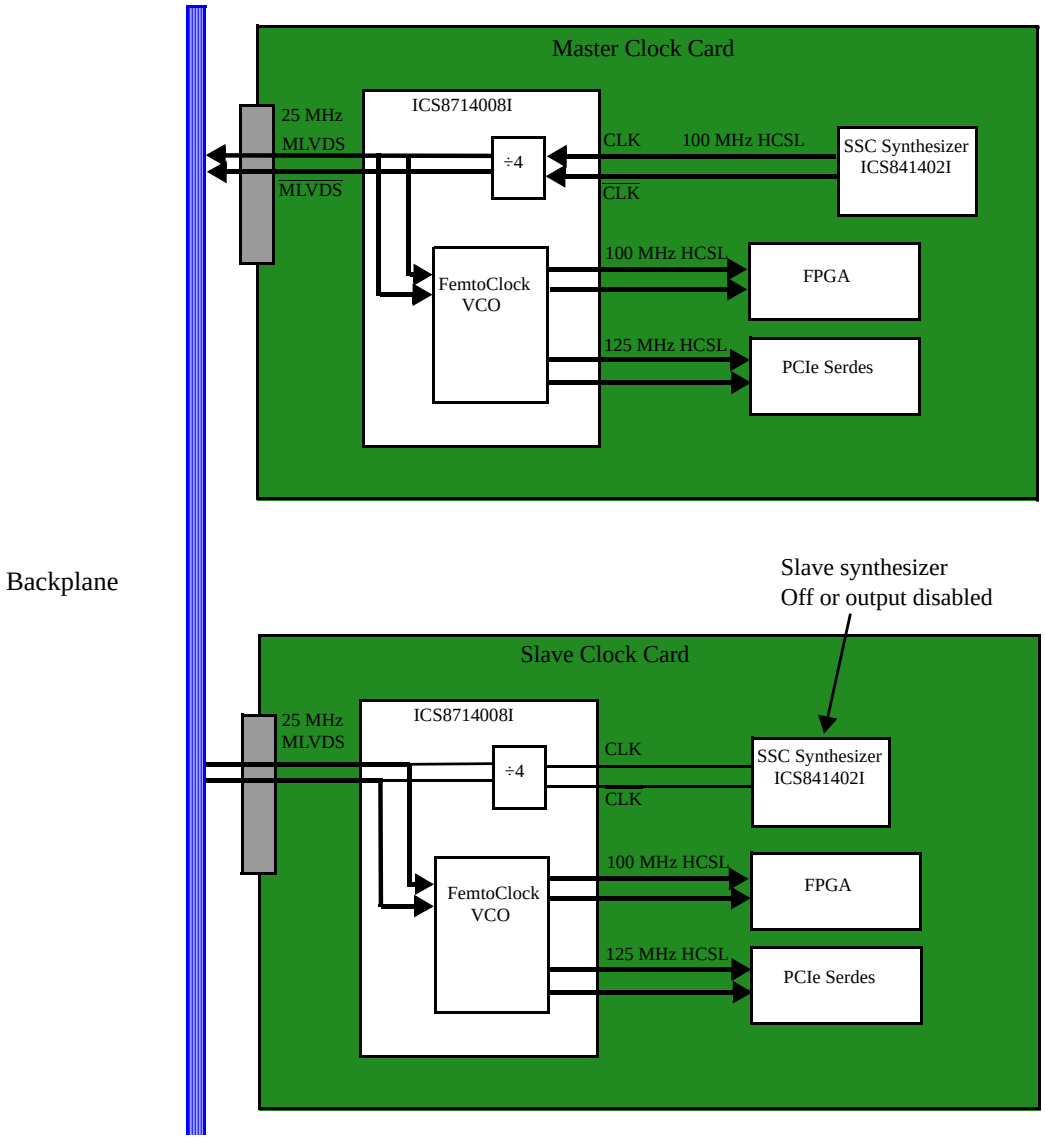


Figure 1. Example Backplane Application

Bold lines ⟶ indicate active clock path

This example shows a case where each card may be dynamically configured as a master or slave card, hence the need for an ICS8714008I and ICS841402I on each card. On the master timing card, the ICS841402I provides a 100MHz reference to the ICS8714008I CLK, nCLK input. The M-LVDS pair on the ICS8714008I is configured as an output (OE_MLVDS = Logic 1) and the internal divider is set to ÷4 to generate 25MHz M-LVDS to the backplane. The 25MHz clock is also used as a reference to the FemtoClock PLL which multiplies to a VCO frequency of 500MHz. Each of the four output pairs may be individually set for ÷4 or ÷5 for 125MHz or 100MHz operation respectively and in this example, one output pair is set to 100MHz for the FPGA and another output pair is set to 125MHz for the PCI Express serdes. For the slave card, the M-LVDS pair is configured as an input (OE_MLVDS = LOW) and the FemtoClock PLL multiplies this reference frequency to 500MHz VCO frequency and the output dividers are set to provide 100MHz to the FPGA and 125MHz to the PCI Express Serdes as shown.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 3.3V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

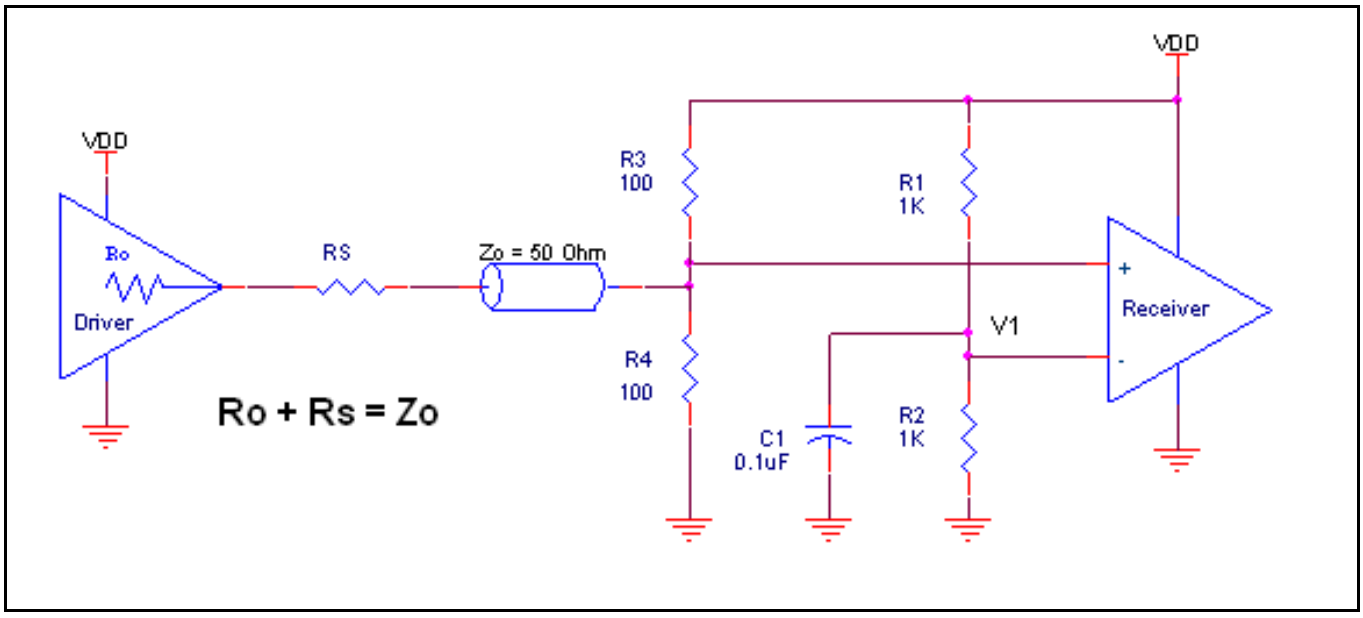


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

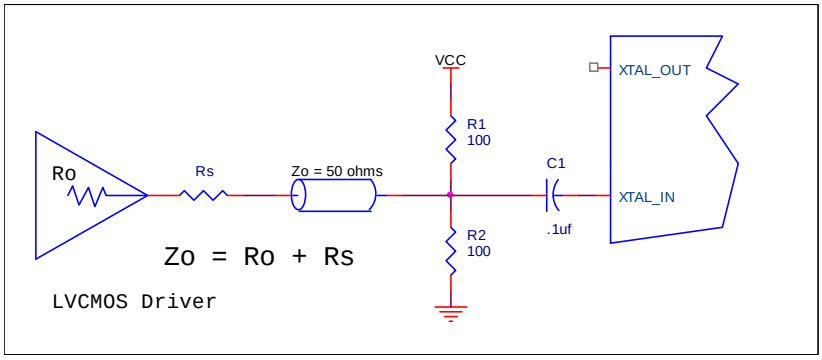


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

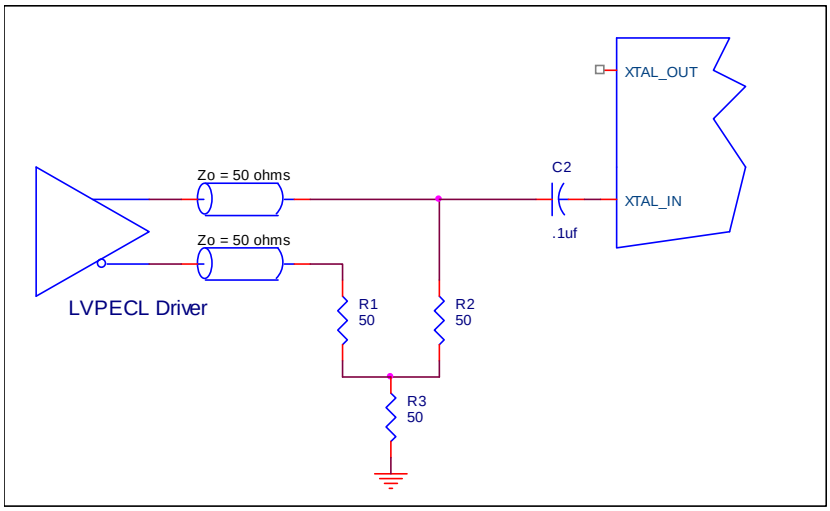


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

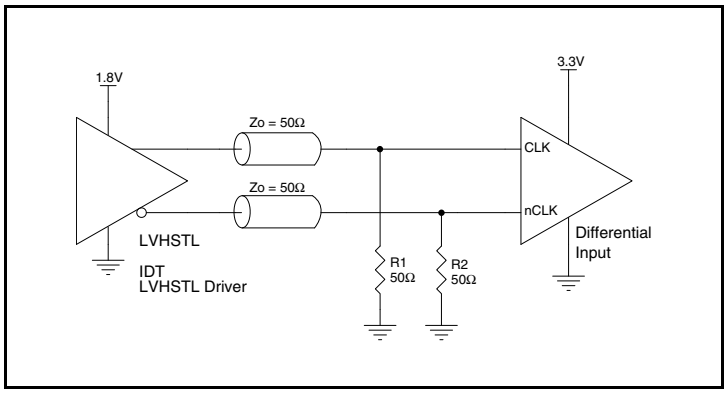


Figure 4A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

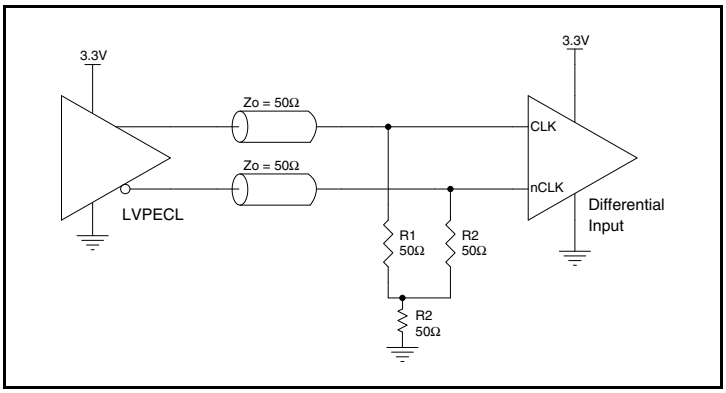


Figure 4B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

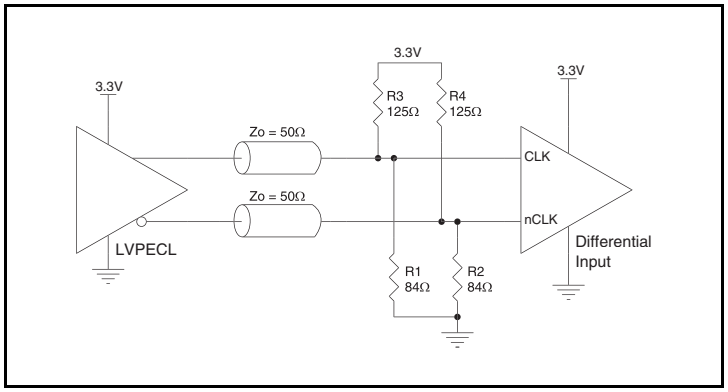


Figure 4C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

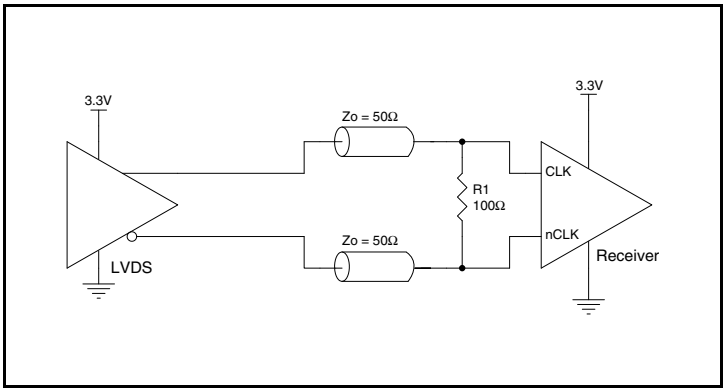


Figure 4D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

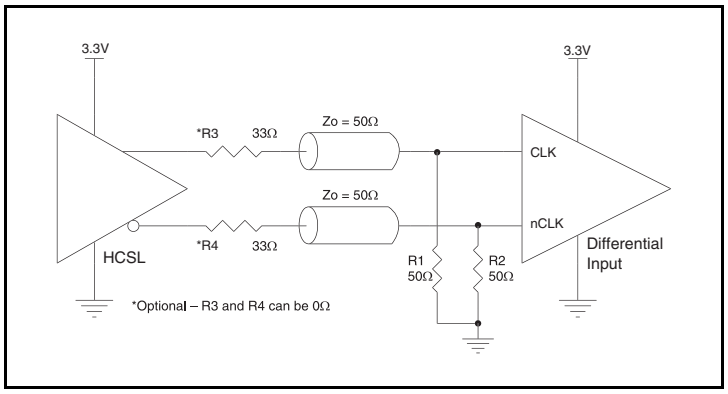


Figure 4E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

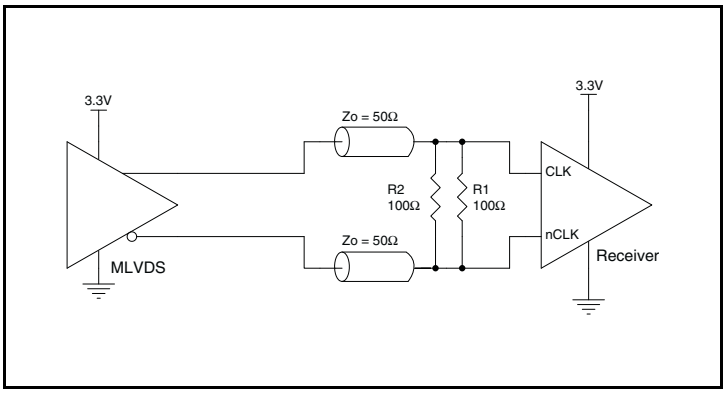


Figure 4F. CLK/nCLK Input Driven by a 3.3V MLVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

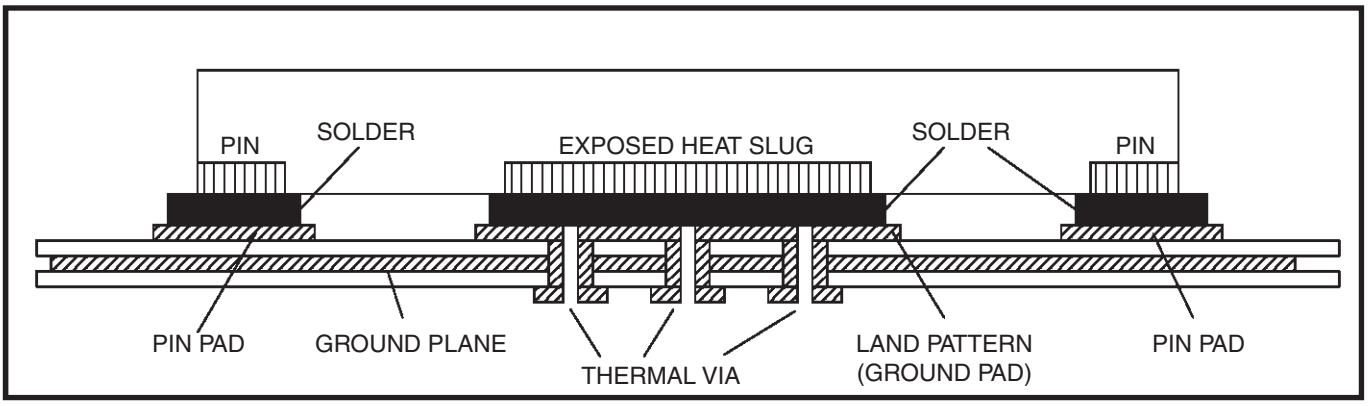


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

MLVDS/nMLVDS Inputs

For applications not requiring the use of the differential input, both MLVDS and nMLVDS can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from MLVDS to ground.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

M-LVDS Outputs

All unused M-LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Recommended Termination

Figure 7A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

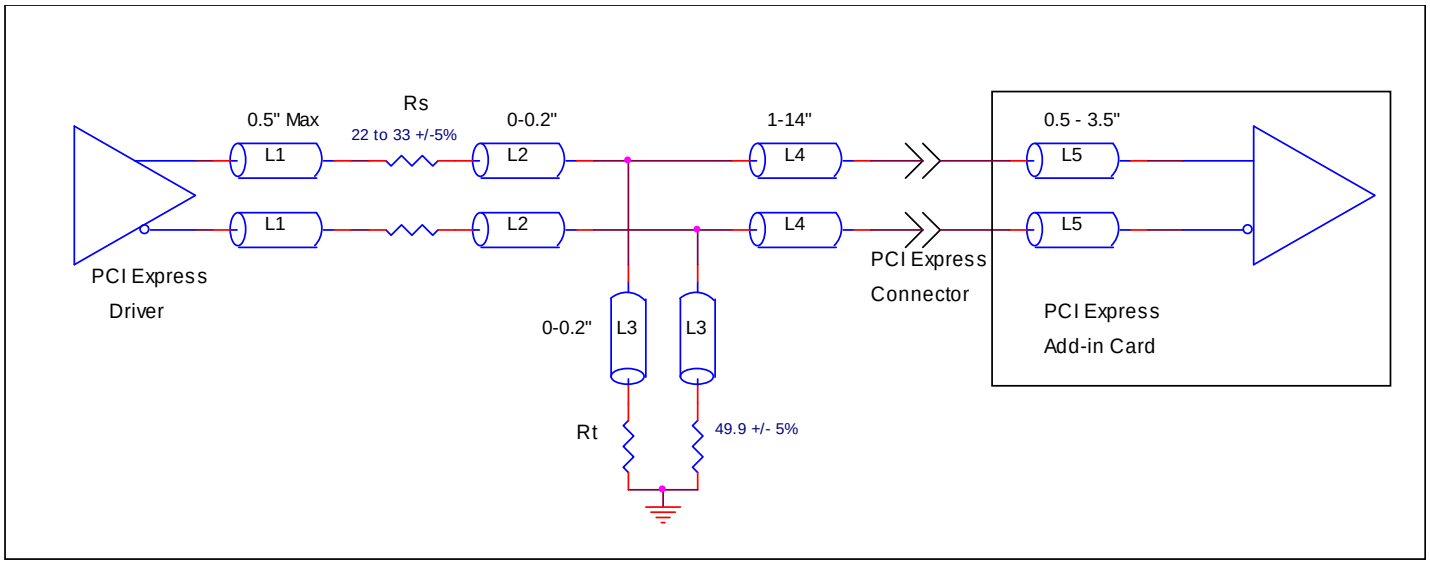


Figure 7A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 7B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

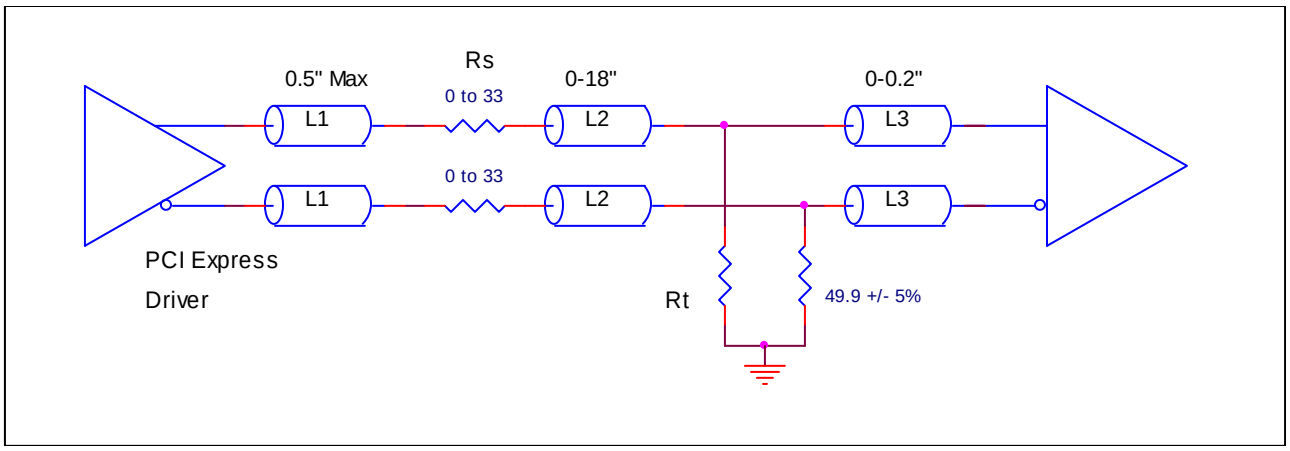


Figure 7B. Recommended Termination (where a point-to-point connection can be used)

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

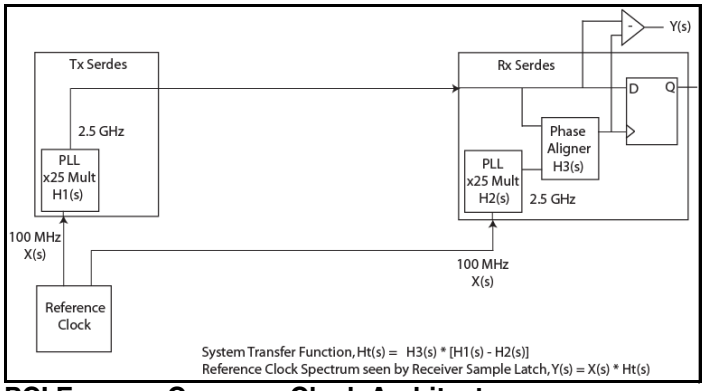
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

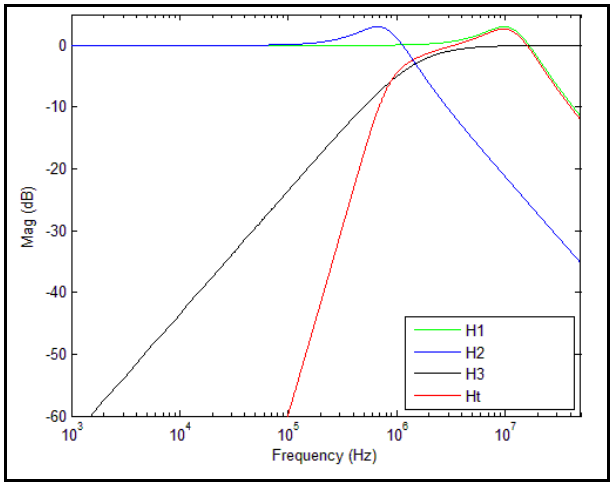
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



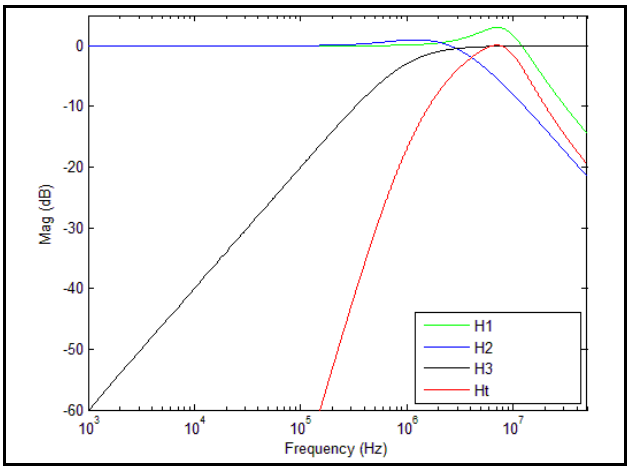
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

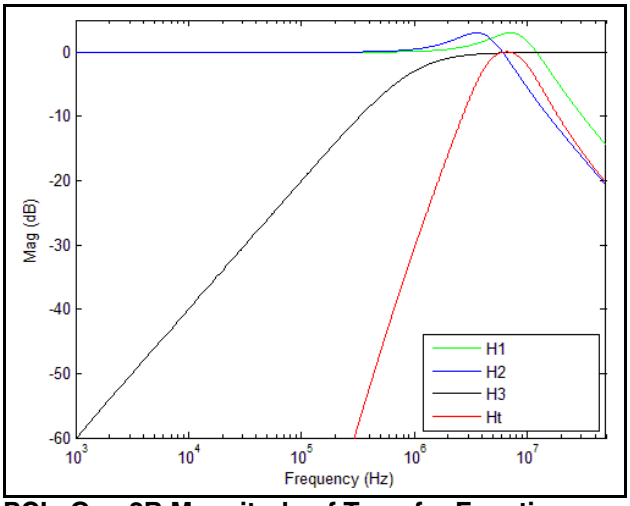


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

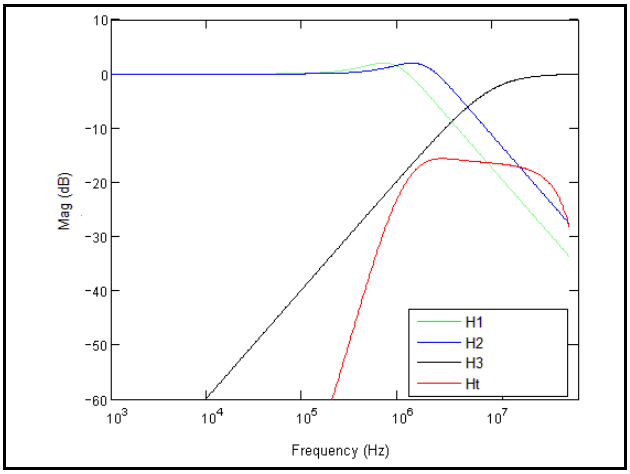


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Schematic Example

Figure 9 (next page) shows an example ICS8714008DI application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. Input and output terminations shown are also intended as examples only and may not represent the exact user configuration.

In this particular schematic the MLVDS port is in output mode, configured by setting OE_MLVDS = 1. Since the zero delay function is local to the chip, the FBOUT to FBIN connection is a special case of a point to point PCIe link. The close proximity of these two ports means that the 33Ω series resistors are not necessary and the 49.9Ω termination resistors are to be placed at the FBIN port.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8714008DI provides separate VDD, VDDO and VDDA power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is highly recommended that the 0.1µF capacitors be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite bead, 10µF and 0.1µF capacitors connected to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

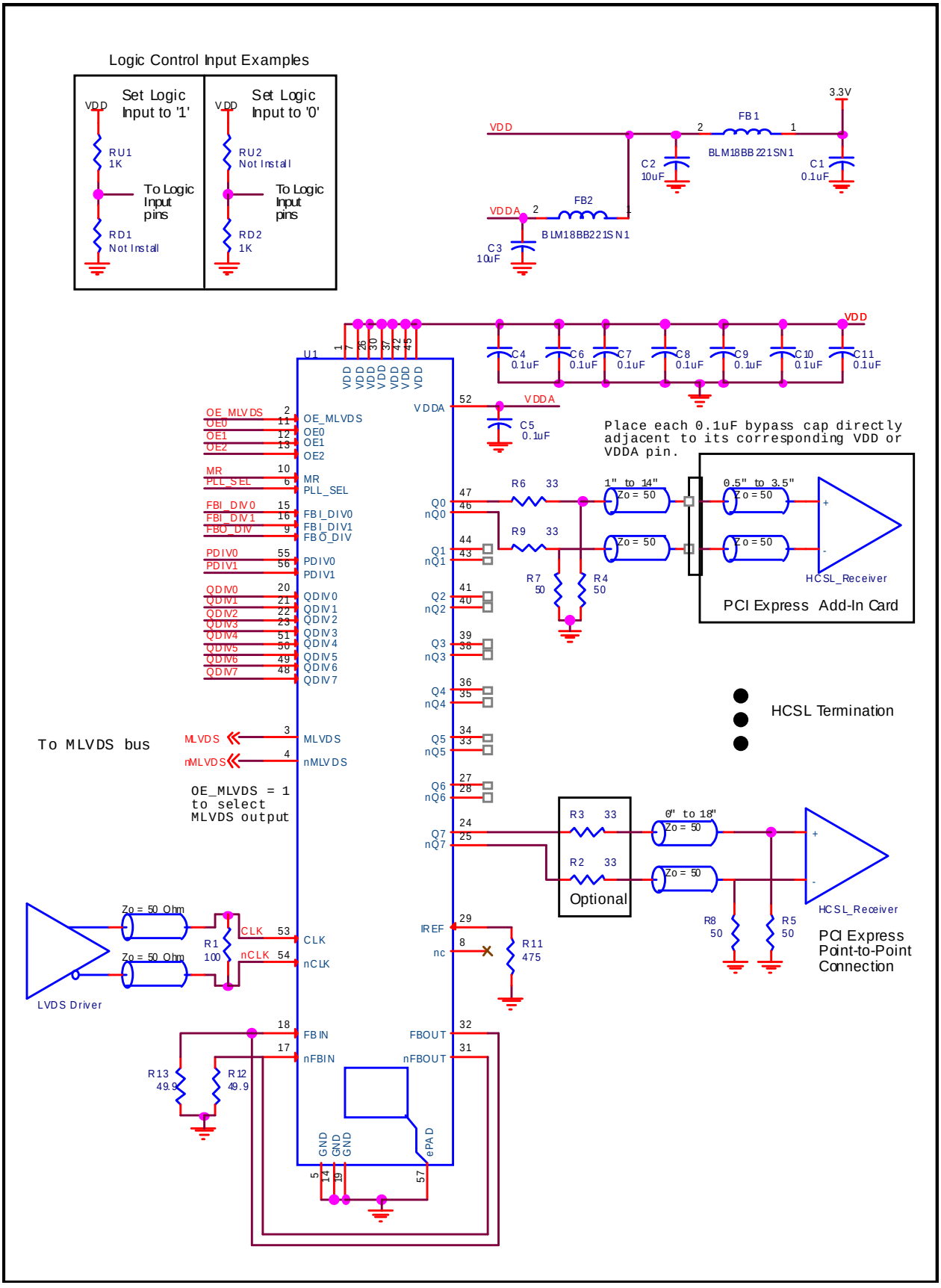


Figure 9. ICS8714008I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8714008I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8714008I is the sum of the core power plus the analog power plus the output power dissipated due to the load. The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating output power dissipated due to the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V *(210mA + 15mA) = **779.6mW**
- Power $(outputs)_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 9 * 44.5mW = **400.5mW**

Total Power$_{\_MAX}$ = 779.6mW + 400.5mW = **1180.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 26.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.180W * 26.7°C/W = 116.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 56-Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.7°C/W	21.71°C/W	20.23°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 10.*

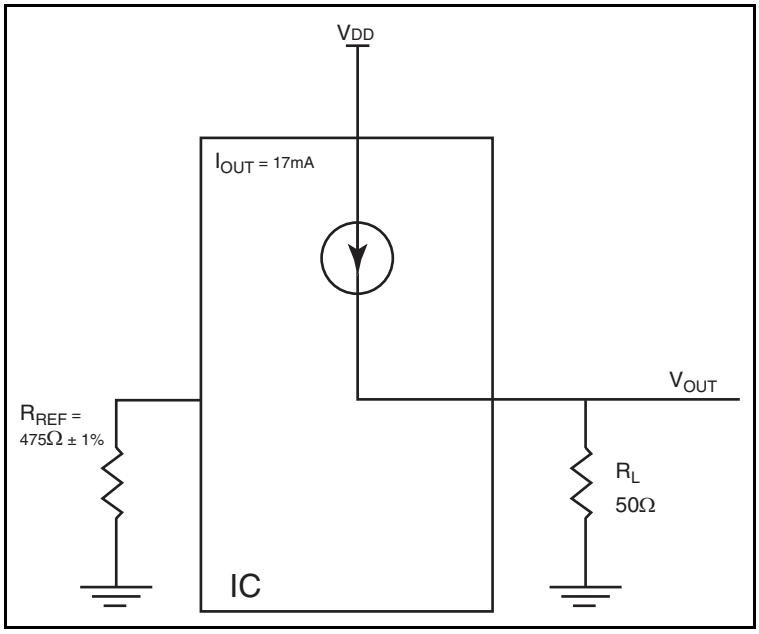


Figure 10. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power = $(V_{DD\_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} = I_{OUT} * R_L$

= $(V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 56-Lead VFQFN

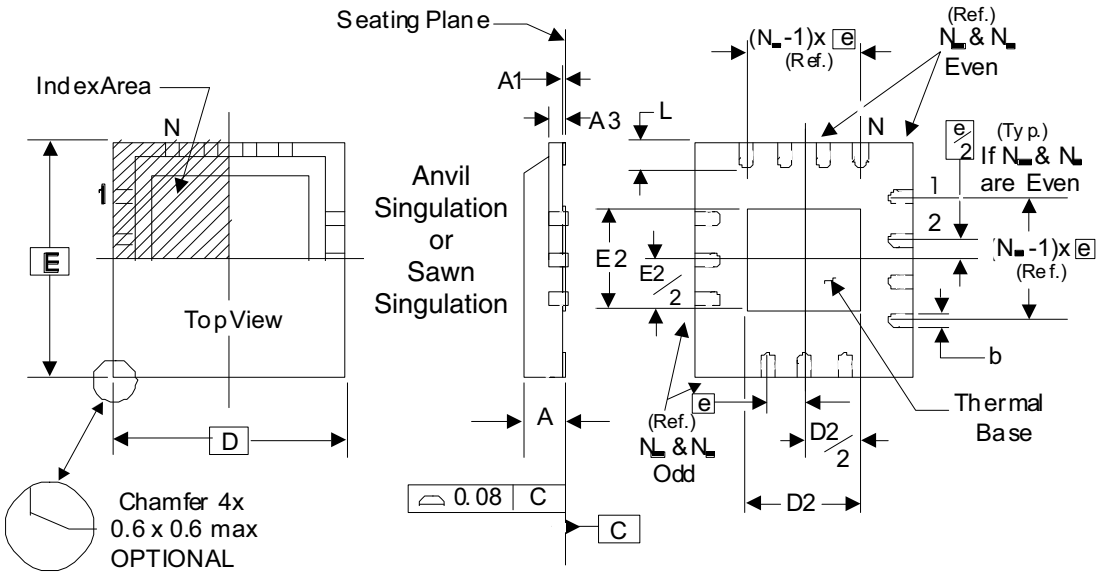
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.7°C/W	21.71°C/W	20.23°C/W

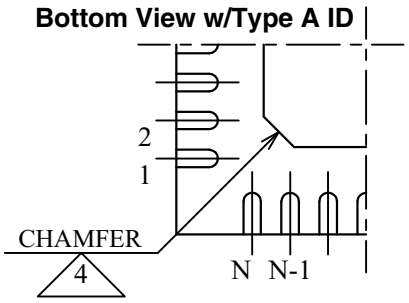
Transistor Count

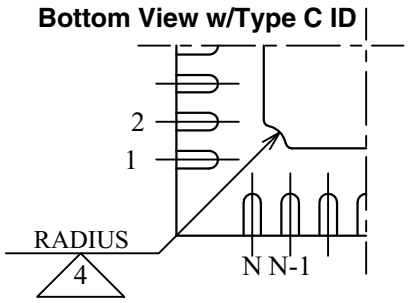
The transistor count for ICS8714008I is: 4962

Package Outline and Package Dimensions

Package Outline - K Suffix for 56-Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VJJD-2/-5 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	56	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	14	
D & E	8.00 Basic	
D2 & E2	2.75	6.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8714008DKILF	ICS8714008DIL	“Lead-Free” 56-Lead VFQFN	Tray	-40°C to 85°C
8714008DKILFT	ICS8714008DIL	“Lead-Free” 56-Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1, 3 26, 27	Correction on pin 26 label from "V_{DD}" to "nc" (not connected). The pin label change will have no effect on any electrical specifications and will not impact any applications of this device. Pin 26 can be left connected to board V_{DD} or unconnected. Updated Schematic.	10/9/2013
A		27	Corrected schematic example.	11/25/2013

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