# **RENESAS** Low Skew, 1-to-6, Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer

# ICS853S006I

DATA SHEET

### **General Description**

The ICS853S006I is a low skew, high performance 1-to-6 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer. The ICS853S006I is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853S006I ideal for those clock distribution applications demanding well defined performance and repeatability.

### **Features**

- Six differential 2.5V, 3.3V LVPECL/ECL outputs
- One differential PCLK, nPCLK input pair •
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 2GHz
- Output skew: 50ps (max) ٠
- Part-to-part skew: 230ps (max)
- Propagation delay: 550ps (max)
- LVPECL mode operating voltage supply range:  $V_{CC}$  = 2.375V to 3.465V,  $V_{EE}$  = 0V
- ECL mode operating voltage supply range:  $V_{CC} = 0V$ ,  $V_{EE} = -2.375V$  to -3.465V
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) package

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## **Block Diagram**



# **Pin Assignment**

			-
Vcc□	1	20	□ Vcc
nQ0□	2	19	🛛 Q5
Q0 🗆	3	18	🗌 nQ5
nQ1□	4	17	🛛 Q4
Q1	5	16	🗆 nQ4
nQ2□	6	15	🗆 Q3
Q2	7	14	🗌 nQ3
Vcc□	8	13	□ Vcc
PCLK	9	12	VEE
nPCLK	10	11	🗆 Vвв

ICS853S006I

20-Lead TSSOP 6.5mm x 4.4mm x 0.92mm package body **G** Package **Top View** 

# Table 1. Pin Descriptions

Number	Name	T	уре	Description
1, 8, 13, 20	V <sub>CC</sub>	Power		Positive supply pin.
2, 3	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
4, 5	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
6, 7	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
9	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
10	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V <sub>CC</sub> /2 default when left floating.
11	V <sub>BB</sub>	Output		Bias voltage.
12	V <sub>EE</sub>	Power		Negative supply pin.
14, 15	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
16, 17	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
18, 19	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

# **Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			75		kΩ
R <sub>VCC/2</sub>	Pullup/Pulldown Resistors			50		kΩ

# **Function Tables**

Table 3. Clock Input Function Table

Inj	outs	Outputs			
PCLK	nPCLK	Q0:Q5	nQ0:nQ5	Input to Output Mode	Polarity
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

Note 1: Please refer to the Applications Information, "Wiring the Differential Input to Accept Single Ended Levels".

# **Absolute Maximum Ratings**

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V <sub>CC</sub>	4.6V (LVPECL mode, V <sub>EE</sub> = 0V)
Negative Supply Voltage, V <sub>EE</sub>	-4.6V (ECL mode, V <sub>CC</sub> = 0V)
Inputs, V <sub>I</sub> (LVPECL mode)	-0.5V to V <sub>CC</sub> + 0.5V
Inputs, V <sub>I</sub> (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, I <sub>O</sub> Continuos Current Surge Current	50mA 100mA
V <sub>BB</sub> Sink//Source, I <sub>BB</sub>	± 0.5mA
Operating Temperature Range, T <sub>A</sub>	-40°C to +85°C
Package Thermal Impedance, $\theta_{JA}$	92.1°C/W (0 mps)
Storage Temperature, T <sub>STG</sub>	-65°C to 150°C

# **DC Electrical Characteristics**

Table 4A. Power Supply DC Characteristics,  $V_{CC}$  = 2.375V to 3.465V;  $V_{EE}$  = 0V,  $T_A$  = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>CC</sub>	Positive Supply Voltage		2.375	3.3	3.465	V
I <sub>EE</sub>	Power Supply Current				60	mA

				-40°C			25°C			85°C		
Symbol	Parameter		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
V <sub>OH</sub>	Output High Vo	oltage; NOTE 1	2.18	2.37	2.41	2.21	2.35	2.42	2.24	2.34	2.41	V
V <sub>OL</sub>	Output Low Vo	ltage; NOTE 1	1.405	1.56	1.68	1.425	1.55	1.65	1.44	1.55	1.65	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		625	800	870	690	800	870	730	800	852	mV
V <sub>IH</sub>	Input High Voltage (Single-ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V <sub>IL</sub>	Input Low Voltage (Single-ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
$V_{BB}$	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	V
V <sub>PP</sub>	Peak-to-Peak I	nput Voltage	150	800	1200	150	800	1200	150	800	1200	mV
V <sub>CMR</sub>	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		V <sub>CC</sub>	1.2		V <sub>CC</sub>	1.2		V <sub>CC</sub>	V
I <sub>IH</sub>	Input High Current	PCLK, nPCLK			150			150			150	μA
	Input	PCLK	-10			-10			-10			μA
1		nPCLK	-150			-150			-150			μA

### Table 4B. LVPECL DC Characteristics, V\_{CC} = 3.3V; V\_{EE} = 0V, T\_A = -40^{\circ}C to $85^{\circ}C$

NOTE: Input and output parameters vary 1:1 with  $V_{\mbox{CC}}.$ 

NOTE 1: Outputs terminated with 50 $\Omega$  to V<sub>CCO</sub> – 2V.

NOTE 2: Single-ended input operation is limited. V<sub>CC</sub>  $\ge$  3V in LVPECL mode.

NOTE 3: Common mode voltage is defined as V<sub>IH</sub>.

NOTE 4: For single-ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{CC}$  + 0.3V

### Table 4C. LVPECL DC Characteristics, $V_{CC}$ = 2.5V; $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

	Parameter			-40°C		25°C			85°C			
Symbol			Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
V <sub>OH</sub>	Output High Ve	oltage; NOTE 1	1.38	1.57	1.61	1.41	1.55	1.62	1.44	1.54	1.61	V
V <sub>OL</sub>	Output Low Vo	oltage; NOTE 1	0.605	0.76	0.88	0.625	0.75	0.85	0.64	0.75	0.85	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		625	800	870	690	800	870	730	800	852	mV
V <sub>IH</sub>	Input High Voltage (Single-ended)		1.275		1.56	1.275		1.56	1.275		1.56	V
V <sub>IL</sub>	Input Low Voltage (Single-ended)		0.63		0.965	0.63		0.965	0.63		0.965	V
V <sub>PP</sub>	Peak-to-Peak	Input Voltage	150	800	1200	150	800	1200	150	800	1200	mV
V <sub>CMR</sub>	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		V <sub>CC</sub>	1.2		V <sub>CC</sub>	1.2		V <sub>CC</sub>	V
I <sub>IH</sub>	Input High Current	PCLK, nPCLK			150			150			150	μA
	Input	PCLK	-10			-10			-10			μA
Ι <sub>ΙL</sub>	Low Current	nPCLK	-150			-150			-150			μA

NOTE: Input and output parameters vary 1:1 with  $V_{CC.}$ 

NOTE 1: Outputs terminated with 50  $\Omega$  to V\_{CCO} – 2V.

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{CC}$  + 0.3V.

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				-40°C			25°C			85°C		
Symbol	Parameter		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
V <sub>OH</sub>	Output High V	oltage; NOTE 1	-1.12	-0.93	-0.89	-1.09	-0.95	-0.88	-1.06	-0.96	-0.89	V
V <sub>OL</sub>	Output Low Vo	oltage; NOTE 1	-1.895	-1.74	-1.62	-1.875	-1.75	-1.65	-1.86	-1.75	-1.65	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		625	800	870	690	800	870	730	800	852	mV
$V_{\text{IH}}$	Input High Voltage (Single-ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V <sub>IL</sub>	Input Low Voltage (Single-ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
$V_{BB}$	Output Voltage Reference; NOTE 2		-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V <sub>PP</sub>	Peak-to-Peak	Input Voltage	150	800	1200	150	800	1200	150	800	1200	mV
V <sub>CMR</sub>	Input High Voltage Common Mode Range; NOTE 3, 4		V <sub>EE</sub> +1.2		0	V <sub>EE</sub> +1.2		0	V <sub>EE</sub> +1.2		0	V
IIH	Input High Current	PCLK, nPCLK			150			150			150	μA
1	Input	PCLK	-10			-10			-10			μA
1	Low Current	nPCLK	-150			-150			-150			μA

### Table 4D. ECL DC Characteristics, $V_{CC}$ = 0V; $V_{EE}$ = -3.465V to -2.375V, $T_{A}$ = -40°C to 85°C

NOTE 1: Outputs terminated with 50 $\Omega$  to V<sub>CCO</sub> – 2V. NOTE 2: Single-ended input operation is limited. V<sub>EE</sub>  $\leq$  -3V in LVPECL mode.

NOTE 3: Common mode voltage is defined as  $V_{IH}$ . NOTE 4: For single-ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{CC}$  + 0.3V

# **AC Electrical Characteristics**

Table 5. AC Characteristics,  $V_{CC}$  = 0;  $V_{EE}$  = -2.375V to -3.465V or ,  $V_{CC}$  = 2.375V to 3.465V;  $V_{EE}$  = 0V,  $T_A$  = -40°C to 85°C

			-40°C		25°C			85°C				
Symbol	Parameter		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Units
f <sub>OUT</sub>	Output Frequency				2			2			2	GHz
t <sub>PD</sub>	Propagation Delay; NOTE 1		230	375	530	260	400	535	300	420	550	ps
<i>t</i> sk(o)	Output Skew; NOT	E 2, 4		21	50		22	50		23	50	ps
<i>t</i> sk(pp)	Part-to-Part Skew;	NOTE 3, 4			230			230			230	ps
<i>t</i> jit	Buffer Additive Phase Jitter, RMS; 156.25MHz, Integration Range: 1kHz – 40MHz, refer to Additive Phase Jitter Section			0.08			0.09			0.10		ps
+ /+	Output Rise/Fall	20% to 80%	55	136	240	55	140	240	55	150	240	ps
t <sub>R</sub> / t <sub>F</sub>	Time	10% to 90%	65	210	400	65	210	400	65	230	400	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters are measured at  $f \leq 1 GHz,$  unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

# **Additive Phase Jitter**

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm)

or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



**Offset from Carrier Frequency (Hz)** 

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rhode & Schwarz SMA 100 as the input source.

# RENESAS

### **Parameter Measurement Information**



3.3V LVPECL Output Load AC Test Circuit



**Differential Input Level** 



**Output Skew** 



**Output Rise/Fall Time** 



2.5V LVPECL Output Load AC Test Circuit



Part-to-Part Skew



**Propagation Delay** 



### **Output Rise/Fall Time**

# **Application Information**

### Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50 $\Omega$  applications, R3 and R4 can be 100 $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V<sub>IL</sub> cannot be less than -0.3V and V<sub>IH</sub> cannot be more than V<sub>CC</sub> + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.



Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

# LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both V<sub>SWING</sub> and V<sub>OH</sub> must meet the V<sub>PP</sub> and V<sub>CMR</sub> input requirements. *Figures 3A to 3E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.



Figure 3A. PCLK/nPCLK Input Driven by a CML Driver



Figure 3C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver



Figure 3E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver



Figure 3D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

### **Recommendations for Unused Output Pins**

### **Outputs:**

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### **Termination for 3.3V LVPECL Outputs**

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$ 



Figure 4A. 3.3V LVPECL Output Termination

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



Figure 4B. 3.3V LVPECL Output Termination

### **Termination for 2.5V LVPECL Outputs**

*Figure 5A* and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to V<sub>CC</sub> – 2V. For V<sub>CC</sub> = 2.5V, the V<sub>CC</sub> – 2V is very close to ground



Figure 5A. 2.5V LVPECL Driver Termination Example



Figure 5C. 2.5V LVPECL Driver Termination Example

level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C*.



Figure 5B. 2.5V LVPECL Driver Termination Example

### **Schematic Example**

*Figure 6* shows a schematic example of ICS853S006I. The ICS853S006I input can accept various types of differential input signal. In this example, the inputs are driven by an LVPECL drivers. For the ICS853S006I LVPECL output driver, an example of LVPECL driver termination approach is shown in this schematic. Additional

LVPECL driver termination approaches are shown in the LVPECL Termination Application Note. It is recommended at least one decoupling capacitor per power pin. The decoupling capacitors should be physically located near the power pins. For ICS853S006I, the unused output can be left floating.



Figure 6. ICS853S006I Example LVPECL Clock Output Buffer Schematic



### **Power Considerations**

This section provides information on power dissipation and junction temperature for the ICS853S006I. Equations and example calculations are also provided.

#### 1. Power Dissipation.

The total power dissipation for the ICS853S006I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> = V<sub>CC MAX</sub> \* I<sub>EE MAX</sub> = 3.465V \* 60mA = 207.9mW
- Power (outputs)<sub>MAX</sub> = 32.02mW
   If all outputs are loaded, the total power is 6 \* 32.02mW = 192.12mW

Total Power\_MAX (3.465V, with all outputs switching) = 207.9mW + 192.12mW = 400.02mW

#### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for this device is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj =  $\theta_{JA}$  \* Pd\_total + T<sub>A</sub>

Tj = Junction Temperature

 $\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd\_total = Total Device Power Dissipation (example calculation is in section 1 above)

 $T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

 $85^{\circ}C + 0.400W * 92.1^{\circ}C/W = 121.84^{\circ}C$ . This is below the limit of  $125^{\circ}C$ .

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

#### Table 6. Thermal Resistance $\theta_{JA}$ for 20 Lead TSSOP, Forced Convection

θ <sub>JA</sub> by Velocity								
Meters per Second	0	1	2.5					
Multi-Layer PCB, JEDEC Standard Test Boards	92.1°C/W	86.5°C/W	83.0°C/W					

#### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in Figure 7.



Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50 $\Omega$  load, and a termination voltage of V<sub>CC</sub> – 2V.

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} 0.88V$ ( $V_{CC\_MAX} - V_{OH\_MAX}$ ) = 0.88V
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} 1.62V$ ( $V_{CC\_MAX} - V_{OL\_MAX}$ ) = 1.62V

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

 $\begin{array}{l} \mathsf{Pd}_{-}\mathsf{H} = [(\mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}} - (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - 2\mathsf{V}))/\mathsf{R}_{\mathsf{L}}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}}) = [(2\mathsf{V} - (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}}))/\mathsf{R}_{\mathsf{L}}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OH}\_\mathsf{MAX}}) = [(2\mathsf{V} - 0.88\mathsf{V})/50\Omega] * 0.88\mathsf{V} = \textbf{19.71mW} \end{array}$ 

 $\mathsf{Pd}_{L} = [(\mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}} - (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - 2\mathsf{V}))/\mathsf{R}_{L}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}}) = [(2\mathsf{V} - (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}}))/\mathsf{R}_{L}] * (\mathsf{V}_{\mathsf{CC}\_\mathsf{MAX}} - \mathsf{V}_{\mathsf{OL}\_\mathsf{MAX}}) = [(2\mathsf{V} - 1.62\mathsf{V})/50\Omega] * 1.62\mathsf{V} = \mathbf{12.31mW}$ 

Total Power Dissipation per output pair = Pd\_H + Pd\_L = 32.02mW

# **Reliability Information**

Table 7.  $\theta_{\text{JA}}$  vs. Air Flow Table for a 20 Lead TSSOP

θ <sub>JA</sub> by Velocity								
Meters per Second	0	1	2.5					
Multi-Layer PCB, JEDEC Standard Test Boards	92.1°C/W	86.5°C/W	83.0°C/W					

### **Transistor Count**

The transistor count for ICS853S006I is: 332

This device is pin and functional compatible with and is the suggested replacement for the ICS853006.

# Package Outline and Package Dimensions

### Package Outline - G Suffix for 20 Lead TSSOP



#### Table 8. Package Dimensions

All Dimensions in Millimeters				
Symbol	Minimum	Maximum		
Ν	20			
Α		1.20		
A1	0.05	0.15		
A2	0.80	1.05		
b	0.19	0.30		
С	0.09	0.20		
D	6.40	6.60		
E	6.40 Basic			
E1	4.30	4.50		
e	0.65 Basic			
L	0.45	0.75		
α	0°	8°		
aaa		0.10		

Reference Document: JEDEC Publication 95, MO-153



# **Ordering Information**

### **Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S006AGILF	ICS53S006AIL	20 Lead TSSOP	Tube	-40°C to 85°C
853S006AGILFT	ICS53S006AIL	20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.



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(Rev.1.0 Mar 2020)

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