

# RENESAS FemtoClock® Crystal-to-LVDS **Clock Generator**

DATA SHEET

## GENERAL DESCRIPTION

The 844021I-01 is an Ethernet Clock Generator. The 844021I-01 uses an 18pF parallel resonant crystal over the range of 24.5MHz - 34MHz. For Ethernet appli-cations, a 25MHz crystal is used. The 844021I-01 has excellent <1ps phase jitter performance, over the 1.875MHz - 20MHz integration range. The 844021I-01 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

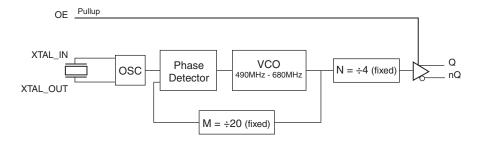
### **FEATURES**

- · One Differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (24.5MHz - 34MHz)
- Output frequency range: 122.5MHz 170MHz
- VCO range: 490MHz 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.32ps (typical) @ 3.3V
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

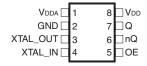
#### COMMON CONFIGURATION TABLE - Gb ETHERNET

	Output Frequency			
Crystal Frequency (MHz)	М	N	Multiplication Value M/N	(MHz)
25	20	4	5	125
26.666	20	4	5	133.33
33.33	20	4	5	166.66

### **BLOCK DIAGRAM**



## PIN ASSIGNMENT



### 844021I-01

8-Lead TSSOP 4.40mm x 3.0mm x 0.925mm package body G Package Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Туре		Description
1	V <sub>DDA</sub>	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Output enable pin. When HIGH, Q/nQ output is active. When LOW, the Q/nQ output is in a high impedance state. LVCMOS/LVT-TL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVDS interface levels.
8	V <sub>DD</sub>	Power		Core supply pin.

NOTE: Pullup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R	Input Pullup Resistor			51		kΩ



#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V<sub>DD</sub> 4.6V

Inputs,  $V_{DD}$  -0.5 V to  $V_{DD}$  + 0.5 V

Outputs, I<sub>o</sub> (LVDS)

Continuous Current 10mA
Surge Current 15mA

Package Thermal Impedance,  $\theta_{MA}$  129.5°C/W (0 mps)

Storage Temperature,  $T_{STG}$  -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ , Ta = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>DD</sub>	Core Supply Voltage		3.135	3.3	3.465	V
V <sub>DDA</sub>	Analog Supply Voltage		V <sub>DD</sub> - 0.10	3.3	V <sub>DD</sub>	V
I <sub>DD</sub>	Power Supply Current				75	mA
I <sub>DDA</sub>	Analog Supply Current				10	mA

Table 3B. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ , Ta = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>DD</sub>	Core Supply Voltage		2.375	2.5	2.625	V
V <sub>DDA</sub>	Analog Supply Voltage		V <sub>DD</sub> - 0.10	2.5	V	V
I <sub>DD</sub>	Power Supply Current				70	mA
I <sub>DDA</sub>	Analog Supply Current				10	mA

Table 3C. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ , Ta = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>IH</sub>	Input High Voltage	$V_{_{DD}} = 3.3V$	2		V <sub>DD</sub> + 0.3	V
	input night voltage	$V_{_{DD}} = 2.5V$	1.7		V <sub>DD</sub> + 0.3	V
\ <u></u>	Innest Law Valtage	$V_{_{DD}} = 3.3V$	-0.3		0.8	V
V <sub>IL</sub>	Input Low Voltage	$V_{_{DD}} = 2.5V$	-0.3		0.7	V
I <sub>IH</sub>	Input High Current	$V_{DD} = V_{IN} = 3.465 \text{V or } 2.625 \text{V}$			5	μΑ
I	Input Low Current	$V_{_{DD}} = 3.465V \text{ or } 2.625V, V_{_{IN}} = 0V$	-150			μΑ



Table 3D. LVDS DC Characteristics,  $V_{_{DD}} = 3.3V \pm 5\%$ , Ta = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>od</sub>	Differential Output Voltage		275		425	mV
$\Delta$ V $_{_{ m OD}}$	V <sub>ob</sub> Magnitude Change				50	mV
Vos	Offset Voltage		1.15		1.45	V
$\Delta V_{os}$	V <sub>os</sub> Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

Table 3E. LVDS DC Characteristics,  $V_{_{DD}} = 2.5V \pm 5\%$ , Ta = -40°C to  $85^{\circ}C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>od</sub>	Differential Output Voltage		215		430	mV
$\Delta$ V $_{_{ m OD}}$	V <sub>op</sub> Magnitude Change				50	mV
V <sub>os</sub>	Offset Voltage		1.05		1.45	V
$\Delta V_{os}$	V <sub>os</sub> Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4. CRYSTAL CHARACTERISTICS

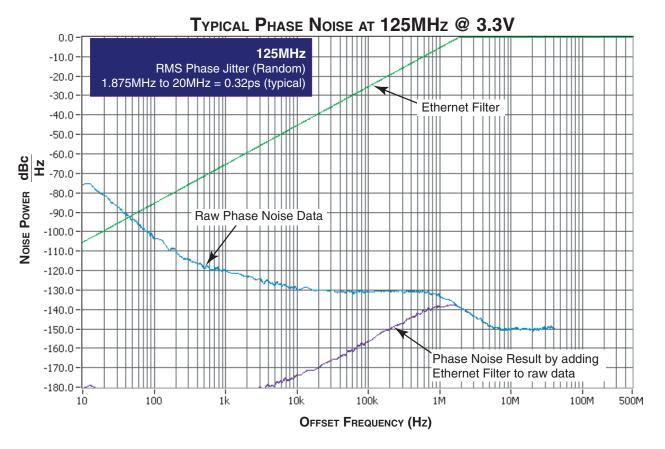
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		F	undamental		
Frequency		24.5		34	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

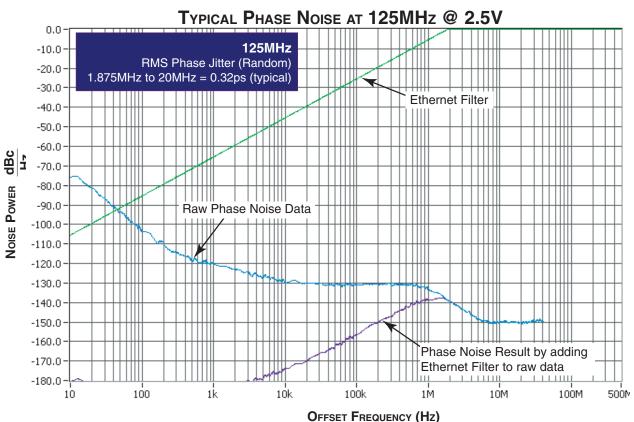
NOTE: It is not recommended to overdrive the crystal input with an external clock.

Table 5. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ , Ta = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>out</sub>	Output Frequency		122.5		170	MHz
tjit(Ø)	RMS Phase Jitter ( Random); NOTE 1	125MHz @ Integration Range: 1.875MHz - 20MHz		0.32		ps
t <sub>R</sub> / t <sub>F</sub>	Output Rise/Fall Time	20% to 80%	200		400	ps
odc	Output Duty Cycle		48		52	%

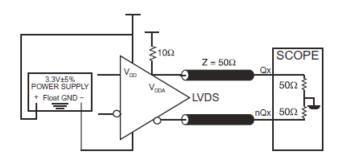
NOTE 1: Please refer to the Phase Noise Plots following this section.

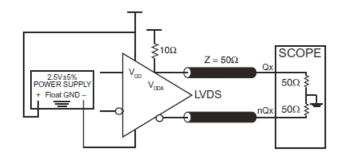




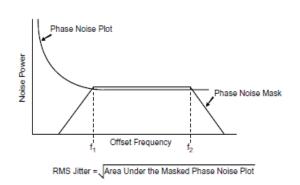


# PARAMETER MEASUREMENT INFORMATION

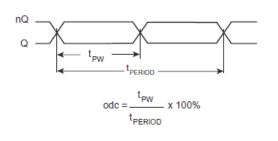




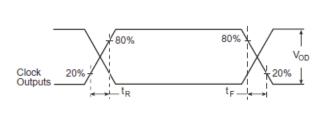
#### LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT



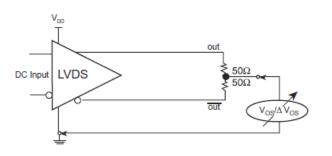
### LVDS 2.5V OUTPUT LOAD AC TEST CIRCUIT



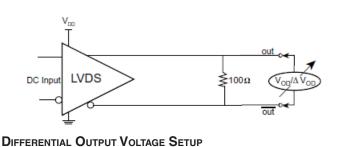
#### **RMS PHASE JITTER**



## OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



#### **OUTPUT RISE/FALL TIME**



### OFFSET VOLTAGE SETUP



# **APPLICATION INFORMATION**

### Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844021I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{_{\rm DD}}$  and  $V_{_{\rm DDA}}$  should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. Figure 1 illustrates this for a generic V $_{_{\rm DD}}$  pin and also shows that V $_{_{\rm DDA}}$  requires that an additional10 $\Omega$  resistor along with a 10µF bypass capacitor be connected to the V $_{_{\rm DDA}}$  pin.

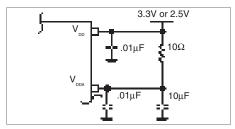


FIGURE 1. POWER SUPPLY FILTERING

### **CRYSTAL INPUT INTERFACE**

The 844021I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

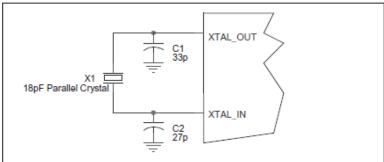


FIGURE 2. CRYSTAL INPUT INTERFACE



# 3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in Figure 4 In a  $100\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of  $100\Omega$  across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

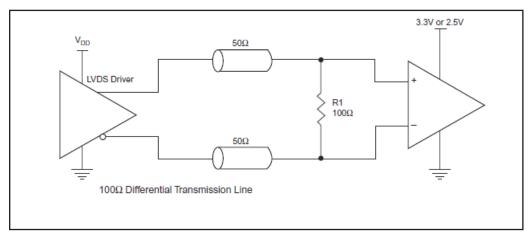


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION



### SCHEMATIC LAYOUT

Figure 5 shows an example of 844021I-01 application schematic. In this example, the device is operated at  $V_{\tiny DD} = 3.3V$ . The decoupling capacitor should be located as close as possible to the power pin. The 18pF parallel resonant 25MHz crystal is used. The C1 = 33pF and C2 = 27pF are recommended

for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. For the LVDS output drivers, place a  $100\Omega$  resistor as close to the receiver as possible.

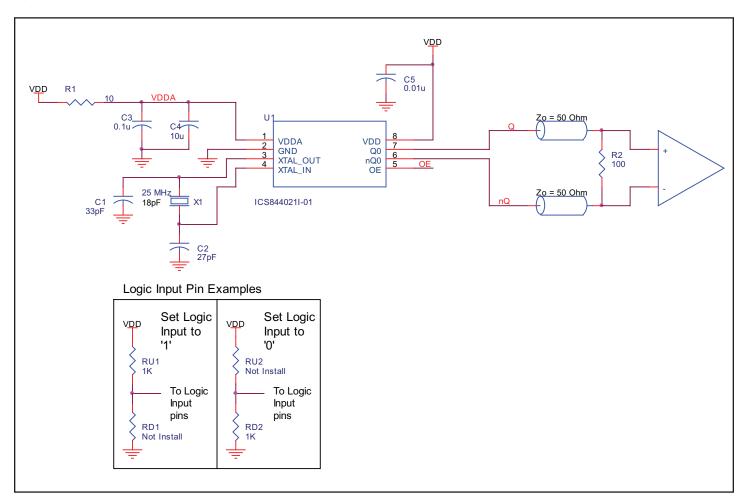


FIGURE 5. 844021I-01 SCHEMATIC LAYOUT



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 844021I-01 Equations and example calculations are also provided.

#### 1. Power Dissipation.

The total power dissipation for the 844021I-01 is the sum of the core power plus the analog plus the power dissipated in the load(s). The following is the power dissipation for  $V_{\infty} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

• Power (core)<sub>MAX</sub> =  $V_{DD,MAX}$  \* ( $I_{DD,MAX}$  +  $I_{DDA,MAX}$ ) = 3.465V \* (75mA + 10mA) = **294.5mW** 

#### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: Tj =  $\theta_{JA}$  \* Pd\_total + T<sub>A</sub>

Tj = Junction Temperature

 $\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd\_total = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is: 85°C + 0.295W \* 129.5°C/W = 123.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

#### Table 6. Thermal Resistance $\theta_{\text{JA}}$ for 8-Lead TSSOP, Forced Convection

# $\theta_{JA}$ by Velocity (Meters per Second)

 0
 1
 2.5

 Multi-Layer PCB, JEDEC Standard Test Boards
 129.5°C/W
 125.5°C/W
 123.5°C/W



# RELIABILITY INFORMATION

Table 7.  $\theta_{_{\mathrm{JA}}}$ vs. Air Flow Table for 8 Lead TSSOP

# $\theta_{\mbox{\tiny JA}}$ by Velocity (Meters per Second)

 0
 1
 2.5

 Multi-Layer PCB, JEDEC Standard Test Boards
 129.5°C/W
 125.5°C/W
 123.5°C/W

### TRANSISTOR COUNT

The transistor count for 844021I-01 is: 2533

# PACKAGE OUTLINE & DIMENSIONS

#### PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

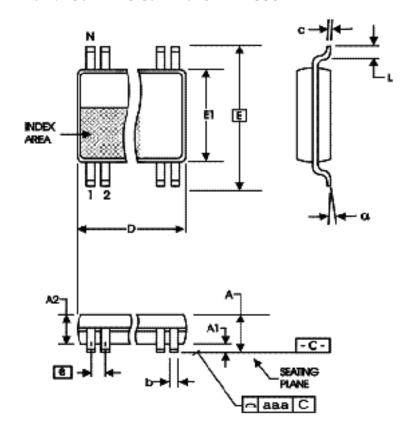


TABLE 8. PACKAGE DIMENSIONS

CVMDOL	Millin	neters		
SYMBOL	Minimum	Maximum		
N	8			
Α		1.20		
A1	0.05	0.15		
A2	0.80	1.05		
b	0.19	0.30		
С	0.09	0.20		
D	2.90	3.10		
E	6.40 E	BASIC		
E1	4.30	4.50		
е	0.65 E	BASIC		
L	0.45	0.75		
α	0°	8°		
aaa		0.10		

Reference Document: JEDEC Publication 95, MO-153



### TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844021BGI-01LF	BI01L	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS844021BGI-01LFT	BI01L	8 lead "Lead-Free" TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.



REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
А	T4 T9	1 4 8 12	Deleted HiPerClockS references. Crystal Characteristics Table - added note. Deleted application note, LVCMOS to XTAL Interface. Deleted quantity from tape and reel.	9/23/12
А	Т9	12	Ordering Information - removed leaded devices. Updated data sheet format.	10/27/15



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