General Description

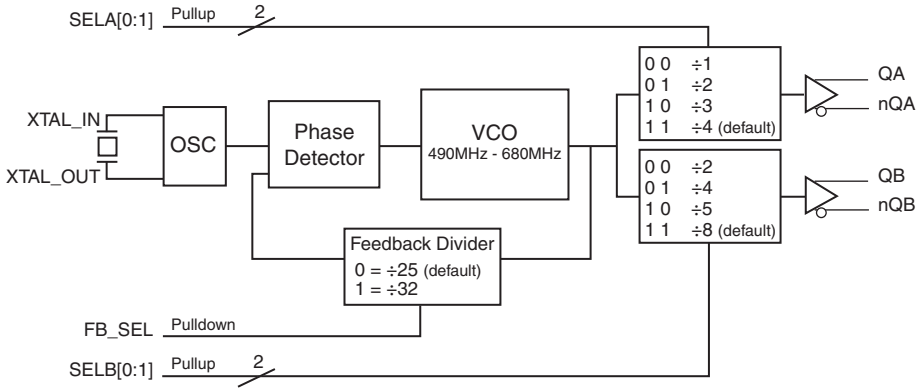
The 843252 is a 2 differential output LVPECL Synthesizer designed to generate Ethernet reference clock frequencies. Using a 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 frequency select pins (SELA[1:0], SELB[1:0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The 843252 IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843252 is packaged in a small 16-pin TSSOP package.

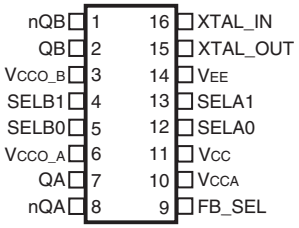
Features

- Two differential LVPECL output pairs
- Using a 25MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Crystal oscillator interface
- VCO frequency: 490MHz – 680MHz
- RMS Phase Jitter @ 156.25MHz, (1.875MHz – 20MHz) using a 25MHz crystal: 0.47ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



843252

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package

Pin Description and Pin Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQB, QB	Output		Bank B differential output pair. LVPECL interface levels.
3	V_{CCO_B}	Power		Output supply pin for QB, nQB outputs.
4, 5	SELB1, SELB0	Input	Pullup	Division select pins for Bank B. LVCMOS/LVTTL interface levels.
6	V_{CCO_A}	Power		Output supply pin for QA, nQA outputs.
7, 8	QA, nQA	Output		Bank A differential output pair. LVPECL interface levels.
9	FB_SEL	Input	Pulldown	Feedback divide select. When LOW, the feedback divider is set for ÷25. When HIGH, the feedback divider is set for ÷32. LVCMOS/LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
12, 13	SELA0, SELA1	Input	Pullup	Division select pins for Bank A. LVCMOS/LVTTL interface levels.
14	V_{EE}	Power		Negative supply pin.
15, 16	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Bank A Frequency Table

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA, nQA Output Frequency (MHz)
Crystal Frequency (MHz)	FB_SEL	SELA1	SELA0				
25	0	0	0	25	1	25	625
25	0	0	1	25	2	12.5	312.5
20	0	0	1	25	2	12.5	250
22.5	0	1	0	25	3	8.333	187.5
25	0	1	1	25	4	6.25	156.25
24	0	1	1	25	4	6.25	150
20	0	1	1	25	4	6.25	125
19.44	1	0	0	32	1	32	622.08
19.44	1	0	1	32	2	16	311.04
15.625	1	0	1	32	2	16	250
18.75	1	1	0	32	3	10.667	200
19.44	1	1	1	32	4	8	155.52
18.75	1	1	1	32	4	8	150
15.625	1	1	1	32	4	8	125

Table 3B. Bank B Frequency Table

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB, nQB Output Frequency (MHz)
Crystal Frequency (MHz)	FB_SEL	SELB1	SELB0				
25	0	0	0	25	2	12.5	312.5
20	0	0	0	25	2	12.5	250
25	0	0	1	25	4	6.25	156.25
24	0	0	1	25	4	6.25	150
20	0	0	1	25	4	6.25	125
25	0	1	0	25	5	5	125
25	0	1	1	25	8	3.125	78.125
24	0	1	1	25	8	3.125	75
20	0	1	1	25	8	3.125	62.5
19.44	1	0	0	32	2	16	311.04
15.625	1	0	0	32	2	16	250
19.44	1	0	1	32	4	8	155.52
18.75	1	0	1	32	4	8	150
15.625	1	0	1	32	4	8	125
15.625	1	1	0	32	5	6.4	100
19.44	1	1	1	32	8	4	77.76
18.75	1	1	1	32	8	4	75
15.625	1	1	1	32	8	4	62.5

Table 3C. Output Bank A Configuration Select Function Table

Inputs		Outputs
SELA1	SELA0	QA, nQA
0	0	÷1
0	1	÷2
1	0	÷3
1	1	÷4 (default)

Table 3D. Output Bank B Configuration Select Function Table

Inputs		Outputs
SELB1	SELB0	QB, nQB
0	0	÷2
0	1	÷4
1	0	÷5
1	1	÷8 (default)

Table 3E. Feedback Divider Configuration Select Function Table

Input	
FB_SEL	Feedback Divide
0	÷25 (default)
1	÷32

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	92.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current				10	mA
I_{EE}	Power Supply Current				145	mA

Table 4B. LVCMOS/LVTTL DC Characteristics,V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL	V_{CC} = V_{IN} = 3.465V			150	µA
		SELA[1:0], SELB[1:0]	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	FB_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		SELA[1:0], SELB[1:0]	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_X} – 1.4		V_{CCO_X} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_X} – 2.0		V_{CCO_X} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Output termination with 50Ω to $V_{CCO\_A, \_B}$ – 2V.

Table 5. Crystal Characteristics

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation				Fundamental		
Frequency	FB_SEL = ÷25		19.6		27.2	MHz
	FB_SEL = ÷32		15.313		21.25	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

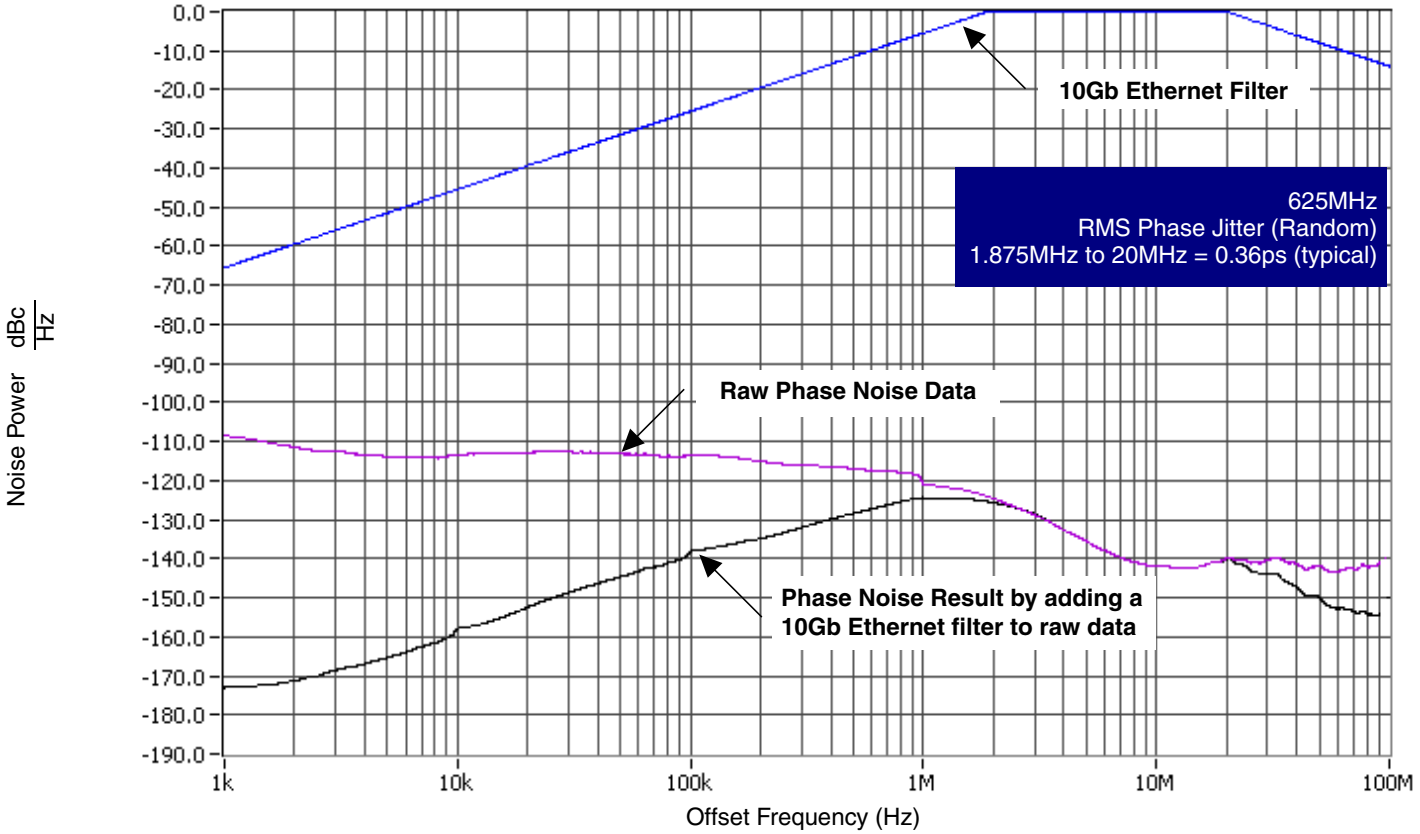
AC Electrical Characteristics

Table 6. AC Characteristics, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

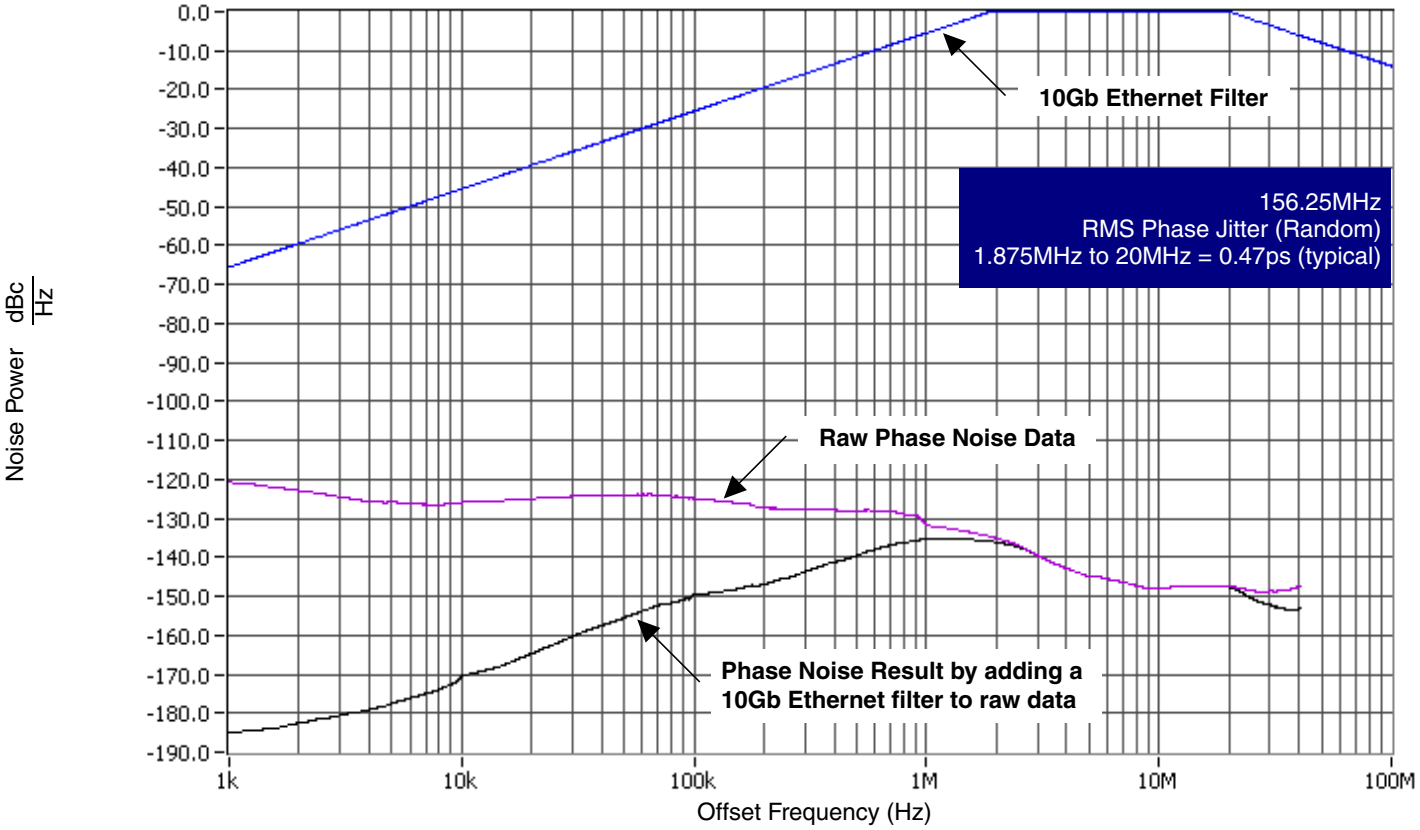
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	Output Divider = ÷ 1	490		680	MHz
		Output Divider = ÷ 2	245		340	MHz
		Output Divider = ÷ 3	163.33		226.67	MHz
		Output Divider = ÷ 4	122.5		170	MHz
		Output Divider = ÷ 5	98		136	MHz
		Output Divider = ÷8	61.25		85	MHz
*t*sk(o)	Output Skew; NOTE 1, 2	Outputs @ Same Frequency			80	ps
		Outputs @ Different Frequencies			190	ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 3	625MHz, (1.875MHz – 20MHz)		0.36		ps
		312.5MHz, (1.875MHz – 20MHz)		0.43		ps
		156.25MHz, (1.875MHz – 20MHz)		0.47		ps
		125MHz, (1.875MHz – 20MHz)		0.47		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plots.

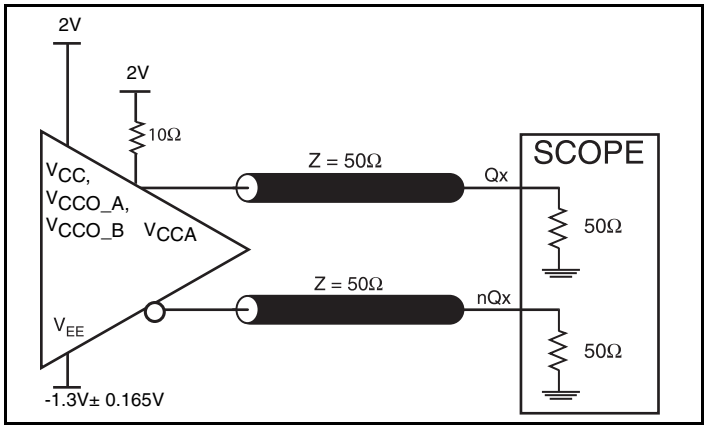
Typical Phase Noise at 625MHz



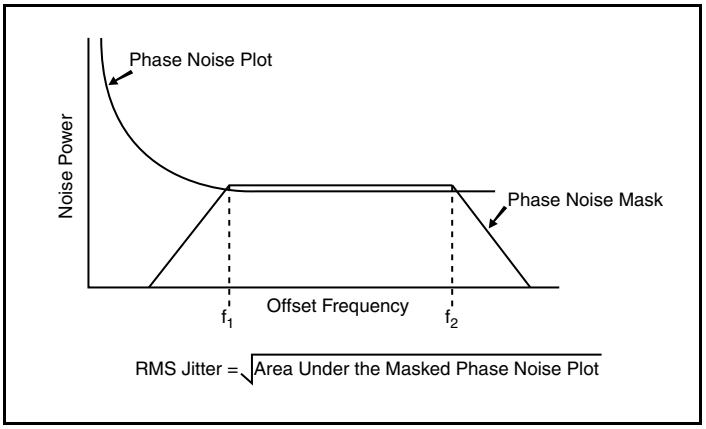
Typical Phase Noise at 156.25MHz



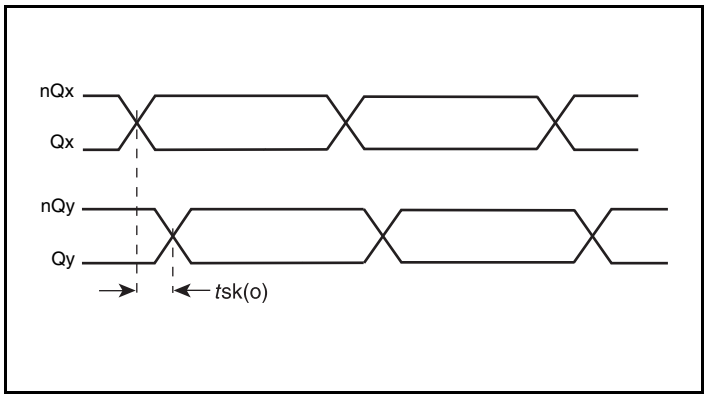
Parameter Measurement Information



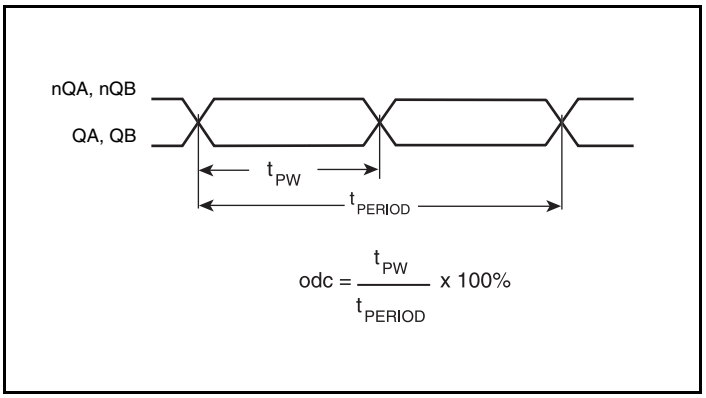
3.3V LVPECL Output Load AC Test Circuit



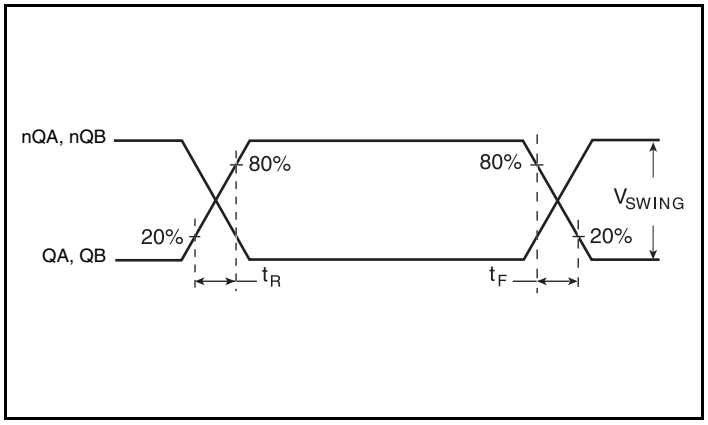
RMS Phase Jitter



Output Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter per- formance, power supply isolation is required. The 843252 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, V_{CCO_A}, and V_{CCO_B} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

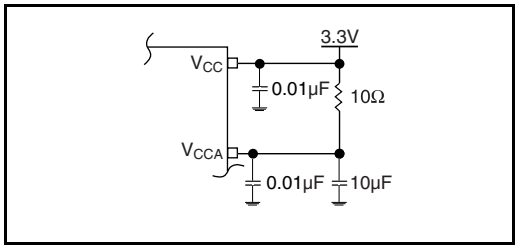


Figure 1. Power Supply Filtering

Crystal Input Interface

The 843252 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

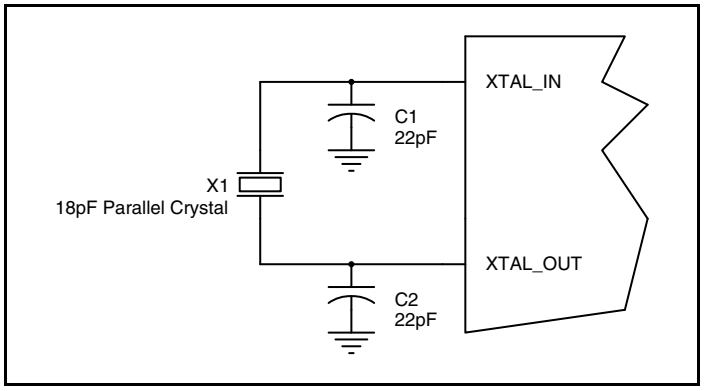


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

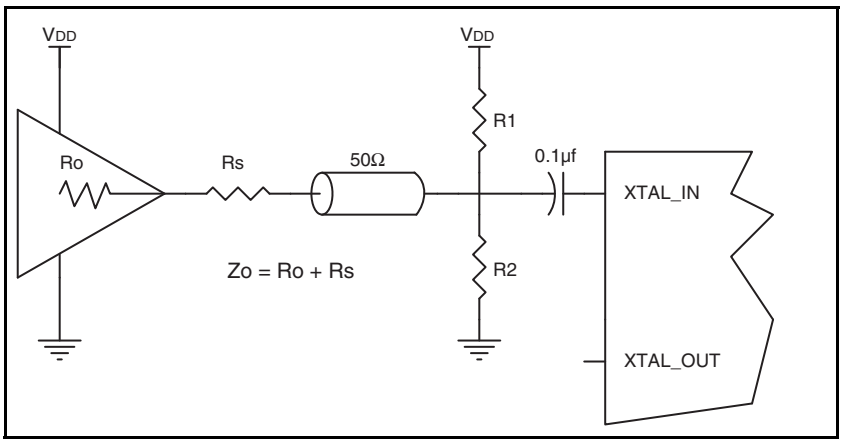


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

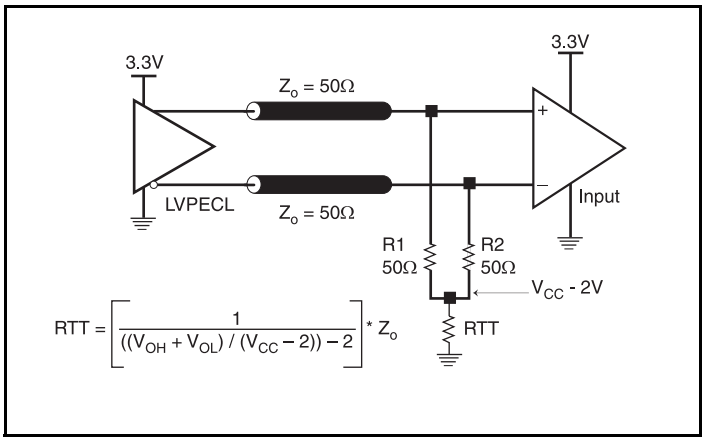


Figure 4A. 3.3V LVPECL Output Termination

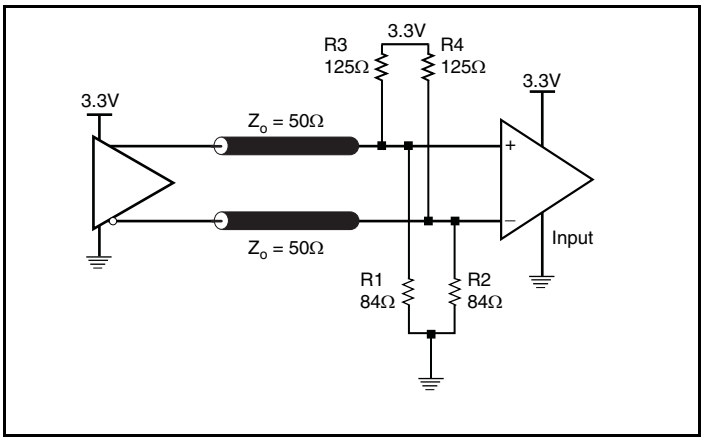


Figure 4B. 3.3V LVPECL Output Termination

Schematic Example

Figure 5 shows an example of 843252 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the *LVPECL Termination Application Note.*

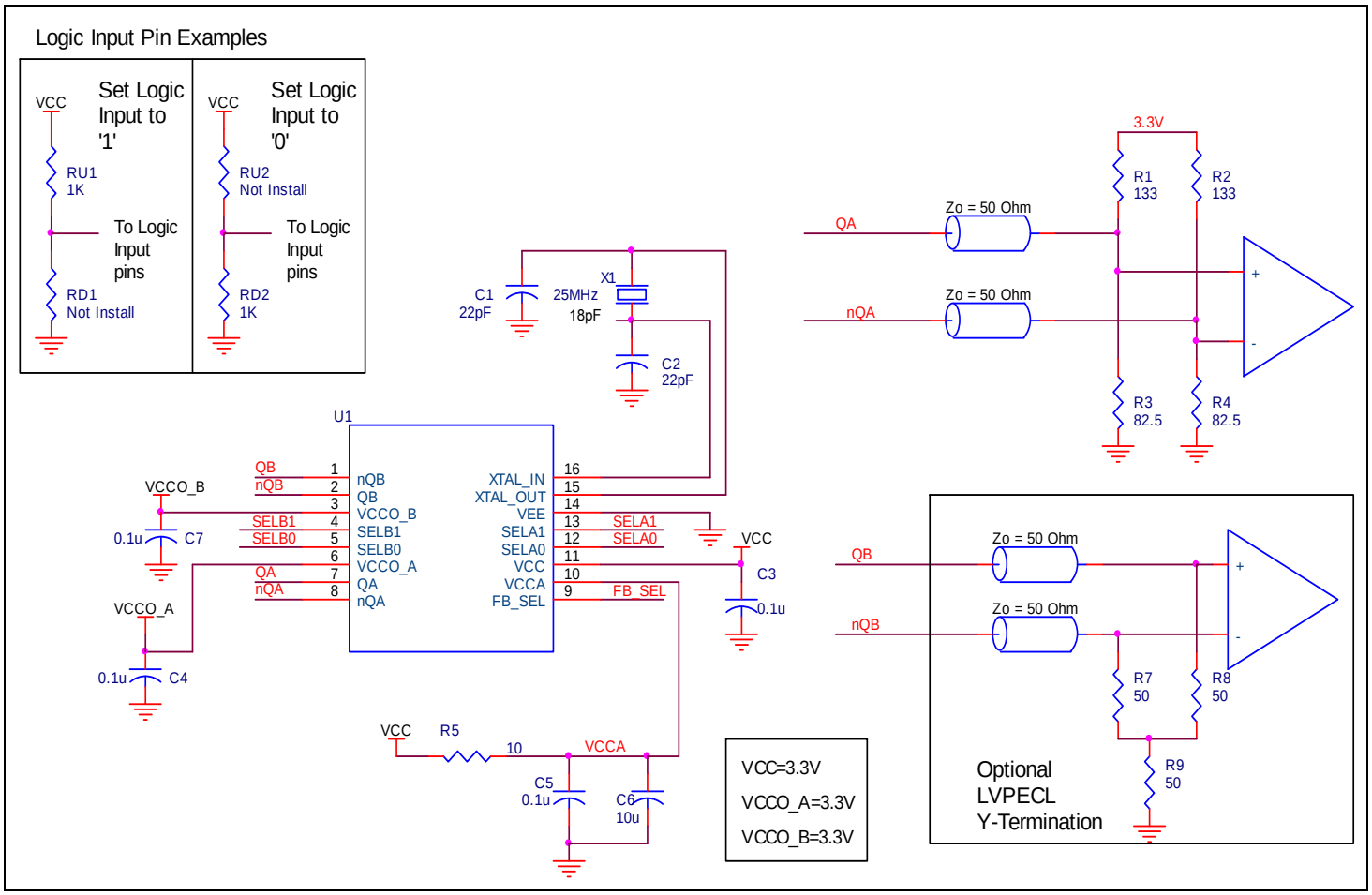


Figure 5. 843252 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843252.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843252 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 145mA = **502.43mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 502.43mW + 60mW = **562.43mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.562W * 92.4°C/W = 121.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

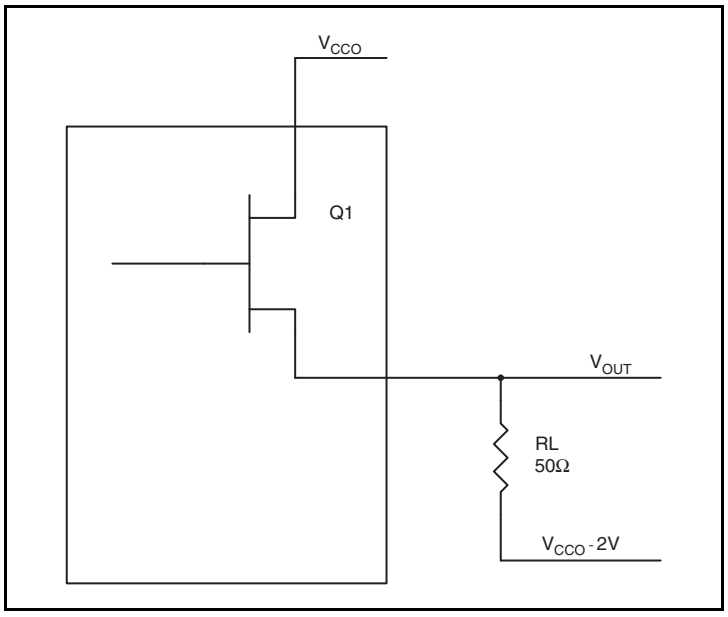


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} – 0.9V$
  $(V_{CCO\_MAX} – V_{OH\_MAX}) =$ **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} – 1.7V$
  $(V_{CCO\_MAX} – V_{OL\_MAX}) =$ **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Transistor Count

The transistor count for 843252 is: 3822

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

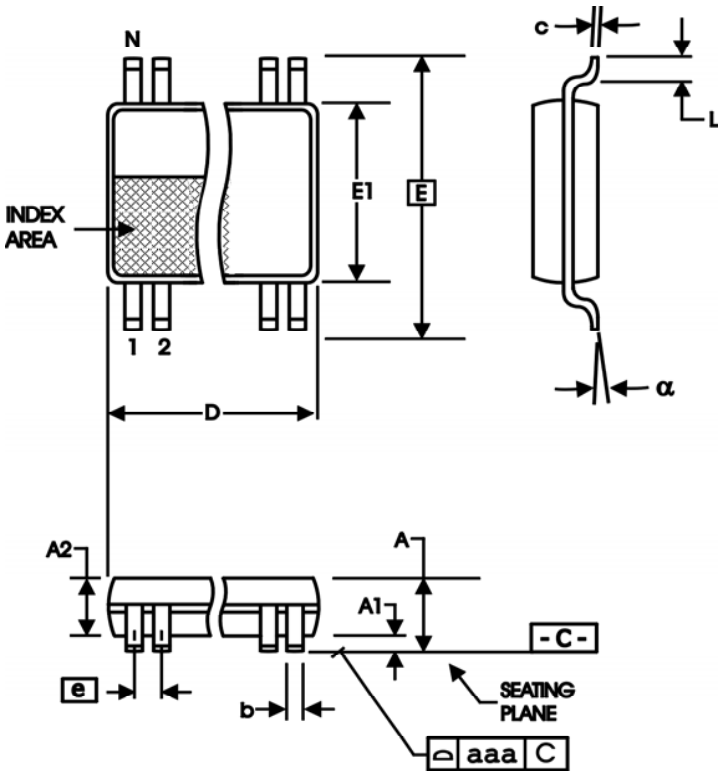


Table 9. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843252AGLF	843252AL	16 Lead TSSOP, Lead-Free	Tube	0°C to 70°C
843252AGLFT	843252AL	16 Lead TSSOP, Lead-Free	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T10	1 15	"General Description" - deleted *HiperClocks* logo and reference text. Ordering Information Table - deleted *Tape & Reel count*. Deleted all *HiperClocks* references throughout the datasheet. Deleted *ICS* prefix from part number throughout the datasheet. Updated datasheet header/footer.	1/19/16

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