FEATURES:

- **First-In/First-Out Dual-Port memory—45MHz**
- **64 x 5 organization**
- **Low-power consumption**
  - *Active: 200mW (typical)*
- **RAM-based internal structure allows for fast fall-through time**
- **Asynchronous and simultaneous read and write**
- **Expandable by bit width**
- **Cascadable by word depth**
- **Half-Full and Almost-Full/Empty status flags**
- **High-speed data communications applications**
- **Bidirectional and rate buffer applications**
- **High-performance CMOS technology**
- **Available in plastic DIP and SOIC**
- **Green parts available, see ordering information**

DESCRIPTION:

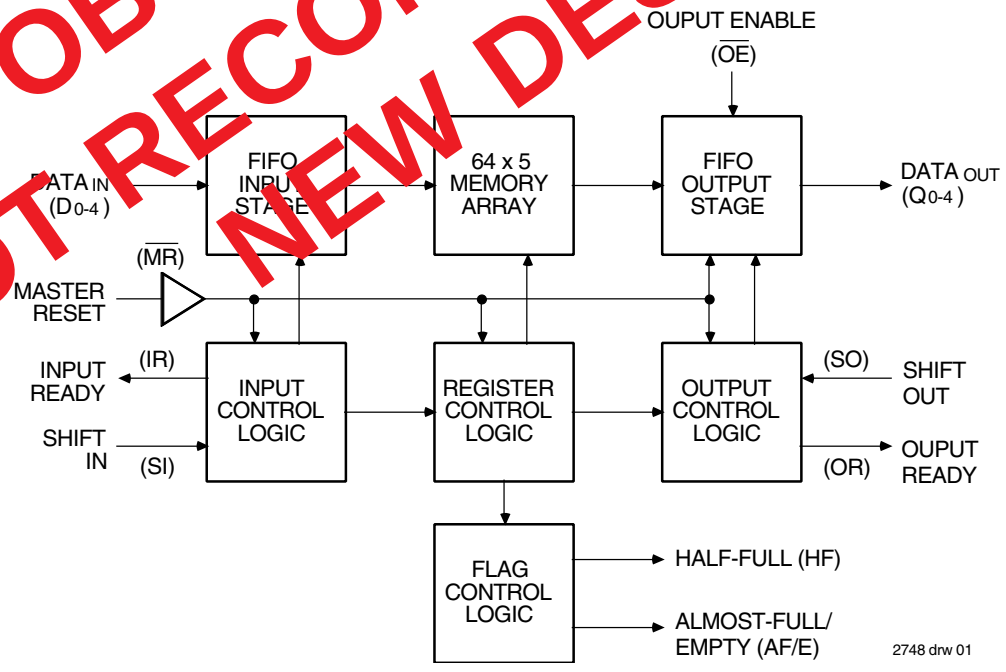
The IDT72413 is a 64 x 5, high-speed First-In/First-Out (FIFO) that loads and empties data on a first-in-first-out basis. It is expandable in bit width. All speed versions are cascad-able in depth.

The FIFO has a Half-Full Flag, which signals when it has 32 or more words in memory. The Almost-Full/Empty Flag is active when there are 56 or more words in memory or when there are 8 or less words in memory.

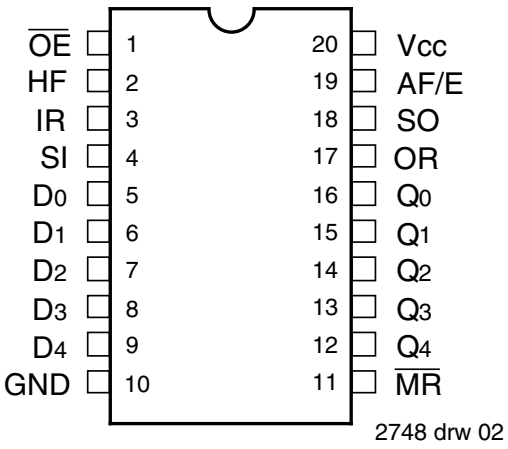
This device is pin and functionally compatible to the MI6413. It operates at a shift rate of 45MHz. This makes it ideal for use in high-speed data buffering applications. This FIFO can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers.

The IDT72413 is fabricated using high-performance CMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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PLASTIC DIP (P20-1, ORDER CODE: P)
SOIC (SO20-2, ORDER CODE: SO)
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

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NOTE:
1. Characterized values, not currently tested.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Commercial	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions			IDT72413 Commercial f_{IN} = 45, 35, 25 MHz Min.	Max.	Unit
I_{IL}	Low-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}			–10	—	µA
IIH	High-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}			—	10	µA
V_{OL}	Low-Level Output Current	V_{CC} = Min.	I_{OL} (Q_{0-4})	24 mA	—	0.4	V
			I_{OL} (IR, OR)(1)	8mA			
			I_{OL} (HF, AF/E)	8mA			
V_{OH}	High-Level Output Current	V_{CC} = Min.	I_{OH} (Q_{0-4})	–4mA	2.4	—	V
			I_{OH} (IR, OR)	–4mA			
			I_{OH} (HF, AF/E)	–4mA			
I_{OS}(2)	Output Short-Circuit Current	V_{CC} = Max.	V_O = 0V		–20	–110	mA
I_{HZ}	HIGH Impedance Output Current	V_{CC} = Max.	V_O = 2.4V		—	20	µA
I_{LZ}	LOW Impedance Output Current	V_{CC} = Max.	V_O = 0.4V		–20	—	µA
I_{CC}(3,4)	Active Supply Current	V_{CC} = Max., $\overline{OE}$ = HIGH Inputs LOW, f = 25MHz			—	60	mA

NOTES:
1. Care should be taken to minimize as much as possible the DC and capactive load on IR and OR when operating at frequencies above 25MHz.
2. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Guaranteed by design, but not currently tested.
3. Tested with outputs open (I_{OUT} = 0).
4. For frequencies greater than 25MHz, I_{CC} = 60mA + (1.5mA x [f –25MHz])

OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Figure	Commercial						Unit
			IDT72413L45		IDT72413L35		IDT72413L25		
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	16	—	ns
t_{SIL}[1]	Shift in LOW TIme	2	11	—	17	—	20	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	25	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	16	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	20	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	30	—	35	—	ns
t_{MRS}	Master Reset Pulse to SI	8	20	—	35	—	35	—	ns

NOTE:

1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between VCC and GND with very short lead length is recommended.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Figure	Commercial						Unit
			IDT72413L45		IDT72413L35		IDT72413L25		
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{IN}	Shift In Rate	2	—	45	—	35	—	25	MHz
t_{IRL}[1]	Shift In ↑ to Input Ready LOW	2	—	18	—	18	—	28	ns
t_{IRH}[1]	Shift In ↓ to Input Ready HIGH	2	—	18	—	20	—	25	ns
f_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	MHz
t_{ORL}[1]	Shift Out ↓ to Output Ready LOW	5	—	18	—	18	—	28	ns
t_{ORH}[1]	Shift Out ↓ to Output Ready HIGH	5	—	19	—	20	—	25	ns
t_{ODH}[1]	Output Data Hold Previous Word	5	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift Next Word	5	—	19	—	20	—	20	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	25	—	28	—	40	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8	—	25	—	28	—	30	ns
t_{MRIRH}[3]	Master Reset ↑ to Input Ready HIGH	8	—	25	—	28	—	30	ns
t_{MRIRL}[2]	Master Reset ↓ to Input Ready LOW	8	—	25	—	28	—	30	ns
t_{MRQ}	Master Reset ↓ to Outputs LOW	8	—	20	—	25	—	35	ns
t_{MRHF}	Master Reset ↓ to Half-Full Flag	8	—	25	—	28	—	40	ns
t_{MRAFE}	Master Reset ↓ to AF/E Flag	8	—	25	—	28	—	40	ns
t_{IPH}[3]	Input Ready Pulse HIGH	4	5	—	5	—	5	—	ns
t_{OPH}[3]	Output Ready Pulse HIGH	7	5	—	5	—	5	—	ns
t_{ORD}[3]	Output Ready ↑ HIGH to Valid Data	5	—	5	—	5	—	7	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	9	—	28	—	28	—	40	ns
t_{AEL}	Shift In ↑ to AF/E	9	—	28	—	28	—	40	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	10	—	28	—	28	—	40	ns
t_{AFH}	Shift In ↑ to AF/E HIGH	10	—	28	—	28	—	40	ns
t_{HFH}	Shift In ↑ to HF HIGH	11	—	28	—	28	—	40	ns
t_{HFL}	Shift Out ↑ to HF LOW	11	—	28	—	28	—	40	ns
t_{PHZ}[3]	Output Disable Delay	12	—	12	—	12	—	15	ns
t_{PLZ}[3]		12	—	12	—	12	—	15	
t_{PLZ}[3]	Output Enable Delay	12	—	15	—	15	—	20	ns
t_{PHZ}[3]		12	—	15	—	15	—	20	

NOTES:

1. Since the FIFO is a very high-speed device, care must be taken in the design of the hardware and the timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between VCC and GND with very short lead length is recommended.
2. If the FIFO is full, (IR = HIGH), $\overline{MR}$ ↑ forces IR to go LOW, and $\overline{MR}$ ↓ causes IR to go HIGH.
3. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

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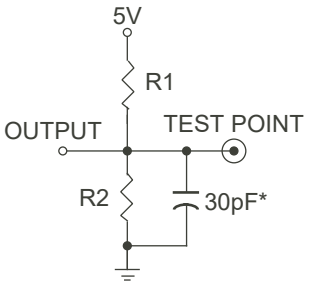
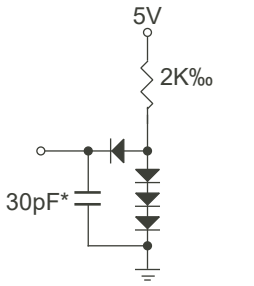
STANDARD TEST LOAD



DESIGN TEST LOAD



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or equivalent circuit
*Including scope and jig

RESISTOR VALUES FOR STANDARD TEST LOAD

I_{OL}	R1	R2
24mA	200Ω	300Ω
12mA	390Ω	760Ω
8mA	600Ω	1200Ω

Figure 1. Output Load

FUNCTIONAL DESCRIPTION:

The IDT72413, 65 x 5 FIFO is designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q_{0-4}) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes the Input Ready (IR) to go LOW. On the HIGH-to-LOW transition of SI, the write pointer is moved to the next word position and IR goes HIGH indicating the readiness to accept new data. If the FIFO is full, IR will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, OR will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty OR goes LOW on the LOW-to-HIGH transition of SO.

FALL-THROUGH MODE

The FIFO operates in a Fall-Through Mode when data gets shifted into an empty FIFO. After the fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH.

A Fall-Through Mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO. The fall-through delay of a RAM-based FIFO (one clock cycle) is far less than the delay of a Shift register-based FIFO.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA INPUT (D_{0-4})

Data input lines. The IDT72413 has a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D0-4 lines. The data has to meet set-up and hold time requirements with respect to the rising edge of SI.

SHIFT OUT (SO)

Shift Out controls the outputs data from the FIFO.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

HALF-FULL FLAG (HF)

Half-Full Flag signals when the FIFO has 32 or more words in it.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW, the FIFO is unavailable for new input data, IR is also used to cascade many FIFOs together, as shown in Figure 13.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Q_{0-4}) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. OR is also used to cascade many FIFOs together, as shown in Figure 13.

OUTPUT ENABLE ($\overline{OE}$)

Output Enable is used to enable the FIFO outputs onto a bus. $\overline{OE}$ is active LOW.

ALMOST-FULL/EMPTY FLAG (AF/E)

Almost-Full/Empty Flag signals when the FIFO is 7/8 full (56 or more words) or 1/8 from empty (8 or less words).

OUTPUTS:

DATA OUTPUT (Q_{0-4})

Data output lines, three-state. The IDT72413 has a 5-bit output.

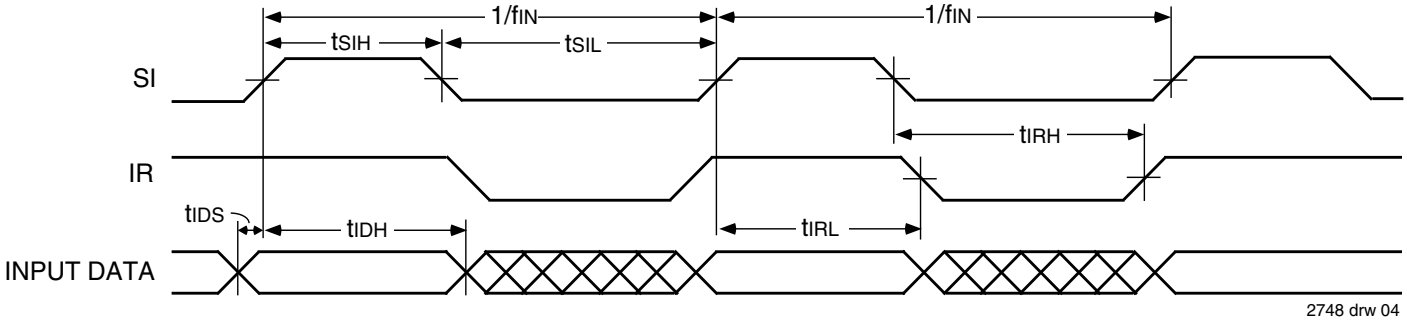
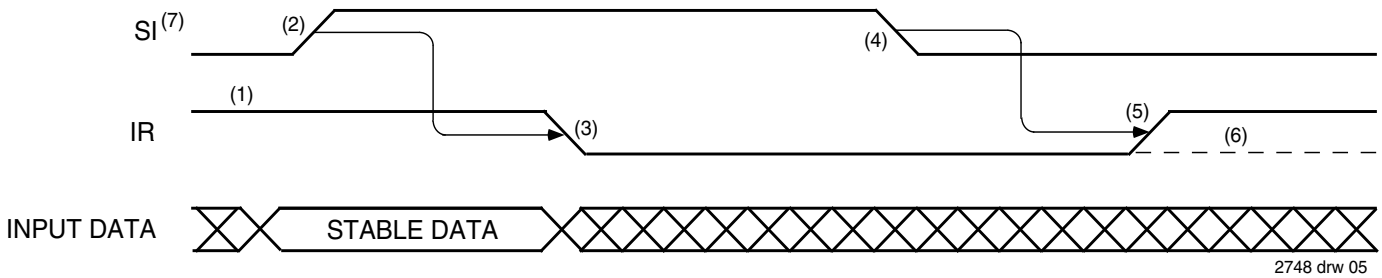


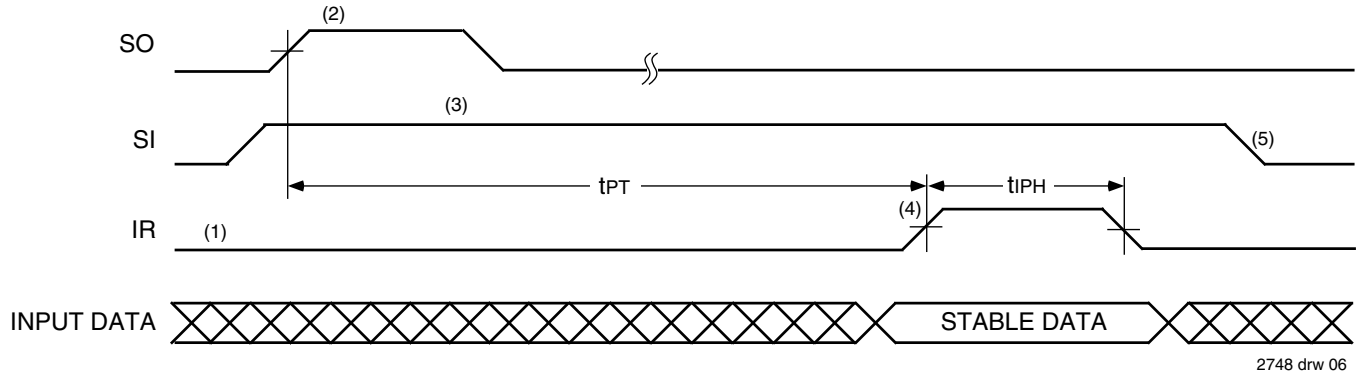
Figure 2. Input Timing



NOTES:

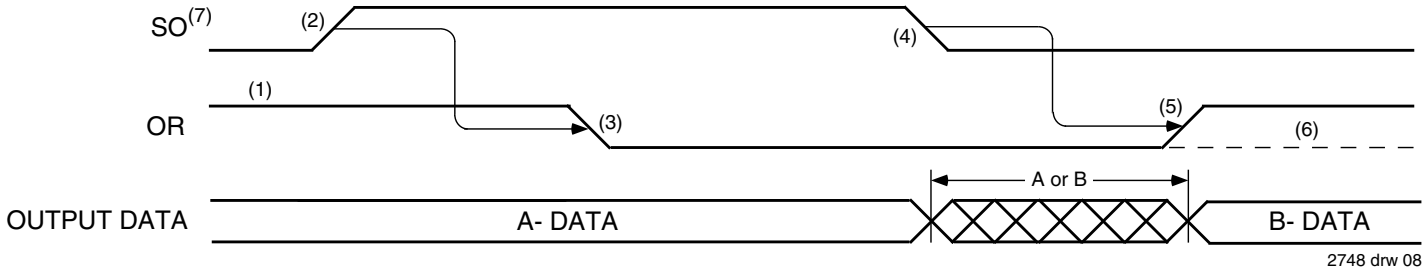
1. IR HIGH indicates space is available and a SI pulse may be applied.
2. Input Data is loaded into the FIFO.
3. IR goes LOW indicating the FIFO is unavailable for new data.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full, then IR remains LOW.
7. SI pulses applied while IR is LOW will be ignored (see Figure 4).

Figure 3. The Machanism of Shifting Data Into the FIFO



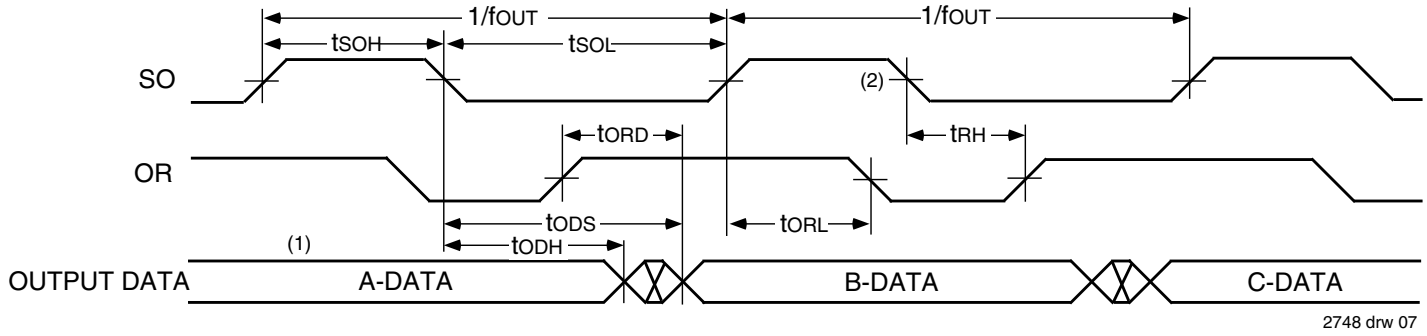
NOTES:
1. FIFO is initially full.
2. SO pulse is applied.
3. SI is held HIGH.
4. As soon as IR becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. SI should not go LOW until (t_{PT} + t_{IPH}).

Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH



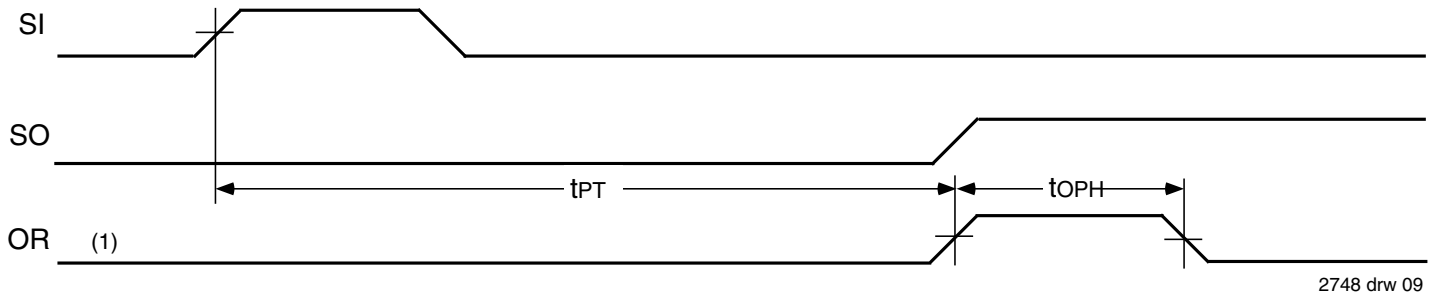
NOTES:
1. This data is loaded consecutively A, B, C.
2. Output data changes on the falling edge of SO after a valid SO sequence, i.e., OR and SO are both HIGH together.

Figure 5. Output TIming



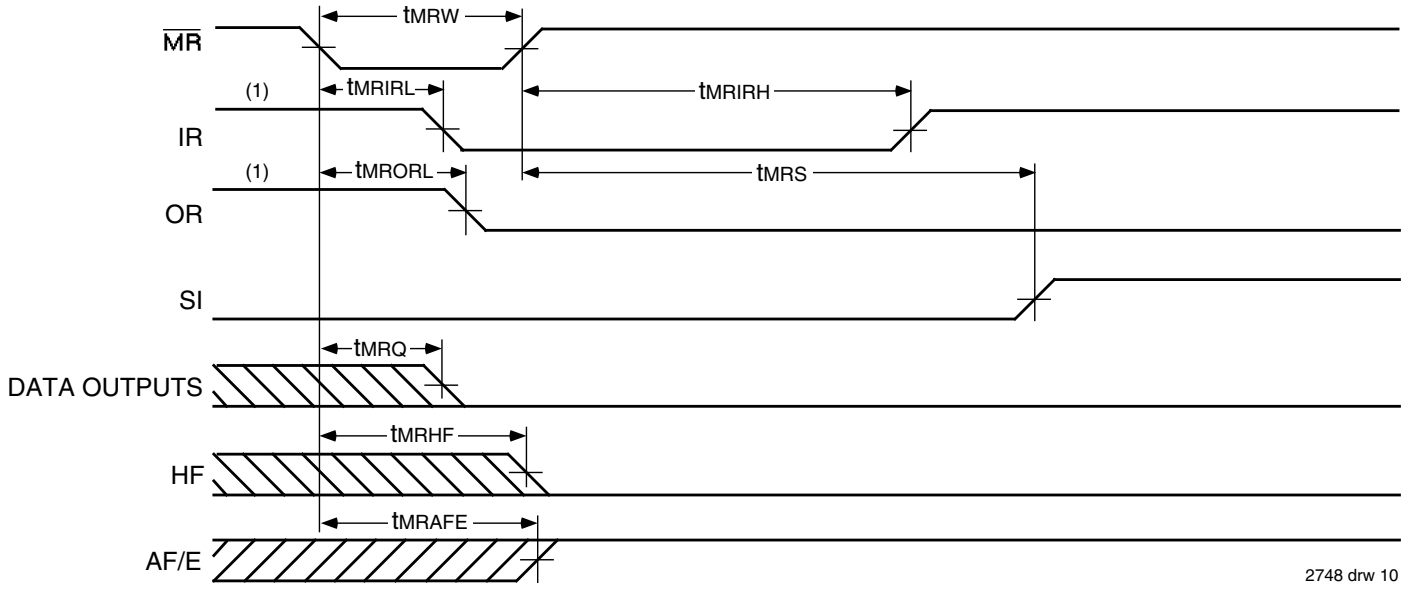
NOTES:
1. OR HIGH indicates that data is available and a SO pulse may be applied.
2. SO goes HIGH causing the next step.
3. OR goes LOW.
4. Read pointer is incremented.
5. OR goes HIGH indicating that new data (B) will be available at the FIFO outputs after t_{ORD} ns.
6. If the FIFO has only one word loaded (A DATA) , OR stays LOW and the A-DATA remains unchanged at the outputs.
7. SO pulses applied when OR is LOW will be ignored.

Figure 6. The Mechanism of Shifting Data Out of the FIFO



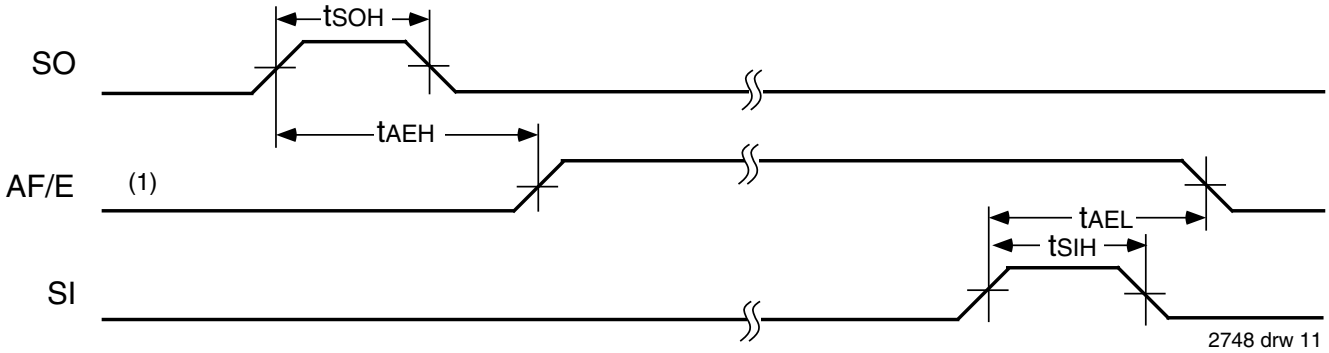
NOTE:
1. FIFO initailly empty.

Figure 7. t_{PT} and t_{OPH} Specification



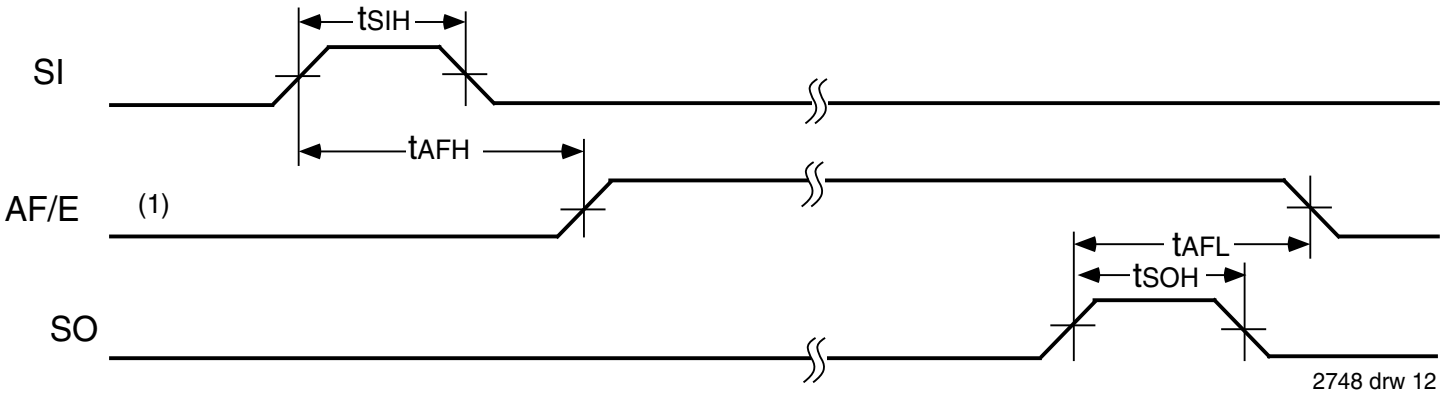
NOTE:
1. FIFO is partially full.

Figure 8. Master Reset Timing



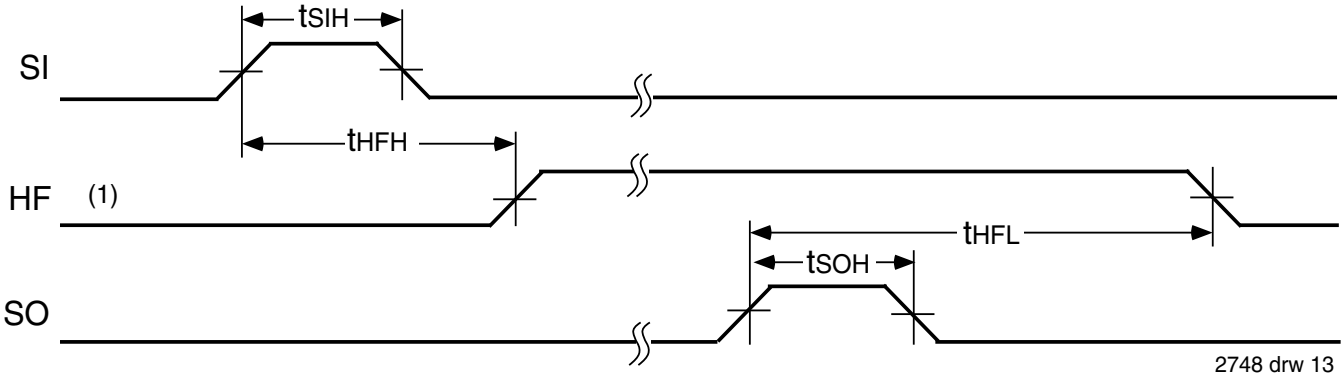
NOTE:
1. FIFO contains 9 words (one more than Almost-Empty).

Figure 9. t_{AEH} and t_{AEL} Specifications



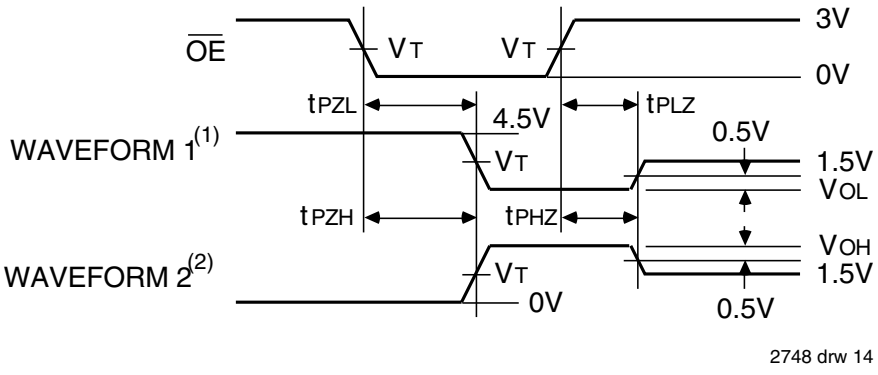
NOTE:
1. FIFO contains 55 words (one short of Almost-Full).

Figure 10. t_{AFH} and t_{AFL} Specifications



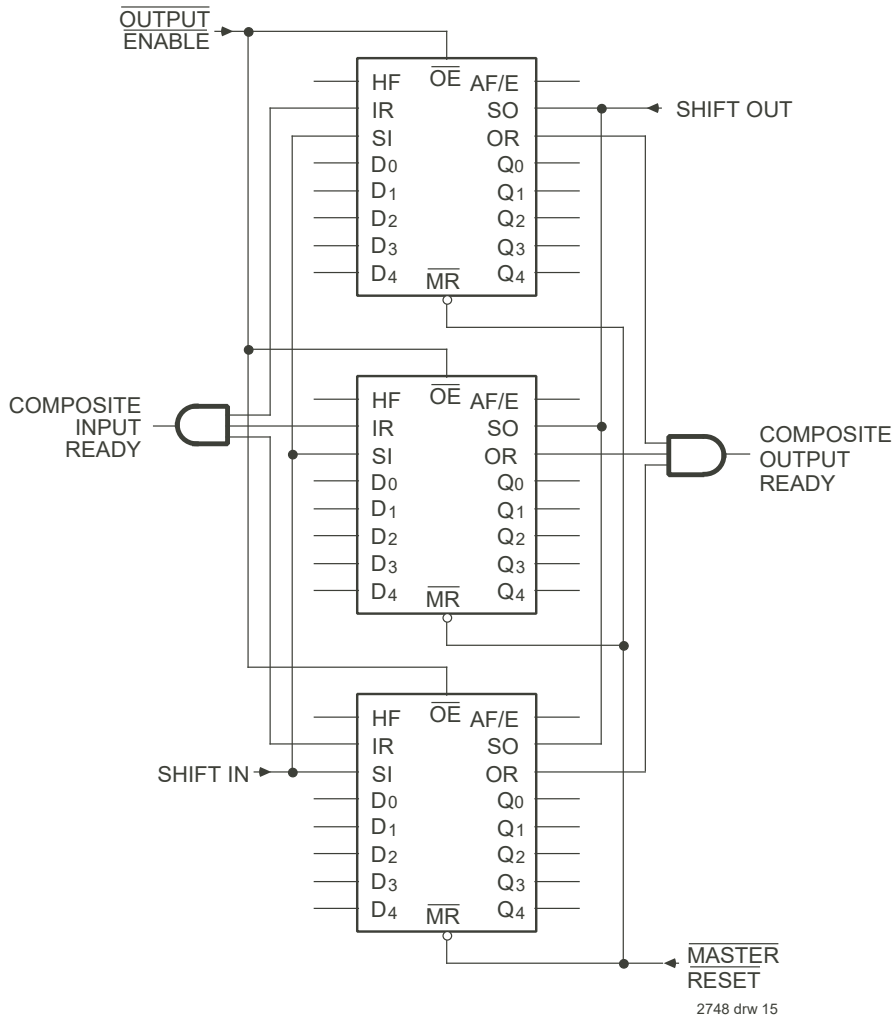
NOTE:
1. FIFO contains 31 words (one short of Half-Full).

Figure 11. t_{HFL} and t_{HFH} Specifications



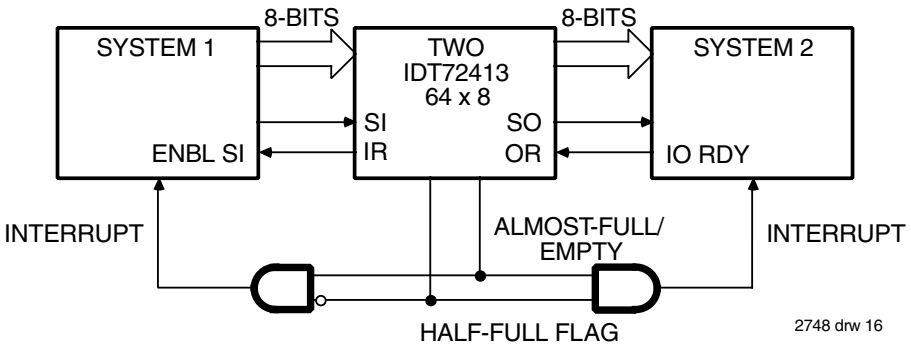
NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Figure 12. Enable and Disable



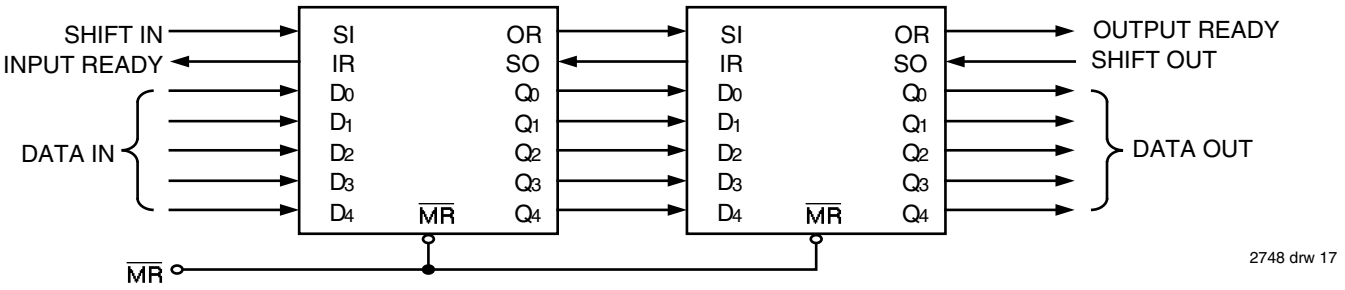
NOTE:
1. FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall-through times of the FIFOs.

Figure 13. 64 x 15 FIFO with IDT72413



NOTE:
1. Cascading the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

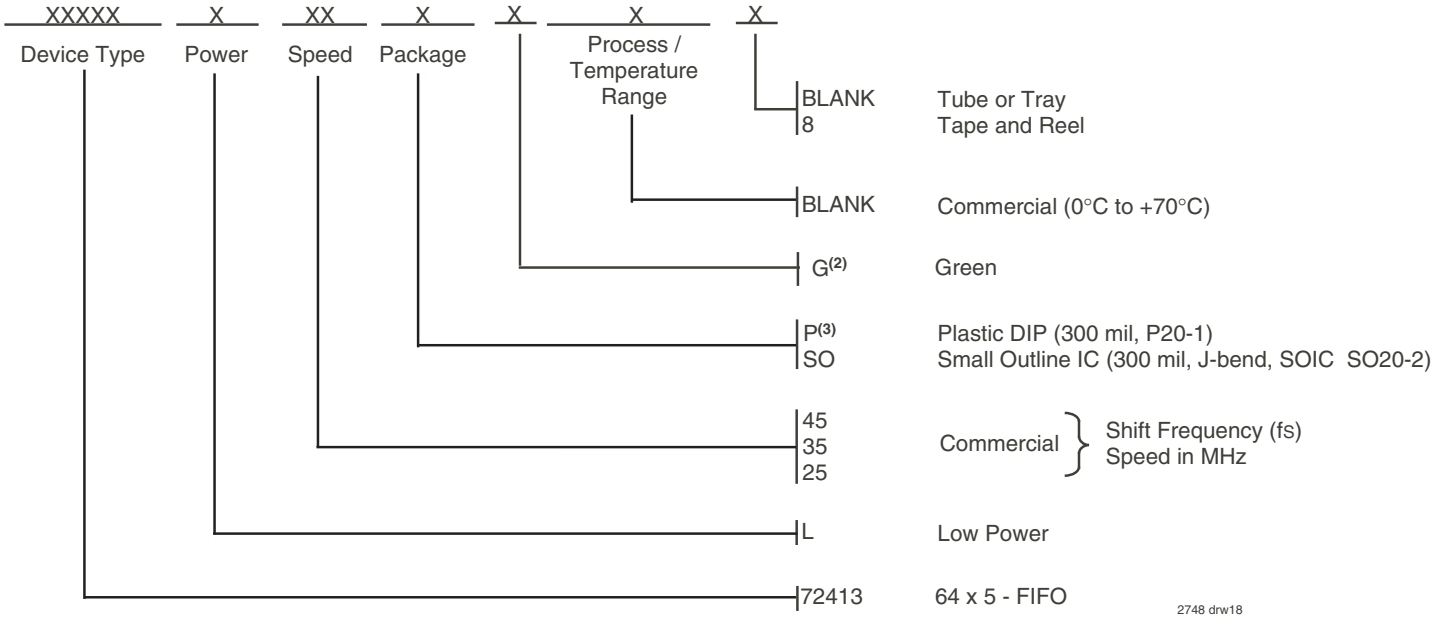
Figure 14. Application for IDT72413 for Two Asynchronous Systems



NOTE:
1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 15. 128 x 5 Depth Expansion

ORDERING INFORMATION



NOTES:
1. Industrial temperature range is available by special order.
2. Green parts are available, for specific speeds and packages contact your sales office.
3. For "P", Plastic Dip, when ordering green package, the suffix is "PDG".

DATASHEET DOCUMENT HISTORY

07/10/2003	pgs. 1, 2, 3, and 10.
02/11/2009	pgs. 1 and 10.
06/29/2012	pgs. 1, 2, 9 and 10.
11/21/2014	PDN# CQ-14-08 issued. See IDT.com for PDN specifics.
08/08/2019	Datasheet changed to Obsolete Status.

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