Product Specification

PE4273

SPDT Broadband UltraCMOS®
5 – 3000 MHz RF Switch

Features

- Single-pin or complementary CMOS logic control inputs
- High ESD tolerance of 1.5 kV
- Low insertion loss
  - 0.50 dB at 1000 MHz
  - 0.65 dB at 2000 MHz
- Isolation
  - 34.5 dB at 1000 MHz
  - 25 dB at 2000 MHz
- Typical input 1 dB compression point of +32 dBm
- Package type 6-lead SC-70

Product Description

The PE4273 RF Switch is designed for the TV tuner, PCTV, set top box, DTV, DVR and general broadband applications. This device offers industry leading broadband linearity, 1.5 kV ESD tolerance and a simple CMOS interface. It offers a simple alternative solution to pin diode and mechanical relay switches.

The PE4273 SPDT Broadband RF Switch is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

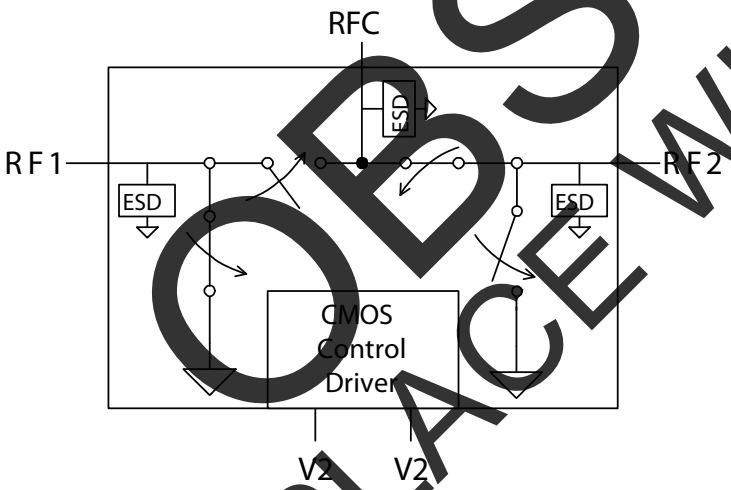


Figure 2. Package Type
6-lead SC-70

Table 1. Electrical Specifications @ +25°C, V_{DD} = 3V (Z_S = Z_L = 75 Ω)

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency	5 - 3000 MHz	5		3000	MHz
Insertion Loss	1000 MHz 2000 MHz		0.50 0.65	0.60 0.75	dB dB
Isolation (RFC - RF1/RF2)	1000 MHz 2000 MHz	32.5 23	34.5 25		dB dB
Isolation (RF1 - RF2)	1000 MHz 2000 MHz	38.5 26	40.5 28		dB dB
Return Loss	1000 MHz 2000 MHz		18.5 14		dB dB
'ON' Switching Time [2]	50% CTRL to 0.1 dB of final value, 1 GHz		0.725	1.5	µs
'OFF' Switching Time [2]	50% CTRL to 25 dB isolation, 1 GHz		0.625	1.3	µs
Video Feedthrough [1,2]			< 2		mV_{pp}
Input 1 dB Compression [2]	5 MHz 1000 MHz	28 30	29 32		dBm dBm
Input IP3 [2]	5 MHz, 19 dBm input power 1000 MHz, 19 dBm input power		54 53		dBm dBm

Notes: 1. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth
2. Measured in a 50 Ω system

Figure 3. Pin Configuration (Top View)

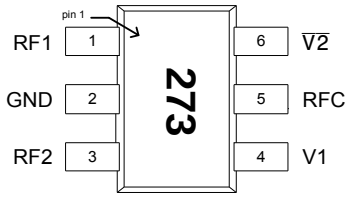


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1	RF Port1 [1]
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2	RF Port2 [1]
4	V1	Switch control input, CMOS logic level.
5	RFC	RF Common [1]
6	V2	This pin supports two interface options: *Single-pin control mode.* A nominal 3-volt supply connection is required. *Complementary-pin control mode.* A complementary CMOS control signal to V1 is supplied to this pin.

Note: 1. All RF pins must be DC blocked with an external series capacitor or held at 0 VDC

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V1 = 3V, V2= 3V)		8	50	µA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50 Ω) 100 - 3000 MHz 5 - 100 MHz		+34 +32	dBm dBm
V_{ESD}	ESD Voltage (HBM, ML_STD 883 Method 3015.7)		1500	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

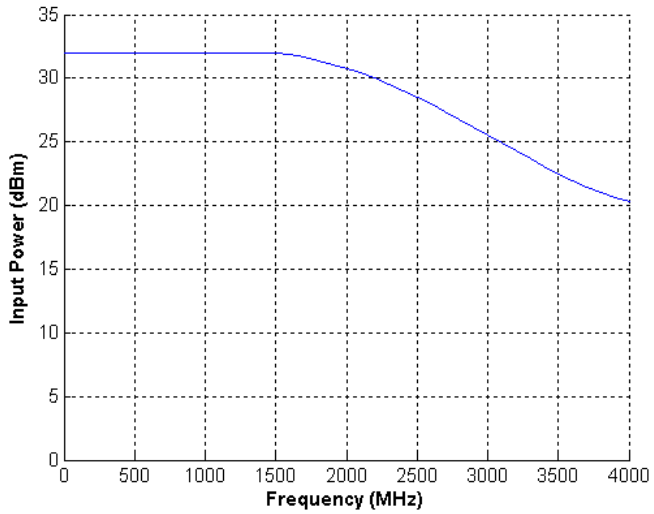
Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 4*.

Figure 4. Maximum Operating Input Power [1]



Note: 1. Operating within DC limits (*Table 3*)

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V2) = V_{DD} Pin 4 (V1) = High	RFC to RF1
Pin 6 (V2) = V_{DD} Pin 4 (V1) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V2) = Low Pin 4 (V1) = High	RFC to RF1
Pin 6 (V2) = High Pin 4 (V1) = Low	RFC to RF2

Control Logic Input

The PE4273 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection (pin 6). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS µProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins V1 and V2 (pins 4 and 6), that can be directly driven by +3-volt CMOS logic or a suitable µProcessor I/O port. This enables the PE4273 to operate in positive control voltage mode within the PE4273 operating limits.

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4273 SPDT switch. The RF common port is connected through a 75 Ω transmission line to the bottom F connector, J2. Port 1 and Port 2 are connected through 75 Ω transmission lines to two F connectors on either side of the board, J3 and J1. A through transmission line connects F connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.021", trace gaps of 0.030", dielectric thickness of 0.028", copper thickness of 0.0021" and ε_r of 4.3.

J6 and J7 provide a means for controlling the DC inputs to the device. The lower left header (J6) is connected to the device V1 input. The lower right header (J7) is connected to the device V2 input. Series resistors (R1 and R2) are provided to reduce the package resonance between RF and DC lines. Footprints for decoupling capacitors (100 pF) are provided on both V1 and V2 traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 5. Evaluation Board Layouts
Peregrine Specification 101/0245

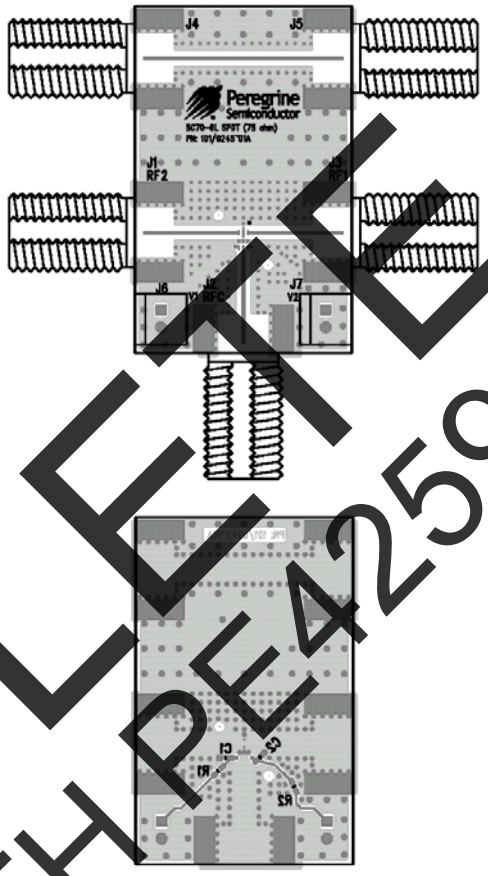
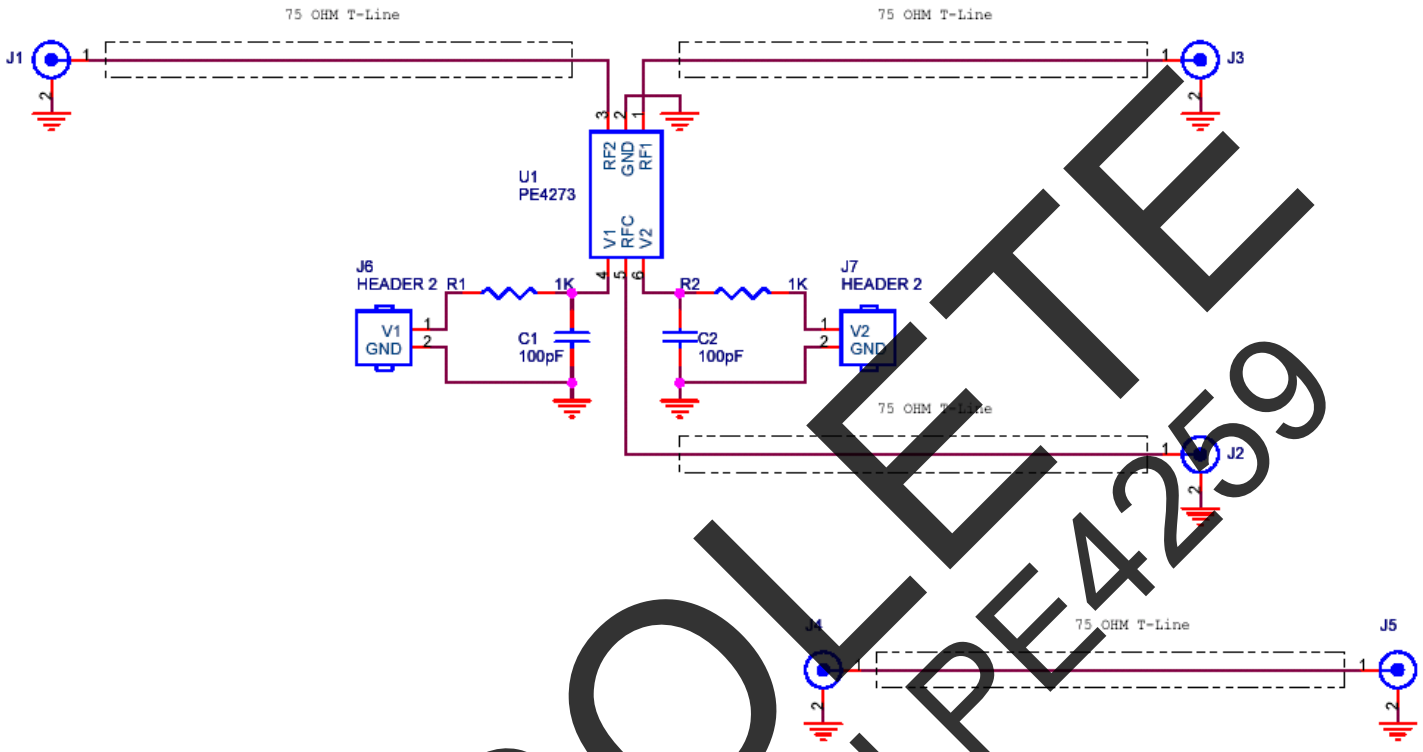


Figure 6. Evaluation Board Schematic
Peregrine Specification 102/0311



Typical Performance Data

Figure 7. Isolation: RF1 - RF2 @ 25°C

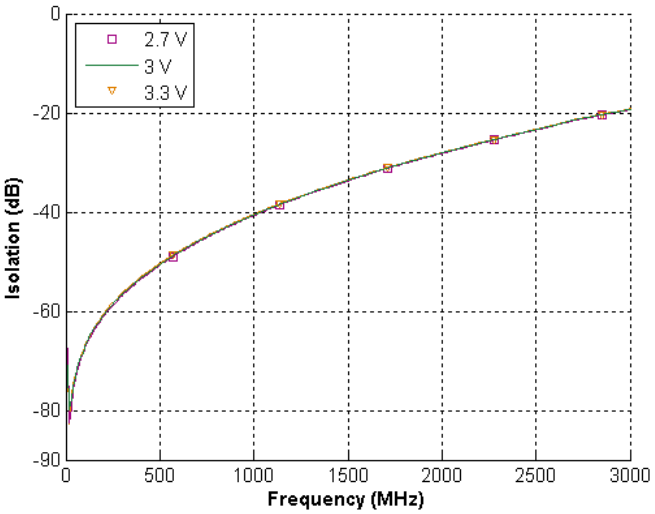


Figure 8. Isolation: RF1 - RF2 @ 3.0V

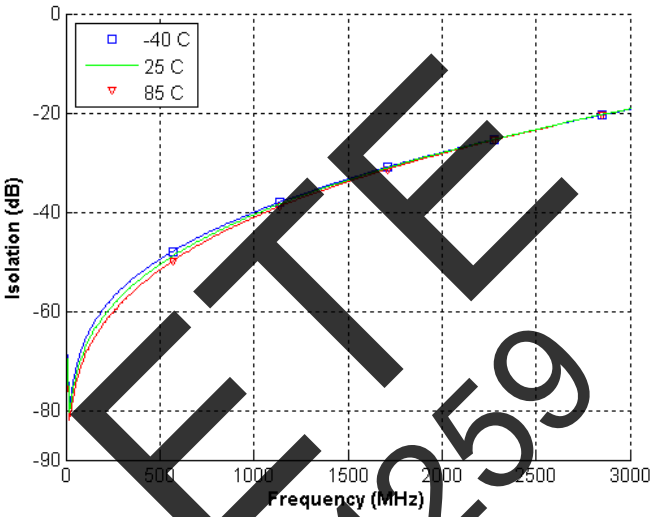


Figure 9. Isolation: RFC - RF1/RF2 @ 25°C

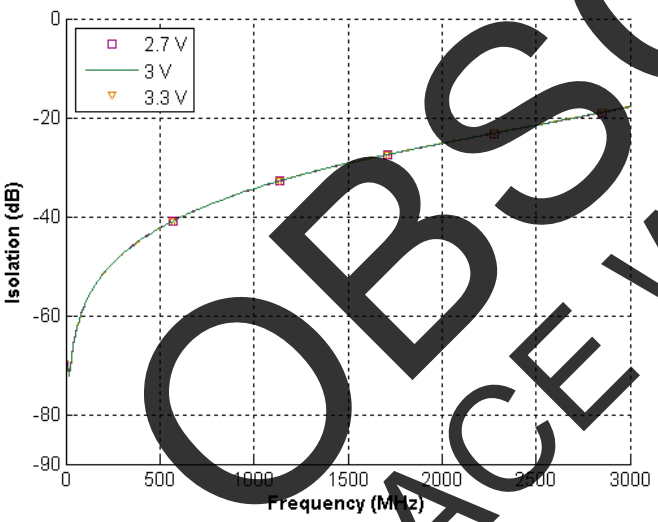
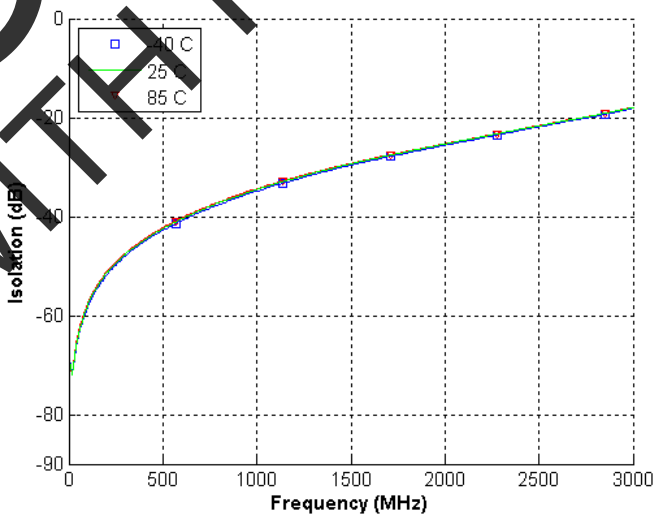


Figure 10. Isolation: RFC - RF1/RF2 @ 3.0V



Typical Performance Data

Figure 11. Insertion Loss @ 25°C

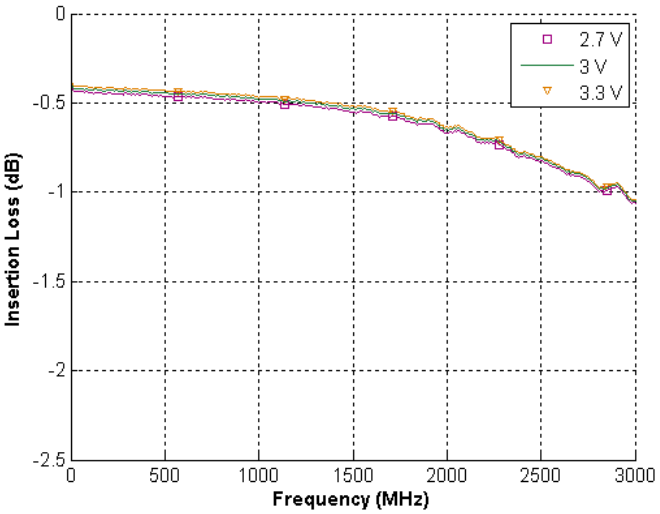


Figure 12. Insertion Loss @ 3.0V

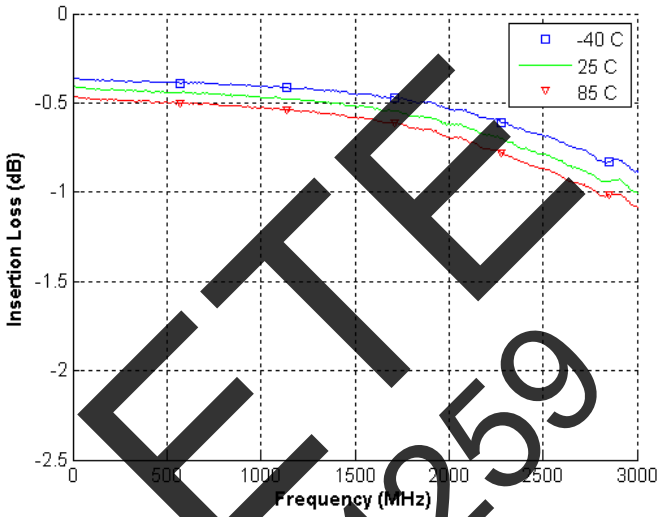


Figure 13. Return Loss: RF1/RF2 @ 25°C

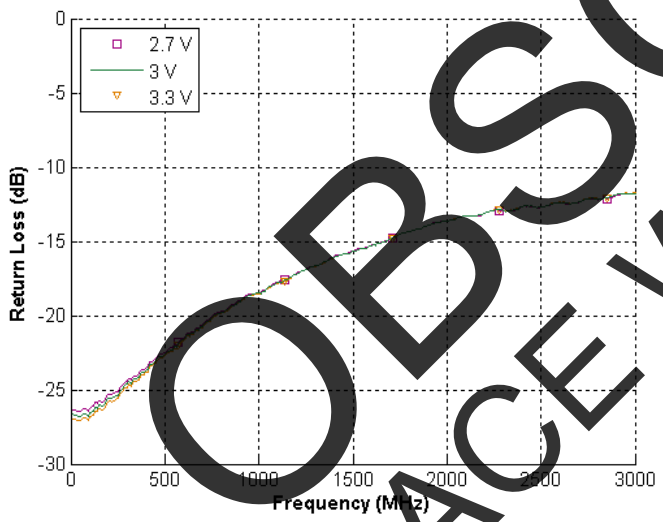
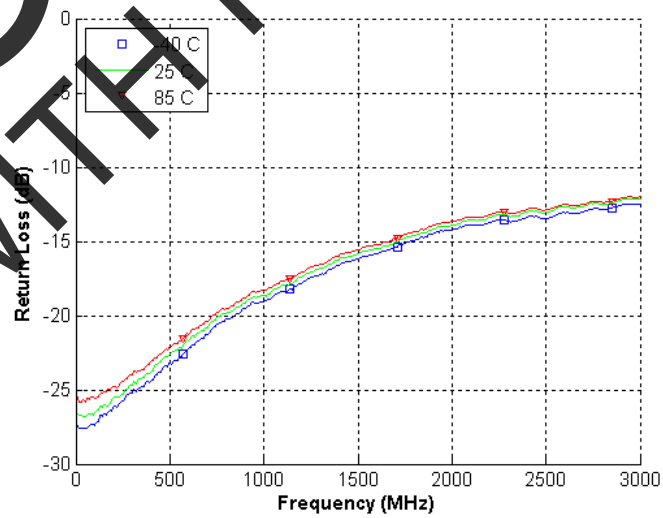


Figure 14. Return Loss: RF1/RF2 @ 3.0V



Typical Performance Data

Figure 15. Return Loss: RFC/RF1 @ 25°C

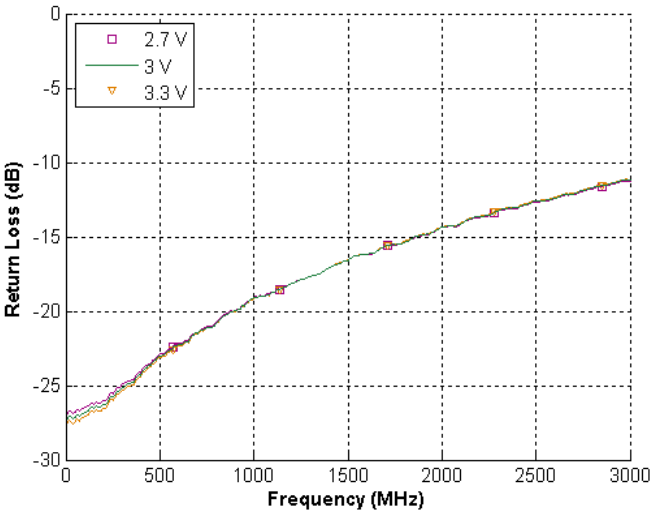


Figure 16. Return Loss: RFC/RF1 @ 3.0V

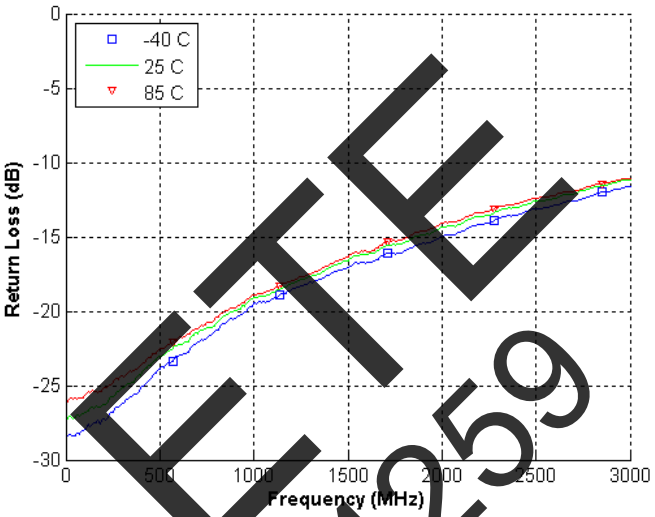


Figure 17. Return Loss: RFC/RF2 @ 25°C

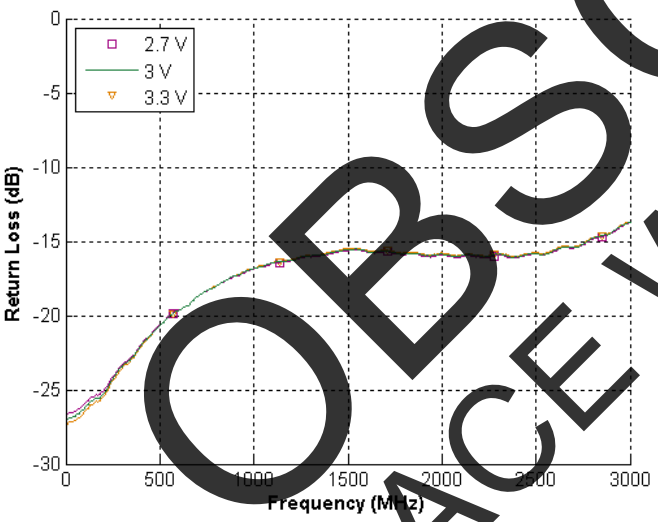
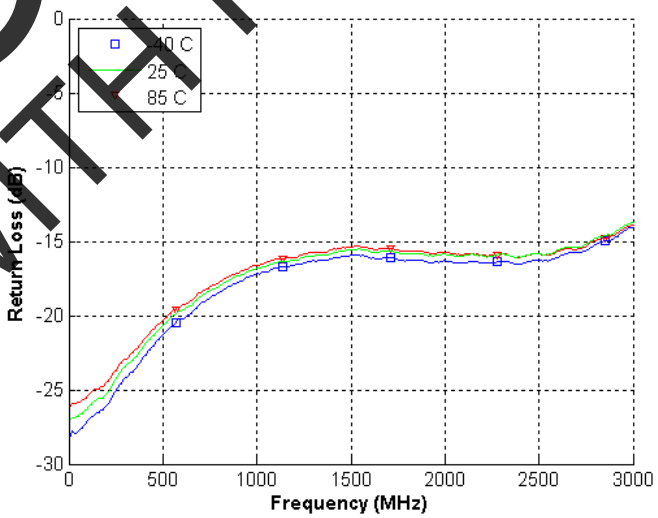


Figure 18. Return Loss: RFC/RF2 @ 3.0V



Typical Performance Data

Figure 19. Input 1 dB Compression and IIP3

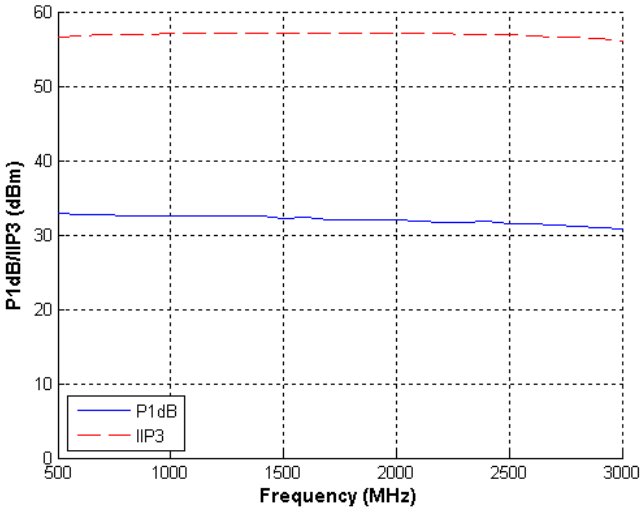


Figure 20. Package Drawing

6-lead SC-70

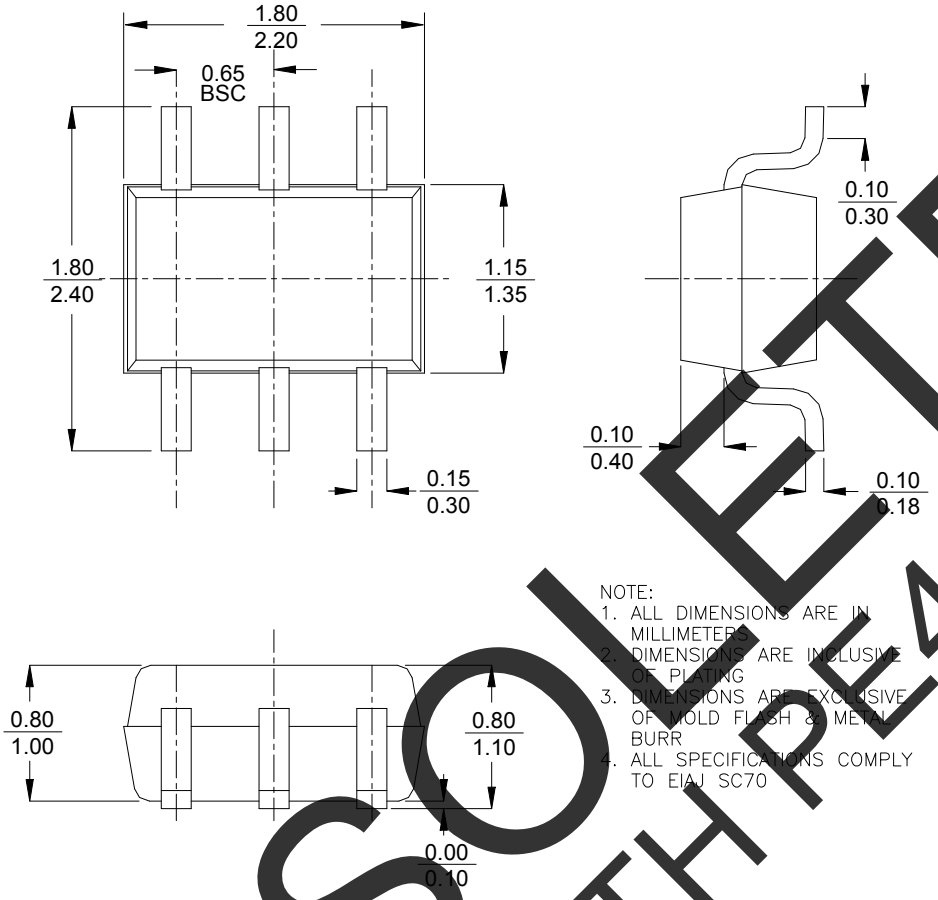
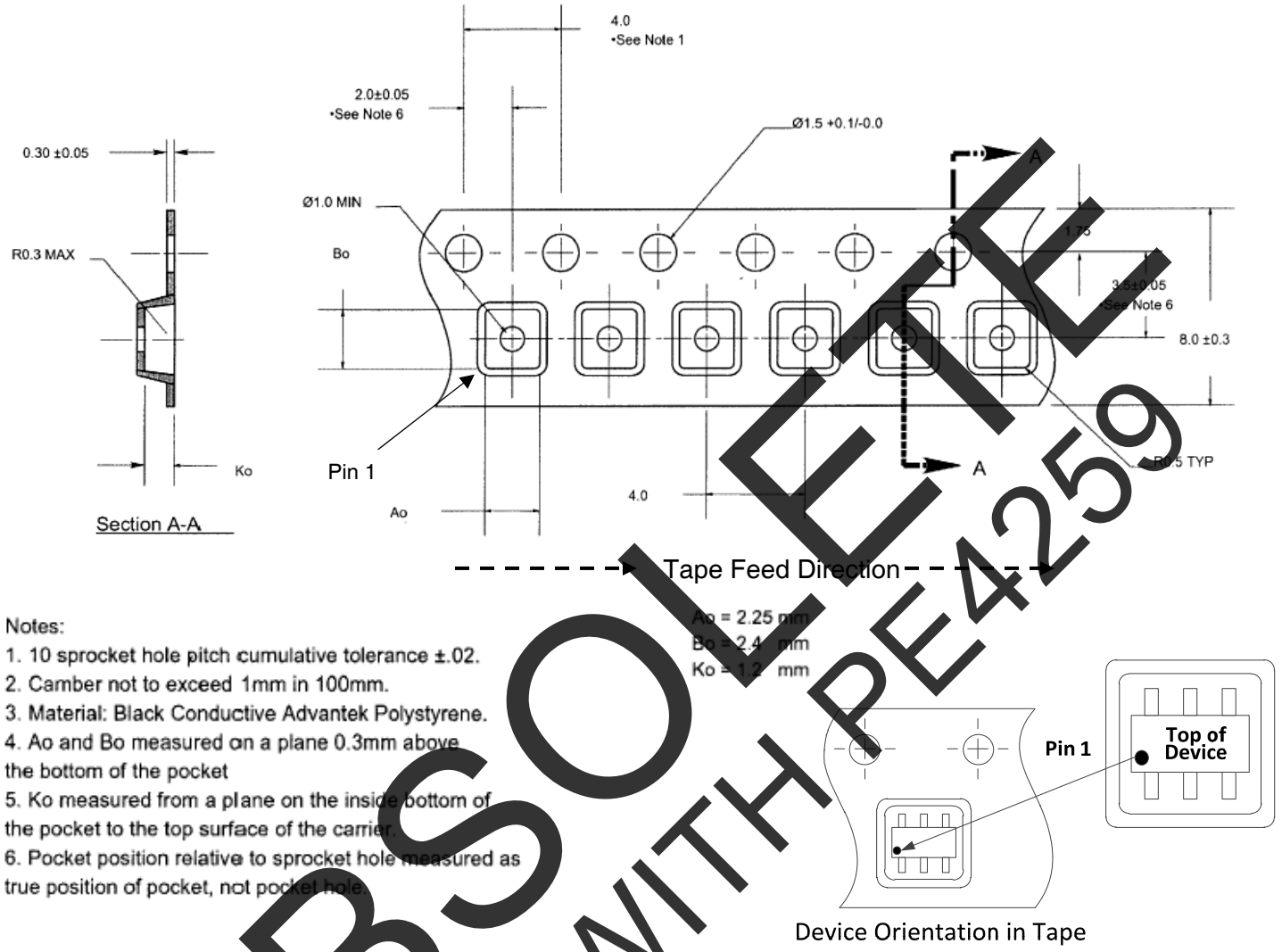


Figure 21. Tape and Reel Specifications



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4273-00	PE4273-EK	PE4273-06SC70-EK	Evaluation Kit	1 / Box
4273-51	273	PE4273G-06SC70-7680A	Green 6-lead SC-70	7680 units / Canister
4273-52	273	PE4273G-06SC70-3000C	Green 6-lead SC-70	3000 units / T&R

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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