Intelligent Power Module (IPM)

600 V, 30 A

STK581U3C2D-E

ON Semiconductor®

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SIP22 70x31.1
CASE 127BU

Overview

This “Inverter IPM” is highly integrated device containing all High Voltage (HV) control from HV−DC to 3−phase outputs in a single SIP module (Single−In line Package). Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

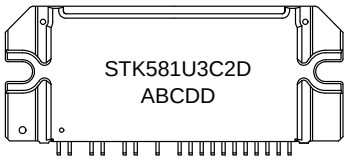
Features

- Single Control Power Supply due to Internal Bootstrap Circuit for High Side Pre−driver Circuit
- All Control Input and Status Output are at Low Voltage Levels directly compatible with Microcontrollers
- Built−in Cross Conduction Prevention
- Externally accessible Embedded Thermistor for Substrate Temperature Measurement
- The Level of the Over−current Protection Current is adjustable with the External Resistor, “RSD”
- These Devices are Pb−Free and are RoHS Compliant

Certification

- UL1557 (File number : E339285)

MARKING DIAGRAM



STK581U3C2D = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot code
Device marking is on package underside

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

Specifications

ABSOLUTE MAXIMUM RATINGS (at Tc = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	P to N, surge < 500 V (Note 1)	450	V
Collector−emitter voltage	V_{CE}	P to U,V,W or U,V,W to N	600	V
Output current	Io	P, N, U,V,W terminal current	±30	A
		P, N, U,V,W terminal current at Tc = 100°C	±15	A
Output peak current	Iop	P, N, U,V,W terminal current for a Pulse width of 1 ms	±45	A
Pre−driver voltage	VD1,2,3,4	VB1 to U, VB2 to V, VB3 to W, V_{DD} to V_{SS} (Note 2)	20	V
Input signal voltage	V_{IN}	HIN1, 2, 3, LIN1, 2, 3	–0.3 to V_{DD}	V
FAULT terminal voltage	VFAULT	FAULT terminal	–0.3 to V_{DD}	V
Maximum power dissipation	Pd	IGBT per channel	49	W
Junction temperature	Tj	IGBT, FRD	150	°C
Storage temperature	Tstg		–40 to +125	°C
Operating case temperature	Tc	IPM case temperature	–40 to +100	°C
Tightening torque		Case mounting screws (Note 3)	1.17	Nm
Withstand voltage	Vis	50 Hz sine wave AC 1 minute (Note 4)	2000	VRMS

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

1. Surge voltage developed by the switching operation due to the wiring inductance between "P" and "N" terminal.
2. Terminal voltage : VD1 = VB1 to U, VD2 = VB2 to V, VD3 = VB3 to W, VD4 = V_{DD} to V_{SS}
3. Flatness of the heat−sink should be 0.15 mm and below.
4. Test conditions : AC 2500 V, 1 s.

ELECTRICAL CHARACTERISTICS (at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V, V_{CC} = 300 V, L = 3.5 mH)

Parameter	Symbol	Conditions		Test Circuit	Min	Typ	Max	Unit
Power Output Section								
Collector−emitter cut−off current	I_{CE}	V_{CE} = 600 V		Fig.1	−	−	0.1	mA
Bootstrap diode reverse current	IR(BD)	VR(BD)			−	−	0.1	mA
Collector to emitter saturation voltage	V_{CE}(SAT)	Ic = 30 A, Tj = 25°C	Upper side	Fig.2	−	1.8	2.7	V
			Lower side (Note 5)		−	2.1	3.0	
		Ic = 15 A, Tj = 100°C	Upper side		−	1.5	−	
			Lower side (Note 5)		−	1.7	−	
Diode forward voltage	VF	IF = 30 A, Tj = 25°C	Upper side	Fig.3	−	2.0	2.9	V
			Lower side (Note 5)		−	2.3	3.2	
		IF = 15 A, Tj = 100°C	Upper side		−	1.5	−	
			Lower side (Note 5)		−	1.7	−	
Junction to case thermal resistance	θj−c(T)	IGBT			−	−	2.5	°C/W
	θj−c(D)	FRD			−	−	3	
Control (Pre−driver) Section								
Pre−driver power dissipation	ID	VD1, 2, 3 = 15 V		Fig.4	−	0.08	0.4	mA
		VD4 = 15 V			−	1.6	4	

ELECTRICAL CHARACTERISTICS (at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V, V_{CC} = 300 V, L = 3.5 mH) (continued)

Parameter	Symbol	Conditions	Test Circuit	Min	Typ	Max	Unit
Control (Pre−driver) Section							
High level Input voltage	Vin H	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to V_{SS}		2.5	−	−	V
Low level Input voltage	Vin L			−	−	0.8	V
Input threshold voltage hysteresis (Note 5)	Vinth(hys)			0.5	0.8	−	V
Logic 1 input leakage current	I_{IN+}	V_{IN} = +3.3 V		−	100	143	μA
Logic 0 input leakage current	$I_{IN−}$	V_{IN} = 0 V		−	−	2	μA
FAULT terminal input electric current	IoSD	FAULT : ON / VFAULT = 0.1 V		−	2	−	mA
FAULT clear time	FLTCLR	Fault output latch time.		18	−	80	ms
V_{CC} and V_S undervoltage positive going threshold	V_{CCUV+} V_{SUV+}			10.5	11.1	11.7	V
V_{CC} and V_S undervoltage negative going threshold	$V_{CCUV−}$ $V_{SUV−}$			10.3	10.9	11.5	V
V_{CC} and V_S undervoltage hysteresis	V_{CCUVH} $V_{SUVH−}$			0.14	0.2	−	V
Over current protection level	ISD	PW = 100 μs, RSD = 0 Ω	Fig.5	38.5	−	48.2	A
Output level for current monitor	ISO	Io = 30 A		0.32	0.34	0.36	V
Switching Characterisitcs							
Switching time	t_{ON}	Io = 30 A	Fig.6	0.3	0.6	1.3	μs
	t_{OFF}			−	0.9	1.6	
Turn−on switching loss	Eon	Io = 30 A		−	800	−	μJ
Turn−off switching loss	Eoff			−	550	−	μJ
Total switching loss	Etot			−	1350	−	μJ
Turn−on switching loss	Eon	Io = 15 A, Tc = 100°C		−	530	−	μJ
Turn−off switching loss	Eoff			−	450	−	μJ
Total switching loss	Etot			−	980	−	μJ
Diode reverse recovery energy	Erec	I_F = 15 A, P = 400 V, Tc = 100°C		−	24	−	μJ
Diode reverse recovery time	trr			−	58	−	ns
Reverse bias safe operating area	RBSOA	Io = 45 A, V_{CE} = 450 V		Full square			
Short circuit safe operating area	SCSOA	V_{CE} = 400 V, Tc = 100°C		4	−	−	μs
Allowable offset voltage slew rate	dv/dt	Between U, V, W to N		−50	−	50	V/ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

5. The lower side's V_{CE}(SAT) and VF include a loss by the shunt resistance

Notes:

1. When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch.After protection operation ends,it returns automatically within about 18 ms to 80 ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre−drive power supply low voltage protection (UVLO : with hysteresis about 0.2 V) is as follows.

Upper side:
The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.

Lower side:
The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

2. When assembling the IPM on the heat sink with M3 type screw, tightening torque range is 0.79 Nm to 1.17 Nm.
3. The pre−drive low voltage protection is the feature to protect devices when the pre−driver supply voltage falls due to an operating malfunction.

RECOMMENDED OPERATING CONDITIONS (at Tc = 25°C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}	P to N	0	280	450	V
Pre−driver supply voltage	VD1, 2, 3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} (Note 6)	13.5	15	16.5	
ON−state input voltage	V_{IN}(ON)	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3	3.0	−	5.0	V
OFF−state input voltage	V_{IN}(OFF)		0	−	0.0	
PWM frequency	f_{PWM}		1	−	20	kHz
Dead time	DT	Turn−off to turn−on	2	−	−	μs
Allowable input pulse width	PWIN	ON and OFF	1	−	−	μs
Package mounting torque		‘M4’ type screw	0.79	−	1.17	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Pre−drive power supply (VD4 = 15 ±1.5 V) must have the capacity of Io = 20 mA (DC), 0.5 A (Peak).

MODULE PIN−OUT DESCRIPTION

Pin	Name	Description
1	VB1	High Side Floating Supply Voltage 1
2	U, VS1	Output 1 − High Side Floating Supply Offset Voltage
3	−	Without Pin
4	VB2	High Side Floating Supply voltage 2
5	V,VS2	Output 2 − High Side Floating Supply Offset Voltage
6	−	Without Pin
7	VB3	High Side Floating Supply voltage 1
8	W,VS3	Output 1 − High Side Floating Supply Offset Voltage
9	−	Without Pin
10	P	Positive Bus Input Voltage
11	−	Without Pin
12	N	Positive Bus Input Voltage
13	HIN1	Logic Input High Side Gate Driver − Phase U
14	HIN2	Logic Input High Side Gate Driver − Phase V
15	HIN3	Logic Input High Side Gate Driver − Phase W
16	LIN1	Logic Input Low Side Gate Driver − Phase U
17	LIN2	Logic Input Low Side Gate Driver − Phase V
18	LIN3	Logic Input Low Side Gate Driver − Phase W
19	FAULT	FAULT Output
20	ISO	Current monitor output
21	VDD	+15V Main Supply
22	VSS	Negative Main Supply

Equivalent Block Diagram

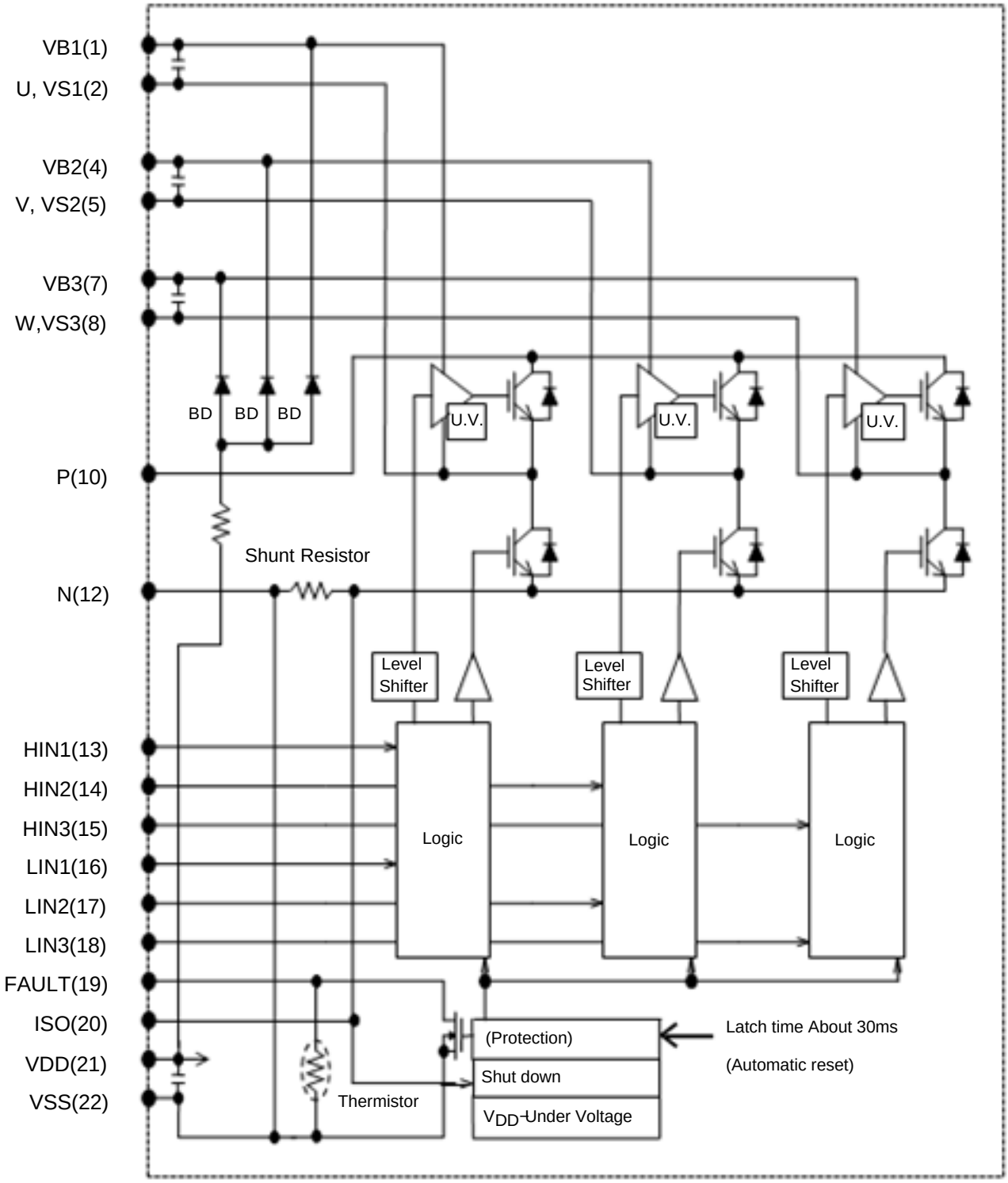


Figure 1. Block Diagram

Test Circuits

(The tested phase : U+ shows the upper side of the U phase and U− shows the lower side of the U phase.)

- ICE / IR(BD)

	U+	V+	W+	U−	V−	W−
M	10	10	10	2	5	8
N	2	5	8	12	12	12

	U(DB)	V(DB)	W(DB)
M	1	4	7
N	22	22	22

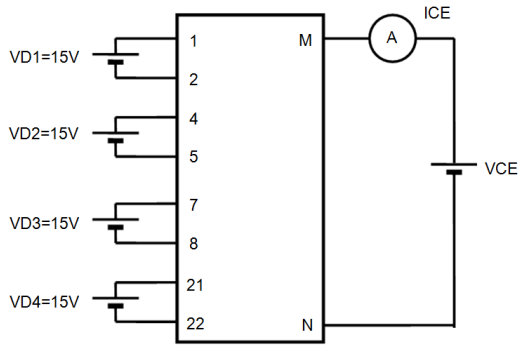


Figure 2. Test Circuit for ICE

- V_{CE}(SAT) (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	10	10	10	2	6	8
N	2	5	8	12	12	12
m	13	14	15	16	17	18

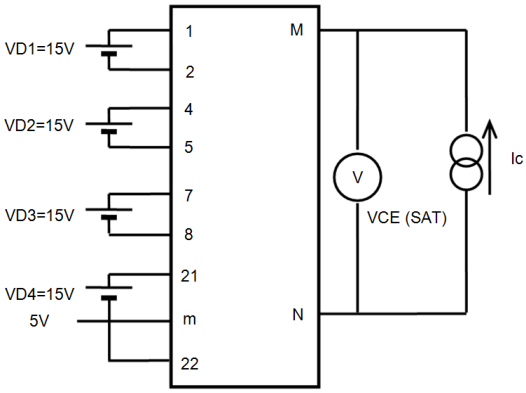


Figure 3. Test Circuit for V_{CE}(sat)

- V_F (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	10	10	10	2	5	8
N	2	5	8	12	12	12

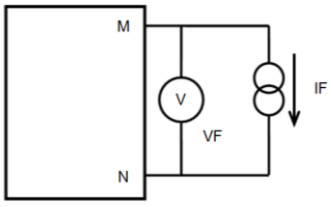


Figure 4. Test Circuit for V_F

- ID

	VD1	VD2	VD3	VD4
M	1	4	7	21
N	2	5	8	22

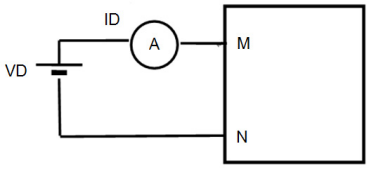
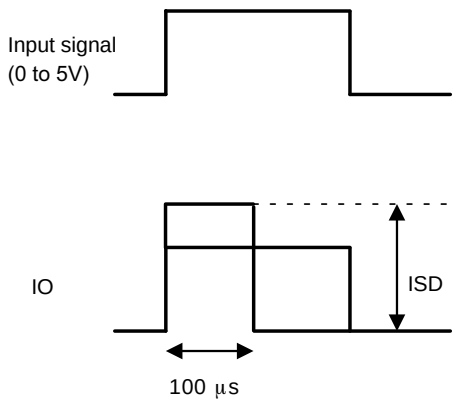


Figure 5. Test Circuit for ID

- ISD



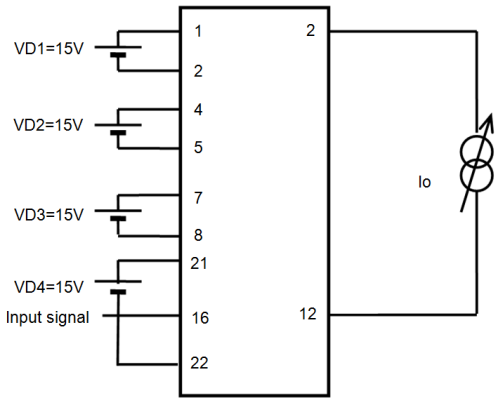
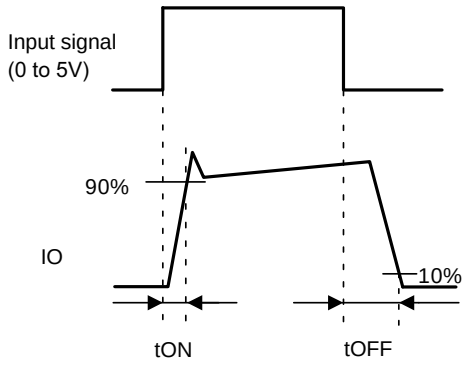


Figure 6. Test Circuit for ISD

- Switching time
  (The circuit is a representative example of the lower side U phase.)



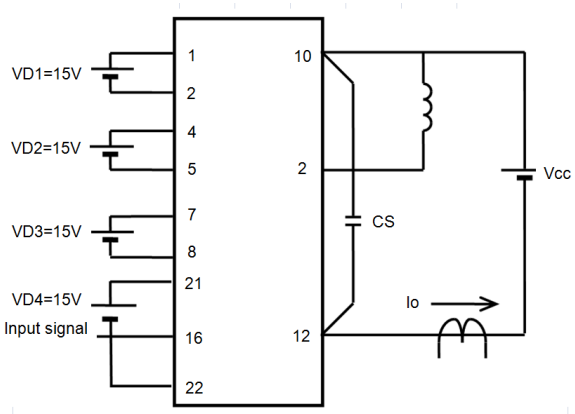
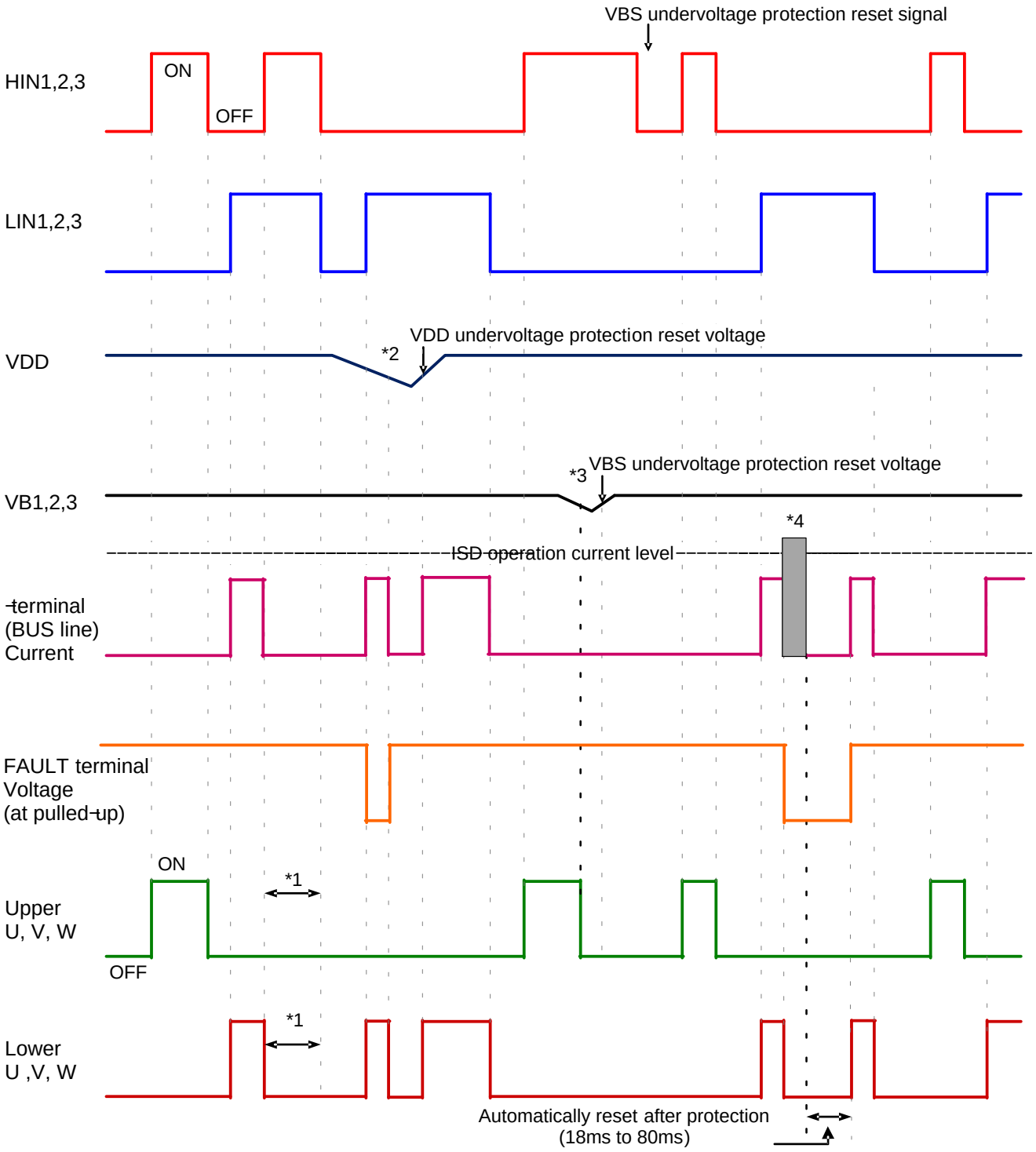


Figure 7. Switching Time Test Circuit

Logic Timing Chart



Notes:

*1: Diagram shows the prevention of shoot−through via control logic. More dead time to account for switching delay needs to be added externally.

*2: When V_{DD} decreases all gate output signals will go low and cut off all of 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.

*3: When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.

*4: In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 18 to 80 ms after the over current condition is removed.

Figure 8. Logic Timing Chart

Logic Level Table

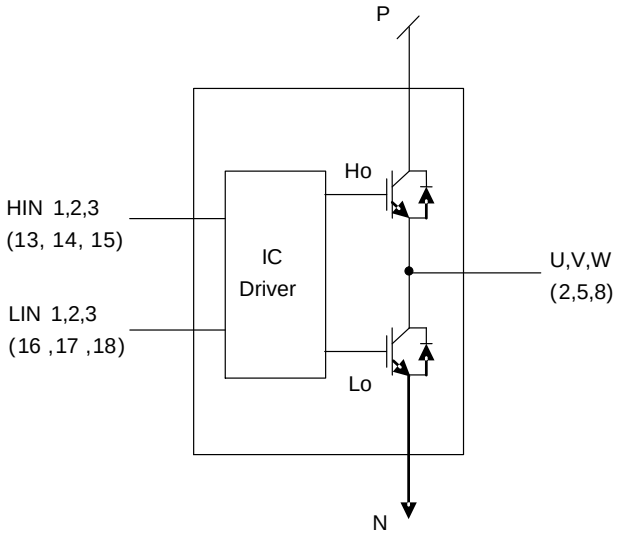


Figure 9.

LOGIC LEVEL TABLE

INPUT			OUTPUT			
HIN	LIN	OCP	Ho	Lo	U, V, W	FAULT
H	L	OFF	H	L	P	OFF
L	H	OFF	L	H	N	OFF
L	L	OFF	L	L	High Impedance	OFF
H	H	OFF	L	L	High Impedance	OFF
X	X	ON	L	L	High Impedance	ON

Sample Application Circuit

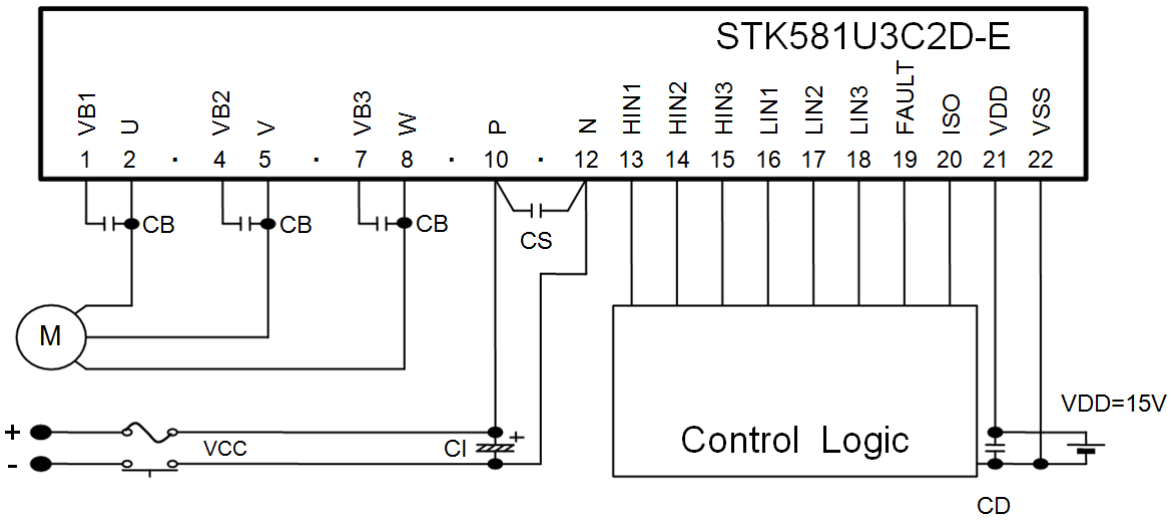


Figure 10. Sample Application Circuit

Usage Precautions

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47 μF (±20%), connect a resistor (about 20 Ω) in series between each 3−phase upper side power supply terminals (VB1, 2, 3) and each bootstrap capacitor.

   When not using the bootstrap circuit, each upper side pre−drive power supply requires an external independent power supply.
2. It is essential that wirning length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10 μF.
3. “ISO” (pin20) is terminal for current monitor. When the pull−down resistor is used, please select it more than 5.6 kΩ
4. “FAULT” (pin19) is open DRAIN output terminal (Active Low). Pull up resistor is recommended more than 5.6 kΩ.
5. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between V_{SS} terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.11, and Fig.12 below.
6. Pull down resistor of 33 kΩ is provided internally at the signal input terminals. An external resistor of 2.2 k to 3.3 kΩ should be added to reduce the influence of external wiring noise.
7. The over−current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.
8. When input pulse width is less than 1.0 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

THERMISTOR CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	99	100	101	kΩ
	R_{100}	Tc = 100°C	5.12	5.38	5.66	kΩ
B−Constant (25 to 50°C)	B		4165	4250	4335	K
Temperature Range			−40	−	+125	°C

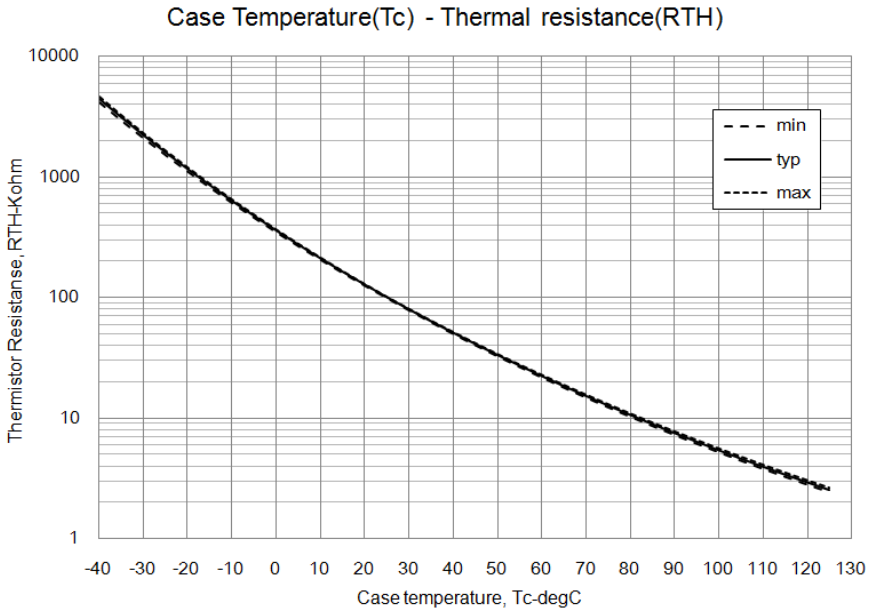


Figure 11. Thermistor Resistance versus Case Temperature

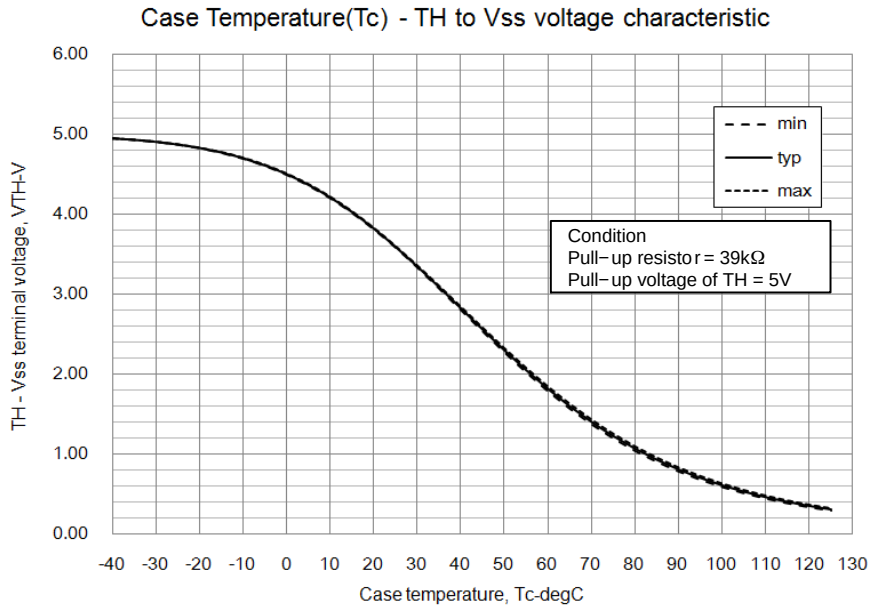


Figure 12. Thermistor Voltage versus Case Temperature

PWM Switching Frequency Characteristics

Maximum sinusoidal phase current as function of switching frequency (V_{BUS} = 300 V, Tc = 100°C)

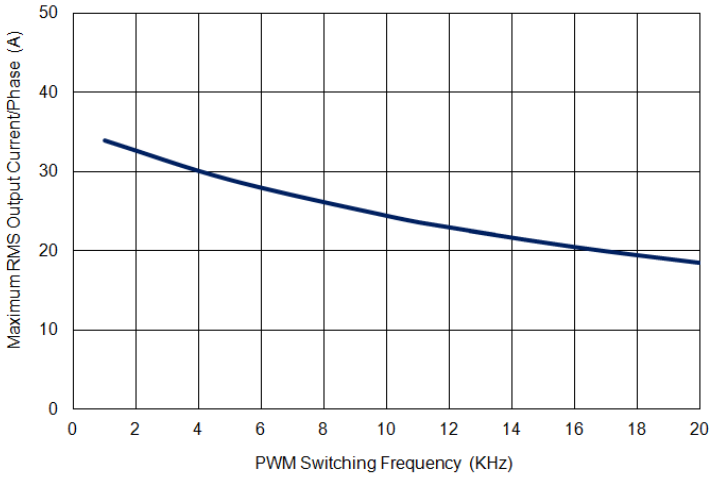


Figure 13. PWM Switching Frequency Characteristics

Switching Waveforms

IGBT Turn−on. Typical turn−on waveform @Tc = 100°C, V_{BUS} = 400 V

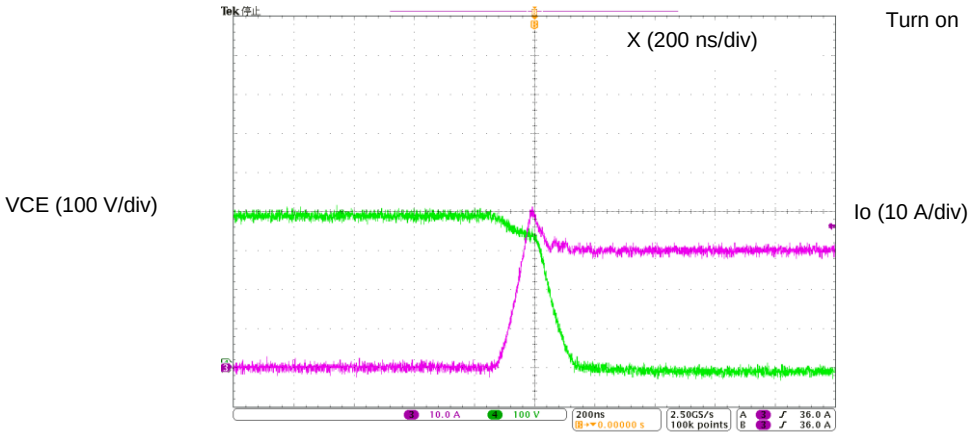


Figure 14.

IGBT Turn−off. Typical turn−off waveform @Tc = 100°C, V_{BUS} = 400 V

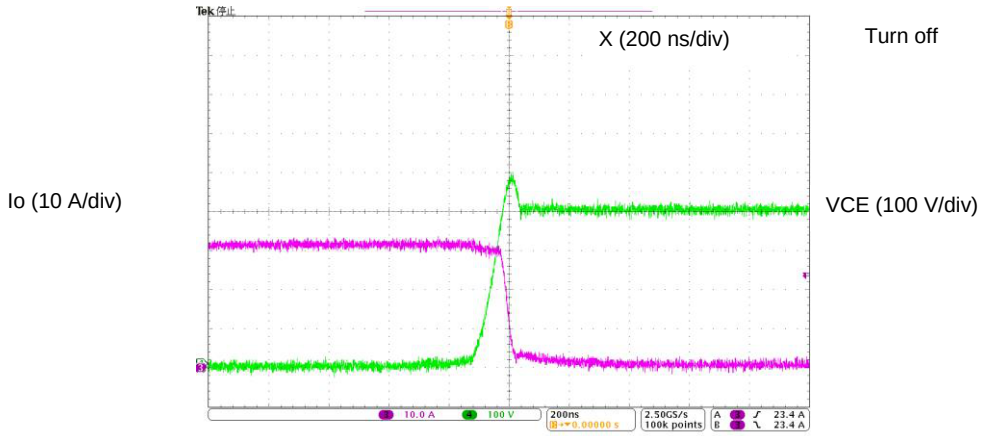


Figure 15.

CB Capacitor Value Calculation for Bootstrap Circuit

CALCULATE CONDITIONS TABLE

Item	Symbol	Value	Unit
Upper side power supply.	VBS	15	V
Total gate charge of output power IGBT at 15 V.	Qg	266	nC
Upper side power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDmax	400	μA
ON time required for CB voltage to fall from 15 V to UVLO	Tonmax	−	s

Capacitance Calculation Formula

CB must not be discharged below to the upper limit of the UVLO − the maximum allowable on−time (Tonmax) of the upper side is calculated as follows:

VBS * CB – Qg – IDmax * Tonmax = UVLO * CB

CB = (Qg + IDmax * Tonmax) / (VBS – UVLO)

The relationship between Tonmax and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production.

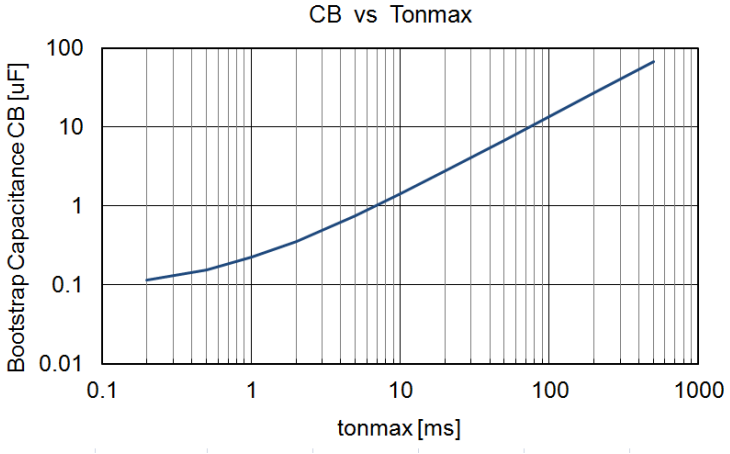


Figure 16. Tonmax−CB Characteristics

ORDERING INFORMATION

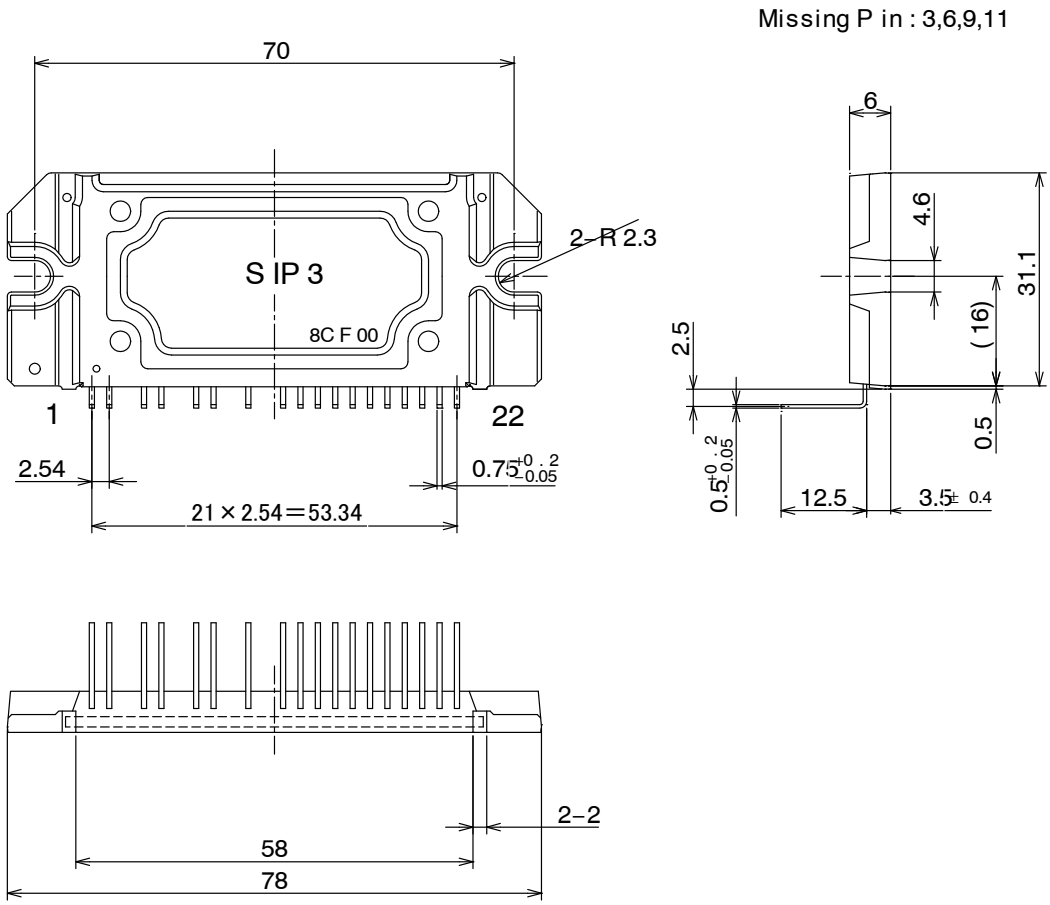
Device	Marking	Package	Shipping
STK581U3C2D−E	STK581U3C2D	SIP22 70x31.1 (Pb−Free)	7 Units / Tube

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SIP22 70x31.1
CASE 127BU
ISSUE O

DATE 30 APR 2012



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