Noninverting Buffer / CMOS Logic Level Shifter

with TTL-Compatible Inputs

The MC74VHC1GT50 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT50 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT50 to be used to interface high voltage to low voltage circuits. The output structures also provide protection when $V_{CC}\!=\!0$ V. These input and output structures help prevent device destruction caused by supply voltage - input/output voltage mismatch, battery backup, hot insertion, etc.

- Designed for 1.65 V to 5.5 V_{CC} Operation
- High Speed: $t_{PD} = 3.5 \text{ ns (Typ)}$ at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A \text{ (Max)}$ at $T_A = 25 \text{°C}$
- TTL-Compatible Inputs: $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.0 \text{ V}$, $V_{CC} = 5 \text{ V}$
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 104; Equivalent Gates = 26

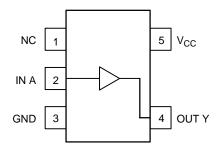


Figure 1. Pinout (Top View)

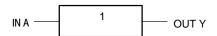


Figure 2. Logic Symbol



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MARKING DIAGRAMS

SC-88A / SOT-353/SC-70 DF SUFFIX CASE 419A



Pin 1 d = Date Code

TSOP-5/SOT-23/SC-59 DT SUFFIX CASE 483



Pin 1

d = Date Code

PIN ASSIGNMENT

1	NC
2	IN A
3	GND
4	OUT Y
5	V _{CC}

FUNCTION TABLE

A Input	Y Output
L	L
Н	Н

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS (Note 1)

Symbol	Characte	ristics	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	$V_{CC} = 0$ High or Low State	-0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current		-20	mA
lok	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I _{OUT}	DC Output Current, per Pin		+25	mA
Icc	DC Supply Current, V _{CC} and GND		+50	mA
P _D	Power dissipation in still air	SC-88A, TSOP-5	200	mW
θ_{JA}	Thermal resistance	SC- 88A, TSOP- 5	333	°C/W
TL	Lead temperature, 1 mm from case for 10	s	260	°C
TJ	Junction temperature under bias		+150	°C
T _{stg}	Storage temperature		-65 to +150	°C
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I _{Latch- Up}	Latch-Up Performance Above V	CC and Below GND at 125°C (Note 5)	±500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those
indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional
operation should be restricted to the Recommended Operating Conditions.

- 2. Tested to EIA/JESD22-A114-A
- 3. Tested to EIA/JESD22-A115-A
- 4. Tested to JESD22-C101-A
- 5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit	
V _{CC}	DC Supply Voltage	1.65	5.5	V	
V _{IN}	DC Input Voltage	0.0	5.5	V	
V _{OUT}	DC Output Voltage	$V_{CC} = 0$ High or Low State	0.0 0.0	5.5 V _{CC}	V
T _A	Operating Temperature Range		-55	+125	°C
t _r , t _f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0	100 20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

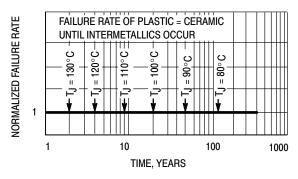


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	T,	= 25 °	С	T _A ≤	85°C	-55 ≤ T _A	≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Minimum		1.65 to 2.29	0.50 V _{CC}			0.50 V _{CC}		0.50 V _{CC}		V
	High-Level Input Voltage		2.3 to 2.99	0.45 V _{CC}			0.45 V _{CC}		0.45 V _{CC}		
	,		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		
V_{IL}	Maximum		1.65 to 2.29			0.10 V _{CC}		0.10 V _{CC}		0.10 V _{CC}	V
	Low-Level Input Voltage		2.3 to 2.99			0.15 V _{CC}		0.15 V _{CC}		0.15 V _{CC}	
			3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	
V _{OH}	Minimum	V _{IN} = V _{IH}	1.65 to 2.99	V _{CC} - 0.1			V _{CC} - 0.1		V _{CC} - 0.1		V
	High-Level Output Voltage	I _{OH} = -50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		
		$V_{IN} = V_{IH}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Maximum	$V_{IN} = V_{IL}$	1.65 to 2.99		0.0	0.1		0.1		0.1	V
	Low-Level Output Voltage	I _{OL} = 50 μA	3.0 4.5		0.0	0.1 0.1		0.1 0.1		0.1 0.1	
		$V_{IN} = V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I _{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5 \text{ V or GND}$	0 to 5.5			± 0.1		±1.0		±1.0	μА
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		20		40	μА
I _{CCT}	Quiescent Supply Current	Input: V _{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μА

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

			7	Γ _A = 25°	С	T _A ≤	85°C		≤ T _A ≤ 5°C	
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} ,	Maximum Propagation	$V_{CC} = 1.8 \pm 0.15 \text{ V C}_{L} = 15 \text{ pF}$			16.6		18.0		22.0	ns
t _{PHL}	L Delay, Input A to Y	$V_{CC} = 2.5 \pm 0.2 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$			13.3 19.5		14.5 22.0		17.5 25.5	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		4.5 6.3	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		3.5 4.3	6.7 7.7		7.5 8.5		8.5 9.5	
C _{IN}	Maximum Input Capacitance			5	10		10		10	pF

		Typical @ 25°C, V _{CC} = 5.0 V		
C_{PD}	Power Dissipation Capacitance (Note 6)	12	pF	

^{6.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

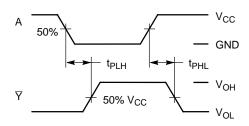
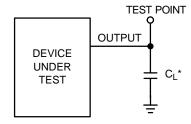


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

	Device Nomenclature							
Device Order Number	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix	Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
MC74VHC1GT50DFT1	МС	74	VHC1G	T50	DF	T1	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT50DFT2	МС	74	VHC1G	T50	DF	T2	SC-88A / SOT-353 / SC-70	178 mm (7") 3000 Unit
MC74VHC1GT50DTT1	МС	74	VHC1G	T50	DT	T1	TSOP-5 / SOT-23 / SC-59	178 mm (7") 3000 Unit

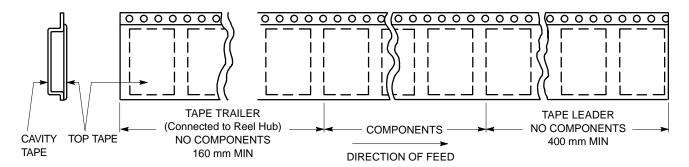
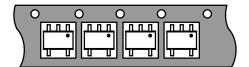
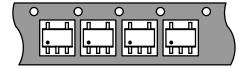


Figure 6. Tape Ends for Finished Goods

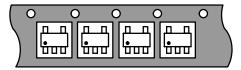


"T1" Pin One Toward Sprocket Hole (3k Reel)



"T2" Pin One Opposing Sprocket Hole (3k Reel)

Figure 7. SC-88A/SOT-353/SC-70-5 DFT1 and DFT2 Reel Configuration/Orientation



"T1" Pin One Opposing Sprocket Hole (3k Reel)

Figure 8. TSOP-5/SC59-5/SOT23-5 DTT1
Reel Configuration/Orientation

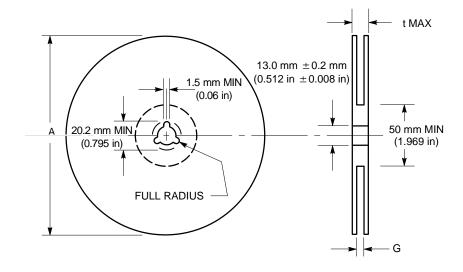


Figure 9. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

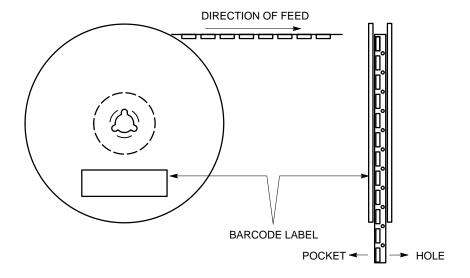
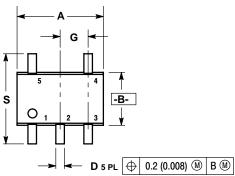


Figure 10. Reel Winding Direction

PACKAGE DIMENSIONS

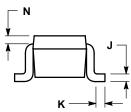
SC-88A / SOT-353 / SC-70 **DF SUFFIX**

5-LEAD PACKAGE CASE 419A-02 ISSUE F



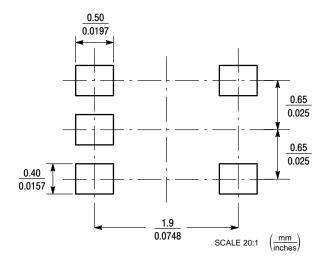
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- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.

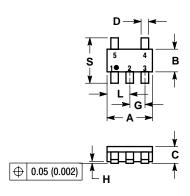
	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65	BSC
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20	REF
S	0.079	0.087	2.00	2.20

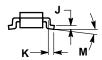


PACKAGE DIMENSIONS

TSOP-5 / SOT-23 / SC-59 DT SUFFIX

5-LEAD PACKAGE CASE 483-01 ISSUE B

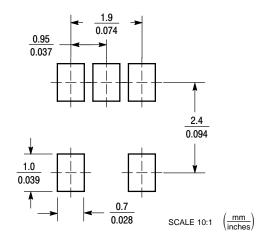




NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- . CONTROLLING DIMENSION: MILLIMETER.
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.1142	0.1220
В	1.30	1.70	0.0512	0.0669
С	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
Н	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181



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