

MC74AC109, MC74ACT109

Dual JK Positive Edge-Triggered Flip-Flop

The MC74AC109/74ACT109 consists of two high-speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to MC74AC74/74ACT74 data sheet) by connecting the J and $\bar{K}$ inputs together.

Asynchronous Inputs:

- LOW input to $\bar{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\bar{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\bar{C}_D$ and $\bar{S}_D$ makes both Q and $\bar{Q}$ HIGH

- Outputs Source/Sink 24 mA
- 'ACT109 Has TTL Compatible Inputs

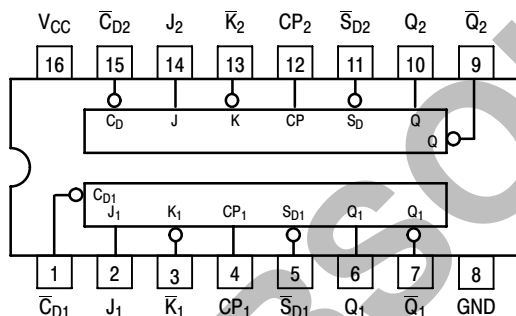


Figure 1. Pinout; 16-Lead Packages Conductors (Top View)

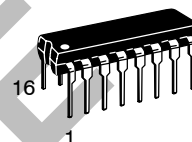
PIN ASSIGNMENT

PIN	FUNCTION
J ₁ , J ₂ , $\bar{K}_1$, $\bar{K}_2$	Data Inputs
CP ₁ , CP ₂	Clock Pulse Inputs
$\bar{C}_D1$, $\bar{C}_D2$	Direct Clear Inputs
$\bar{S}_D1$, $\bar{S}_D2$	Direct Set Inputs
Q ₁ , Q ₂ , $\bar{Q}_1$, $\bar{Q}_2$	Outputs

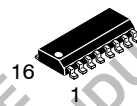


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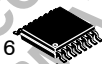
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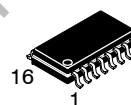
DIP-16
N SUFFIX
CASE 648



SO-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



EIAJ-16
M SUFFIX
CASE 966

ORDERING INFORMATION

Device	Package	Shipping
MC74AC109N	PDIP-16	25 Units/Rail
MC74ACT109N	PDIP-16	25 Units/Rail
MC74AC109D	SOIC-16	48 Units/Rail
MC74ACT109D	SOIC-16	48 Units/Rail
MC74AC109DR2	SOIC-16	2500 Tape & Reel
MC74ACT109DR2	SOIC-16	2500 Tape & Reel
MC74AC109DT	TSSOP-16	96 Units/Rail
MC74ACT109DT	TSSOP-16	96 Units/Rail
MC74AC109DTR2	TSSOP-16	2500 Tape & Reel
MC74ACT109DTR2	TSSOP-16	2500 Tape & Reel
MC74AC109M	EIAJ-16	50 Units/Rail
MC74ACT109M	EIAJ-16	50 Units/Rail
MC74AC109MEL	EIAJ-16	2000 Tape & Reel
MC74ACT109MEL	EIAJ-16	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

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TRUTH TABLE

Inputs					Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\downarrow$	L	L	L	H
H	H	$\downarrow$	H	L	Toggle	
H	H	$\downarrow$	L	H	Q_0	$\bar{Q}_0$
H	H	$\downarrow$	H	H	H	L
H	H	L	X	X	Q_0	$\bar{Q}_0$

H = HIGH Voltage Level

L = LOW Voltage Level

$\downarrow$ = LOW-to-HIGH Clock Transition

X = Immaterial

$Q_0(\bar{Q}_0)$ = Previous $Q_0(\bar{Q}_0)$ before
LOW-to-HIGH Transition of Clock

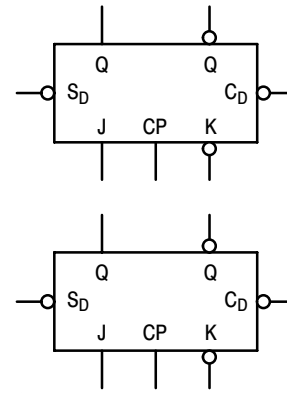
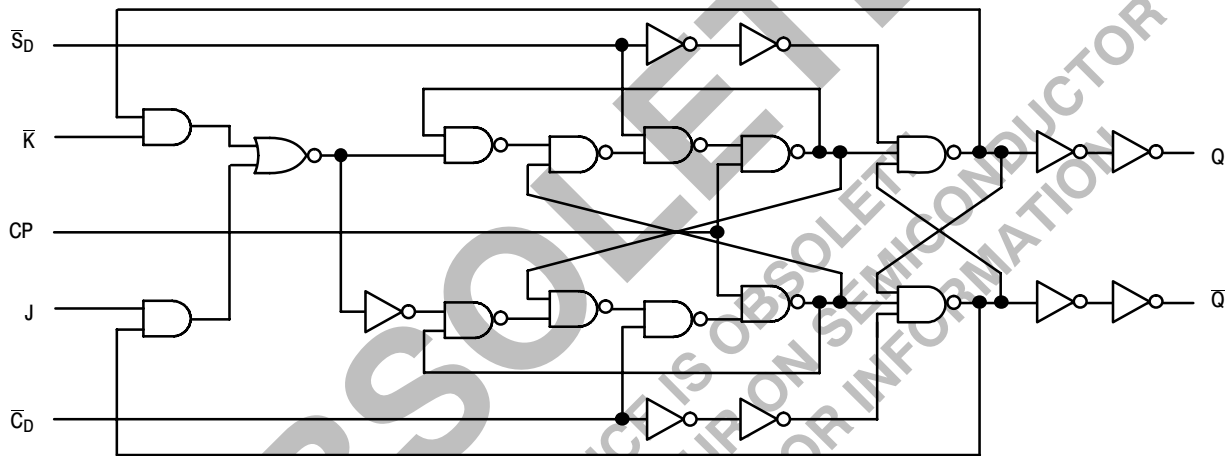


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram
(One Half Shown)

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0
		'ACT	4.5	5.0	5.5
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	–
		V _{CC} @ 4.5 V	–	40	–
		V _{CC} @ 5.5 V	–	25	–
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	–
		V _{CC} @ 5.5 V	–	8.0	–
T _J	Junction Temperature (PDIP)	–	–	140	°C
T _A	Operating Ambient Temperature Range	–40	25	85	°C
I _{OH}	Output Current – High	–	–	–24	mA
I _{OL}	Output Current – Low	–	–	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Unit	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	–	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
		4.5	–	3.86	3.76		
		5.5	–	4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	–	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5	–	0.36	0.44		
		5.5	–	0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	–	–	–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	125 150	– –	– –	100 125	– –	MHz	3–3
t _{PLH}	Propagation Delay CP _n to Q _n or $\overline{Q}_n$	3.3 5.0	4.0 2.5	– –	13.5 10.0	3.5 2.0	16.0 10.5	ns	3–6
t _{PHL}	Propagation Delay CP _n to Q _n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	– –	14.0 10.0	3.0 1.5	14.5 10.5	ns	3–6
t _{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	3.3 5.0	3.0 2.5	– –	12.0 9.0	2.5 2.0	13.0 10.0	ns	3–6
t _{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	– –	12.0 9.5	3.0 2.0	13.5 10.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Set-up Time, HIGH or LOW J _n or K _n to CP _n	3.3	–	6.5	7.5	ns	3–9
		5.0	–	4.5	5.0		
t _h	Hold Time, HIGH or LOW J _n or K _n to CP _n	3.3	–	0	0	ns	3–9
		5.0	–	0.5	0.5		
t _w	Pulse Width CP _n or C _{Dn} or S _{Dn}	3.3	–	4.0	4.5	ns	3–6
		5.0	–	3.5	3.5		
t _{rec}	Recovery Time C _{Dn} or S _{Dn} to CP	3.3	–	0	0	ns	3–9
		5.0	–	0	0		

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Unit	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = –50 μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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DC CHARACTERISTICS (continued)

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Unit	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
		4.5	–	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA
		5.5	–	0.36	0.44		I _{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	–	1.5	mA	V _I = V _{CC} – 2.1 V
I _{OLD}	†Minimum Dynamic	5.5	–	–	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}	Output Current	5.5	–	–	–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	145	–	–	125	–	MHz	3–3
t _{PLH}	Propagation Delay CP _n to Q _n or Q̄ _n	5.0	4.0	–	11.0	3.5	13.0	ns	3–6
t _{PHL}	Propagation Delay CP _n to Q _n or Q̄ _n	5.0	3.0	–	10.0	2.5	11.5	ns	3–6
t _{PLH}	Propagation Delay C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	5.0	2.5	–	9.5	2.0	10.5	ns	3–6
t _{PHL}	Propagation Delay C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	5.0	2.5	–	10.0	2.0	11.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Set-up Time, HIGH or LOW J _n or K _n to CP _n	5.0	–	2.0	2.5	ns	3–9
t _h	Hold Time, HIGH or LOW J _n or K _n to CP _n	5.0	–	2.0	2.0	ns	3–9
t _w	Pulse Width CP _n or C _{Dn} or S _{Dn}	5.0	–	5.0	6.0	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC109, MC74ACT109

AC OPERATING REQUIREMENTS (continued)

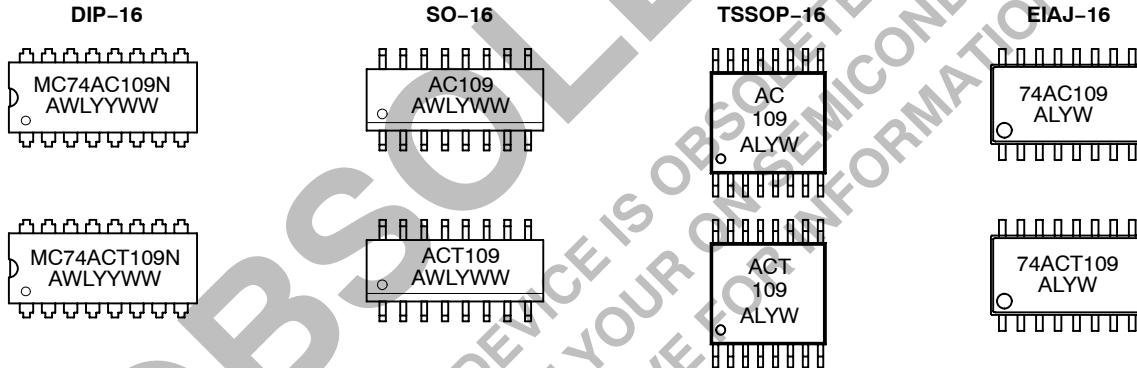
Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _{rec}	Recovery Time C _{Dn} or S _{Dn} to CP	5.0	–	0	0	ns	3–9

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	35	pF	V _{CC} = 5.0 V

MARKING DIAGRAMS



A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week

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PACKAGE DIMENSIONS

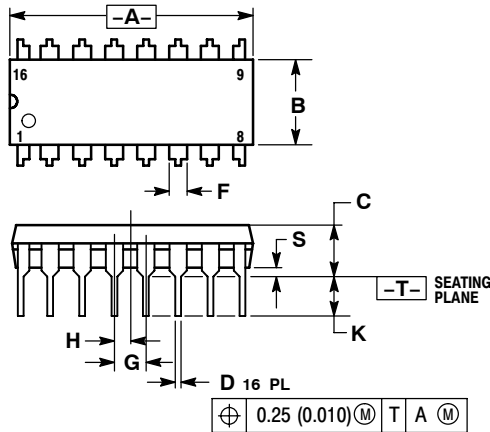
PDIP-16

N SUFFIX

16 PIN PLASTIC DIP PACKAGE

CASE 648-08

ISSUE R



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

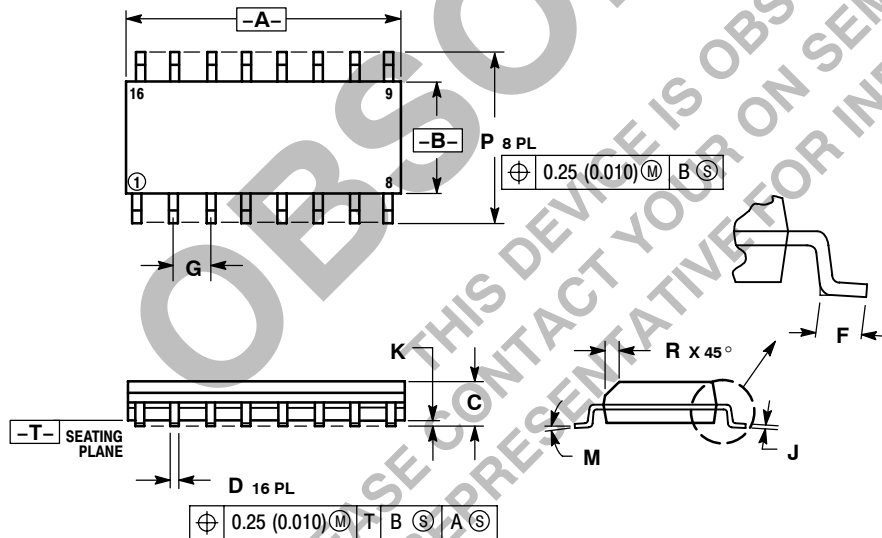
SO-16

D SUFFIX

16 PIN PLASTIC SOIC PACKAGE

CASE 751B-05

ISSUE J



NOTES:

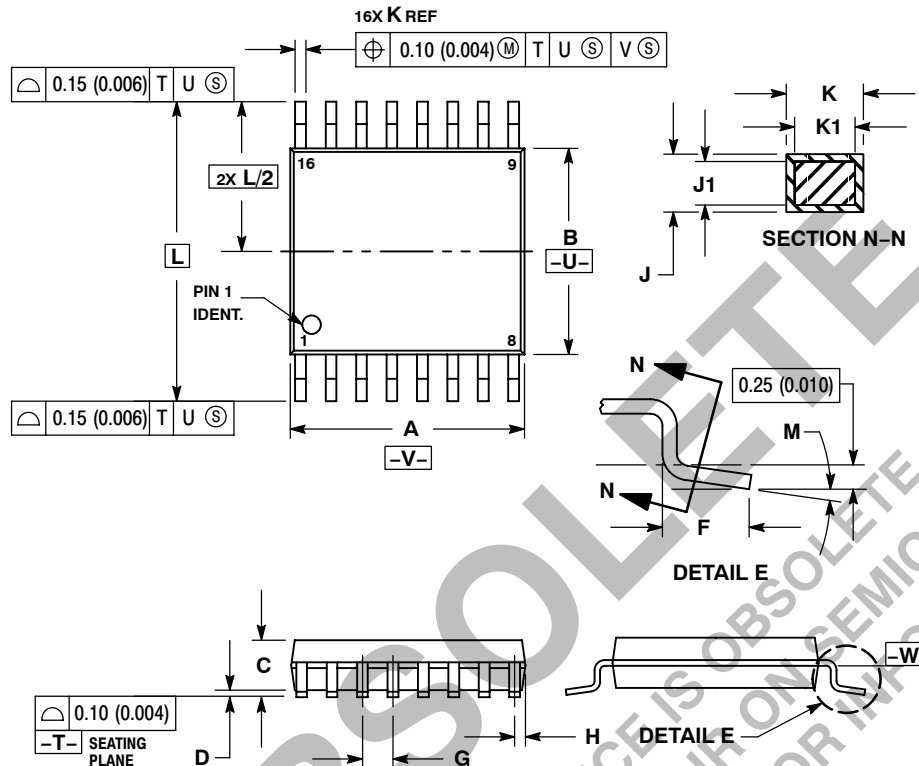
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MC74AC109, MC74ACT109

PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
 16 PIN PLASTIC TSSOP PACKAGE
 CASE948F-01
 ISSUE O

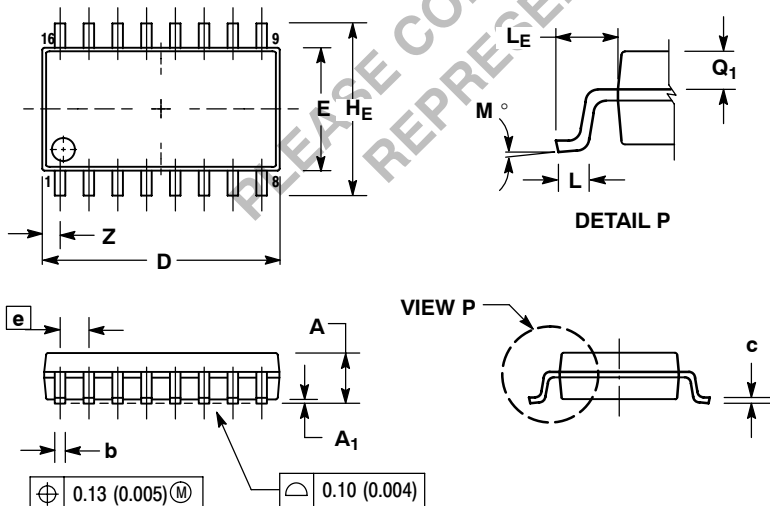


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

EIAJ-16
M SUFFIX
 16 PIN PLASTIC EIAJ PACKAGE
 CASE966-01
 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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