FAIRCHILD SEMICONDUCTOR®

September 2009

FXM2IC102
2-Bit I²C Bus Interface Voltage Translator / Repeater

Features

- Bi-Directional Interface between any Two Levels from 1.65V to 5.5V
- Auto-Direction Sensing, Direction Control not Needed
- Buffer Isolates Capacitance and Allows 400pF on Each Port
- Open-Drain Inputs/Outputs
- Schmitt Trigger Data Inputs
- Accommodates Standard-Mode and Fast-Mode I²C-bus Devices
- Fully Configurable: Inputs and Outputs Track V_{CC} Level
- Non-Preferential Power-up; Either V_{CC} May be Powered Up First
- Outputs Remain in 3-State until Active V_{CC} Level is Reached
- Power-Off High Impedance
- Active HIGH Output Enable Referenced to V_{CCA}
- 5V-Tolerant Output Enable
- Packaged in 8-Terminal Leadless MicroPak™ (1.6mm x 1.6mm)
- ESD Protection Exceeds:
  - 8kV HBM ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 15kV HBM I/O to GND ESD (per JESD22-A114 & Mil Std 883e 3015.7)

Description

The FXM2IC102 is a configurable dual-voltage-supply translator designed for bi-directional voltage translation over a wide range of input and output voltage levels.

The FXM2IC102 is intended for use as a voltage translator in applications using the I²C bus interface. Input and output voltage levels are compatible with I²C device specification voltage levels.

The device is designed so that the A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over voltage ranges: 1.8V, 2.5V, 3.3V, and 5.0V.

The device remains in 3-state until both V_{CC}s reach active levels, allowing either V_{CC} to be powered up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The two ports of the device have auto-direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Schmitt triggers are used on data inputs for signal noise suppression. Typically the inputs have 100 millivolts of hysteresis over the full V_{CC} range.

The FXM2IC102 typically consumes only 230nA during "no I²C data transactions" when V_{CCA} = 1.8V and V_{CCB} = 3.3V. *See Figure 4 and Figure 5 for more details.*

FXM2IC102 exhibits robust I²C repeater performance due to strong current sinking capability in > 400pf bus segments. *See Figure 6 and Figure 7 for details.*

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Eco Status	Package	Packing Method
FXM2IC102L8X	-40 to +85°C	XG	Green	8-Lead MicroPak, 1.6mm Wide	3000 Units on Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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Pin Configuration

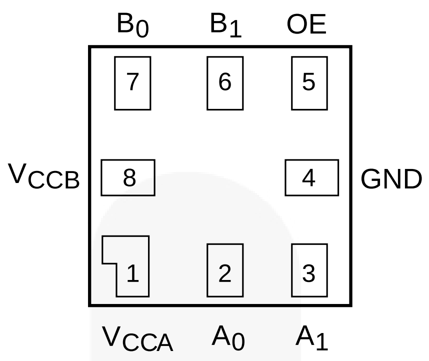

Figure 1. Pin Configuration (Top-Through View)

Pin Definitions

Pin #	Name	Description
1	V_{CCA}	A-Side Power Supply
2, 3	A_0, A_1	A-Side Inputs or 3-State Outputs
4	GND	Ground
5	OE	Output Enable Input
6, 7	B_1, B_0	B-Side Inputs or 3-State Outputs
8	V_{CCB}	B-Side Power Supply

Functional Diagram

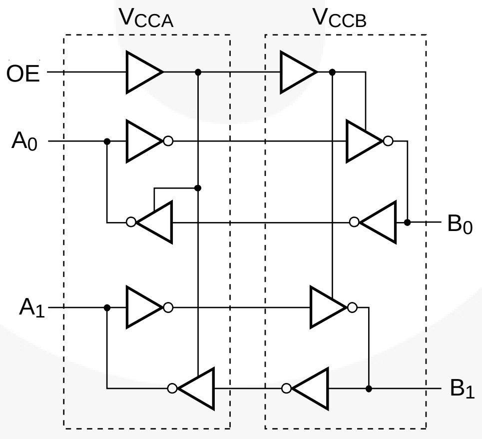

Figure 2. Functional Diagram

Truth Table

Control	Outputs
OE	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{CCA}, V_{CCB}	Supply Voltage		–0.5	7.0	V
V_{IN}	DC Input Voltage	A Port	–0.5	7.0	V
		B Port	–0.5	7.0	
		Control Input (OE)	–0.5	7.0	
V_O	Output Voltage[1]	A_n Outputs 3-State	–0.5	7.0	V
		B_n Outputs 3-State	–0.5	7.0	
		A_n Outputs Active	–0.5	V_{CCA} + 0.5V	
		B_n Outputs Active	–0.5	V_{CCB} + 0.5V	
I_{IK}	DC Input Diode Current	At V_{IN} < 0V		–50	mA
I_{OK}	DC Output Diode Current	At V_O < 0V		–50	mA
		At V_O > V_{CC}		+50	
I_{OH} / I_{OL}	DC Output Source/Sink Current		–50	+50	mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin			±100	mA
T_{STG}	Storage Temperature Range		–65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		8000	V
		Charged Device Model, JESD22-C101		2000	

Note:
1. I_O absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Units
V_{CCA}, V_{CCB}	Power Supply Operating		1.65	5.50	V
V_{IN}	Input Voltage	A Port	0	5.5	V
		B Port	0	5.5	
		Control Input (OE)	0	V_{CCA}	
$\Delta t / \Delta V$	Maximum Input Edge Rate	$V_{CCA/B}$ = 1.65V to 5.5V		200	ns/V
T_A	Free Air Operating Temperature		–40	+85	°C

Note:
2. All unused inputs and I/O pins must be held at V_{CCI} or GND. V_{CCI} is the V_{CC} associated with the input side.

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Power-Up/Power-Down Sequencing

FXM translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0V, outputs are in a high-impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Application Circuit

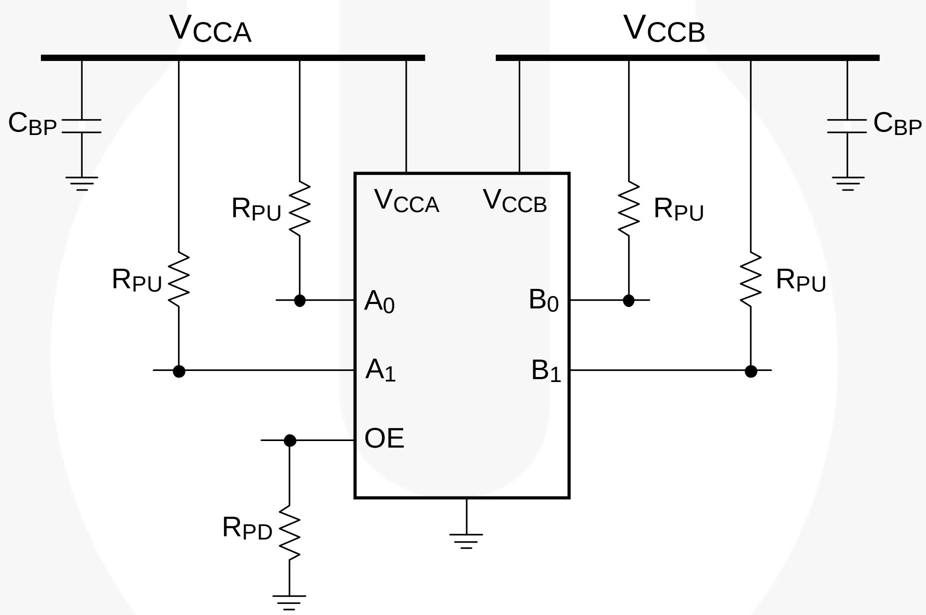

Figure 3. Application Circuit

Application Notes

The FXM2IC102 has open-drain outputs and requires pull-up resistors on the four data I/O pins, as shown in Figure 3. If a pair of data I/O pins (A_n/B_n) is not used, both pins should be tied to GND (or both to V_{CC}). In this case, pull-down or pull-up resistors are not required.

The recommended values for the pull-up resistors (R_{PU}) are 1kΩ minimum to 10kΩ maximum. The recommended value for the bypass capacitors (C_{BP}) is 0.1µF. The recommended value for the pull-down resistor (R_{PD}) on OE is 1kΩ or higher and may depend upon the current-sinking capability of the device driving the OE pin.

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Low I_{CC} During I^2C Idle

In a typical Mobile Internet Device (MID) application, I^2C data transactions are idle the vast majority of the time. Therefore, it is critical that the I^2C translator burns as little current as possible when no data transactions are passing across the I^2C bus. Figure 4 and Figure 5 plot the typical FXM2IC102 I_{CC} performance across the entire voltage translation range during no I^2C data transactions. In Figure 4, V_{CCB} = 5.5V and in Figure 5, V_{CCB} = 3.3V.

For example, to translate from 1.8V to 3.3V (Figure 5), with no I^2C data transactions present, the total I_{CC} of the FXM2IC102 is typically only 230nA. In effect, the FXM2IC102 virtually powers itself down when the I^2C bus is idle.

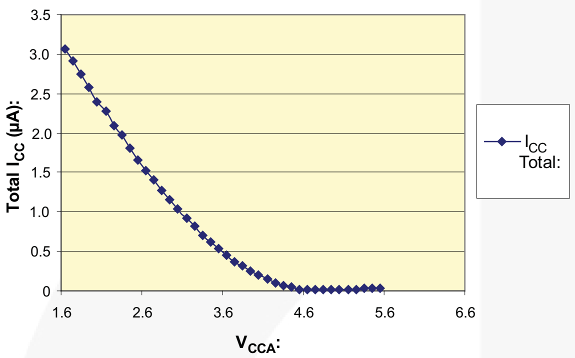

Figure 4. FXM2IC102 I_{CC} vs. V_{CCA} Sweep During no I^2C Data Transactions (V_{CCB} = 5.5V. T_A = +25°C)

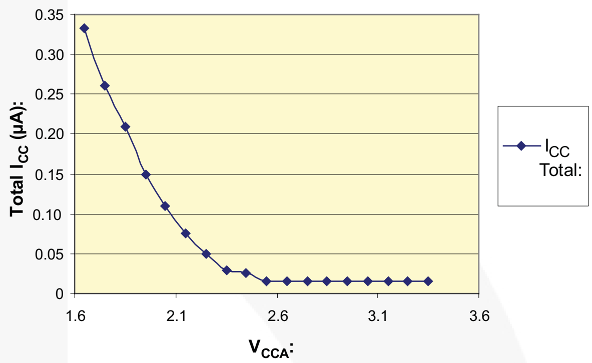

Figure 5. FXM2IC102 I_{CC} vs. V_{CCA} Sweep During no I^2C Data Transactions (V_{CCB} = 3.3V. T_A = +25°C)

Note:

3. Figure 4 depicts the typical I_{CC} of the FXM2IC102 when translating from 5.5V on the V_{CCB} supply to a range of 1.65V – 5.5V on the V_{CCA} supply.

Note:

4. Figure 5 depicts the typical I_{CC} of the FXM2IC102 when translating from 3.3V on the V_{CCB} supply to a range of 1.65V – 3.3V on the V_{CCA} supply.

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What Makes a Good I2C Repeater?

The I²C specification identifies the maximum number of devices allowed on an I²C segment as 400pf. Therefore, when an I²C segment exceeds 400pf, a repeater is required to split the segment into two, whereby each of the individual I²C segments does not exceed 400pf.

The question then arises, "What makes a good I²C repeater?" The question becomes complicated when considering the following factors:

- Current sinking capability of the outputs
- Output edge rates
- Distributed and lumped capacitances of the I²C segment
- Speed of the I²C bus: standard mode (100kbits/s), fast mode (400kbit/s), or fast-mode plus (1000kbit/s)
- Pull-up resistor sizing
- System signal delays, including device propagation delay and time of flight vs. meeting critical data setup/hold times
- Multiple master / slave topologies
- Clock stretching

It is possible to simplify this by focusing on the output current sinking capability relative to the bus impedance.

The DC electrical tables of the I²C specification, for fast mode, require a maximum V_{OL} of 0.4V while sinking 3mA of current when V_{DD} > 2V, and a maximum V_{OL} of 0.2 * V_{DD}, while sinking 3mA when V_{DD} < 2V. The minimum I_{OL} is 3mA for a V_{OL} of 0.4V and 6mA for a V_{OL} of 0.6V.

In short, the more a repeater can sink current while maintaining the maximum V_{OL}, the more capacitance it can drive at a given data rate. The I²C specifically benchmarks this by stating: "to drive a full bus load at 400kHz, 6mA I_{OL} is required at 0.6V V_{OL}. Parts not meeting this specification can still function, but not at 400kHz and 400pF".

As shown in Figure 6, the FXM2IC102 can typically sink 11mA – 13mA, depending on temperature, while maintaining a V_{OL} of 0.33V when V_{DD} is only 1.65V. This says the FXM2IC102 delivers conservatively twice the current sinking capability for a 400pF, 1.65V segment running at 400kHz.

If V_{DD} = 1.95V, (Figure 7) the FXM2IC102 can sink 18mA – 21mA, depending on temperature, while maintaining a V_{OL} of 0.39V. This says the FXM2IC102 delivers conservatively 3 times the current sinking capability for a 400pF, 1.95V segment running at 400kHz.

If V_{DD} = 3.0V, the FXM2IC102 can sink 25mA – 30mA, depending on temperature, while maintaining a V_{OL} of 0.4V. This says the FXM2IC102 delivers conservatively 4x the current sinking capability for a 400pF, 3.0V segment running at 400kHz.

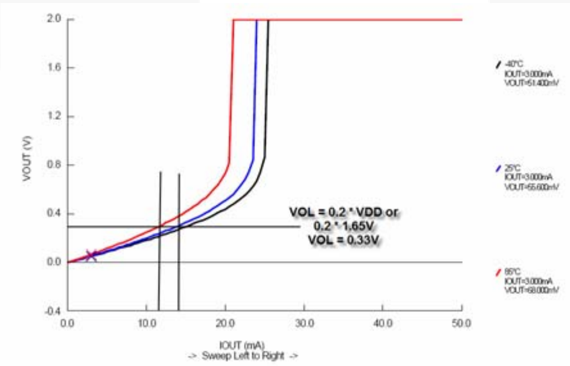

Figure 6. V_{OL} vs. I_{OL} (V_{DD} = 1.65V)

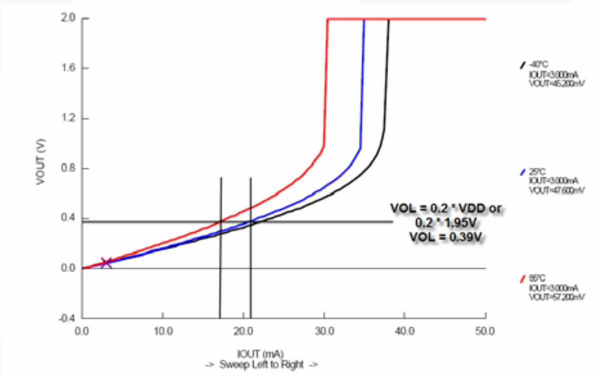

Figure 7. V_{OL} vs. I_{OL} (V_{DD} = 1.95V)

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DC Electrical Characteristics

T_A = –40°C to +85°C.

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min.	Max.	Units
V_{IHA}	High Level Input Voltage A	Data Inputs A_n	1.65–5.50	1.65–5.50	0.7 x V_{CCA}		V
		Control Input OE	1.65–5.50	1.65–5.50	0.9 x V_{CCA}		
V_{IHB}	High Level Input Voltage B	Data Inputs B_n	1.65–5.50	1.65–5.50	0.7 x V_{CCB}		V
V_{ILA}	Low Level Input Voltage A	Data Inputs A_n	1.65–5.50	1.65–5.50		0.3 x V_{CCA}	V
		Control Input OE	1.65–5.50	1.65–5.50		0.1 x V_{CCA}	
V_{ILB}	Low Level Input Voltage B	Data Inputs B_n	1.65–5.50	1.65–5.50		0.3 x V_{CCB}	V
V_{OLA}	Low Level Output Voltage A[5]	A Port, I_{OL} = 3mA	1.65–2.30	1.65–5.50		0.1 x V_{CCA}	V
		A Port, I_{OL} = 6mA	3.00–5.50	1.65–5.50		0.2	
V_{OLB}	Low Level Output Voltage B[5]	B Port, I_{OL} = 3mA	1.65–5.50	1.65–2.30		0.1 x V_{CCB}	V
		B Port, I_{OL} = 6mA	1.65–5.50	3.00–5.50		0.2	
I_L	Input Leakage Current	Control Input OE, V_{IN} = V_{CCA} or GND	1.65–5.50	1.65–5.50		±1.0	µA
I_{OFF}	Power Off Leakage Current	A_n: V_{IN} or V_O = 0V to 5.5V	0	5.50		±2.0	µA
		B_n: V_{IN} or V_O = 0V to 5.5V	5.50	0		±2.0	
I_{OZ}	3-State Output Leakage[6]	A_n, B_n: V_O = 0V to 5.5V, OE = V_{IL}	5.50	5.50		±2.0	µA
		A_n: V_O = 0V to 5.5V, OE = Don't Care	5.50	0		±2.0	
		B_n: V_O = 0V to 5.5V, OE = Don't Care	0	5.50		±2.0	
$I_{CCA/B}$	Quiescent Supply Current[7,8]	V_{IN} = V_{CCI} or GND, I_O = 0	1.65–5.50	1.65–5.50		5.0	µA
I_{CCZ}	Quiescent Supply Current[7]	V_{IN} = V_{CCI} or GND, I_O = 0, OE = V_{IL}	1.65–5.50	1.65–5.50		5.0	µA
I_{CCA}	Quiescent Supply Current[6]	V_{IN} = 5.5V or GND, I_O = 0, OE = Don't Care, B_n to A_n	0	1.65–5.50		–2.0	µA
			1.65–5.50	0		2.0	
I_{CCB}	Quiescent Supply Current[6]	V_{IN} = 5.5V or GND, I_O = 0, OE = Don't Care, A_n to B_n	1.65–5.50	0		–2.0	µA
			0	1.65–5.50		2.0	

Notes:
5. This is the output voltage for static conditions. Dynamic drive specifications are given in the Dynamic Output Electrical Characteristics table.
6. "Don't Care" indicates any valid logic level.
7. V_{CCI} is the V_{CC} associated with the input side.
8. Reflects current per supply, V_{CCA} or V_{CCB}.

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Dynamic Output Electrical Characteristics

Output rise / fall time and dynamic output current[9]. Output load: C_L = 50pF, R_L = 1kΩ. T_A = -40°C to +85°C.

Symbol	Parameter	V_{CCO}:[10]								Units
		4.5 to 5.5V		3.0 to 3.6V		2.3 to 2.7V		1.65 to 1.95V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
t_{rise}	Output Rise Time, A Port, B Port[11]		4		5		6		8	ns
t_{fall}	Output Fall Time, A Port, B Port[12]		4		5		6		8	ns
I_{OHD}	Dynamic Output Current HIGH[11]	-45		-24		-15		-8		mA
I_{OLD}	Dynamic Output Current LOW[12]	+45		+24		+15		+8		mA

Notes:
9. Dynamic output characteristics are guaranteed, but not tested.
10. V_{CCO} is the V_{CC} associated with the output side.
11. *See Figure 12*.
12. *See Figure 13*.

Maximum Data Rate[13]

Output Load: C_L = 50pF, R_L = 1kΩ. T_A = -40°C to +85°C.

V_{CCA}	V_{CCB}:				Units
	4.5 to 5.5V	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V	
	Min.	Min.	Min.	Min.	
4.5V to 5.5V	40	35	30	20	MHz
3.0V to 3.6V	35	35	30	20	MHz
2.3V to 2.7V	30	30	25	20	MHz
1.65V to 1.95V	20	20	20	20	MHz

Notes:
13. Maximum data rate is guaranteed, but not tested.

Capacitance

T_A = +25°C.

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance Control Pin (OE)	V_{CCA} = V_{CCB} = GND	4	pF
$C_{I/O}$	Input/Output Capacitance, A_n, B_n	V_{CCA} = V_{CCB} = 5.0V, OE = V_{CCA}	6	pF
C_{pd}	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 5.0V, V_{IN} = 0V or V_{CC}, f = 10MHz	40	pF

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AC Characteristics

Output Load: C_L = 50pF, R_L = 1kΩ. T_A = -40°C to +85°C.

Symbol	Parameter	V_{CCB}:								Units
		4.5 to 5.5V		3.0 to 3.6V		2.3 to 2.7V		1.65 to 1.95V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{CCA} = 4.5 to 5.5V										
t_{PLH}	A to B	1.0	4.5	1.5	5.5	2.0	7.0	3.0	11.5	ns
	B to A	1.0	4.5	1.5	5.5	1.5	6.5	2.5	9.5	
t_{PHL}	A to B	2.0	6.0	2.5	6.5	3.0	8.0	4.0	12.5	ns
	B to A	2.0	6.0	2.5	7.0	3.0	8.0	3.5	12.0	
t_{PZL}	OE to A		9.5		10.0		11.5		18.0	ns
	OE to B		9.0		11.0		13.5		22.0	
t_{PLZ}	OE to A		26.5		26.5		26.5		26.5	ns
	OE to B		26.0		26.5		20.5		15.5	
t_{skew}	A Port, B Port(14)		0.5		0.5		0.5		0.5	ns
V_{CCA} = 3.0 to 3.6V										
t_{PLH}	A to B	1.5	5.5	1.5	6.5	2.0	8.0	3.0	12.0	ns
	B to A	1.5	5.5	1.5	6.5	2.0	7.5	2.5	10.5	
t_{PHL}	A to B	2.5	7.0	2.5	7.5	3.0	9.0	4.0	13.0	ns
	B to A	2.5	6.5	2.5	7.5	3.0	9.5	4.0	13.0	
t_{PZL}	OE to A		12.5		13.0		15.5		21.0	ns
	OE to B		10.0		12.5		14.5		22.5	
t_{PLZ}	OE to A		27.5		28.0		28.0		28.0	ns
	OE to B		27.5		28.0		28.5		22.5	
t_{skew}	A Port, B Port(14)		0.5		0.5		0.5		0.5	ns
V_{CCA} = 2.3 to 2.7V										
t_{PLH}	A to B	1.5	6.5	2.0	7.5	2.5	8.5	3.5	12.5	ns
	B to A	2.0	7.5	2.0	8.0	2.5	8.5	3.0	11.5	
t_{PHL}	A to B	3.0	8.5	3.0	9.5	3.0	10.0	4.0	13.5	ns
	B to A	3.0	8.0	3.0	9.0	3.0	10.0	4.5	14.0	
t_{PZL}	OE to A		16.0		16.5		18.0		23.5	ns
	OE to B		11.0		14.0		15.5		23.5	
t_{PLZ}	OE to A		29.0		29.0		29.5		29.5	ns
	OE to B		29.0		29.0		29.5		29.5	
t_{skew}	A Port, B Port(14)		0.5		0.5		0.5		0.5	ns
V_{CCA} = 1.65 to 1.95V										
t_{PLH}	A to B	2.5	9.5	2.5	10.5	3.0	11.5	4.0	15.0	ns
	B to A	3.0	11.5	3.0	12.0	3.5	12.5	4.0	15.0	
t_{PHL}	A to B	3.5	11.5	4.0	12.5	4.5	14.0	5.0	15.5	ns
	B to A	4.0	12.5	4.0	13.0	4.0	13.5	5.0	15.5	
t_{PZL}	OE to A		27.0		27.0		27.0		30.0	ns
	OE to B		18.0		19.5		22.5		29.0	
t_{PLZ}	OE to A		34.0		34.0		34.5		35.0	ns
	OE to B		31.5		32.5		33.5		36.5	
t_{skew}	A Port, B Port(14)		0.5		0.5		0.5		0.5	ns

Note:

14. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) *(see Figure 15)*. Skew is guaranteed, but not tested.

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Applications Test Circuit

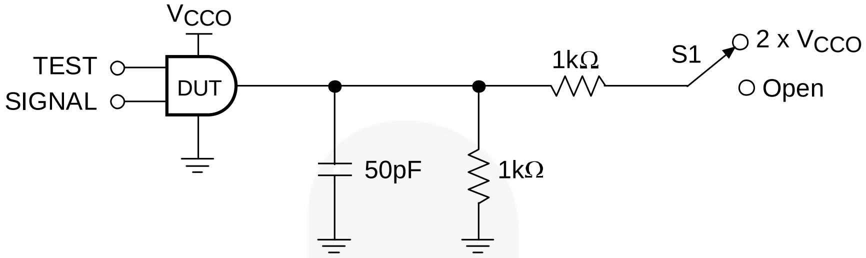

Figure 8. AC Test Circuit

Table 1. Propagation Delay Table

Test	Input Signal	Output Enable Control	S1 Position
t_{PLH}, t_{PHL}	Data Pulses	V_{CCA}	Open
t_{PZL} (OE to A_n, B_n)	0V	LOW to HIGH Switch	2 x V_{CCO}
t_{PLZ} (OE to A_n, B_n)	0V	HIGH to LOW Switch	2 x V_{CCO}

Table 2. AC Load Table

V_{CCO}	C_L	R_L
1.8 ±0.15V	50pF	1kΩ
2.5 ±0.2V	50pF	1kΩ
3.3 ±0.3V	50pF	1kΩ
5.0 ±0.5V	50pF	1kΩ

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Timing Diagrams

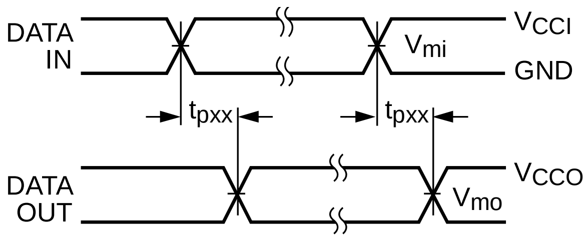


Figure 9. Waveform for Inverting and Non-Inverting Functions[15]

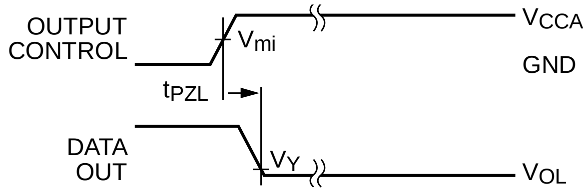


Figure 10. 3-STATE Output Low Enable Time[15]

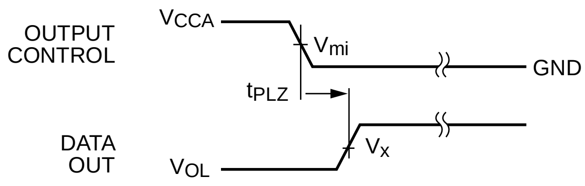
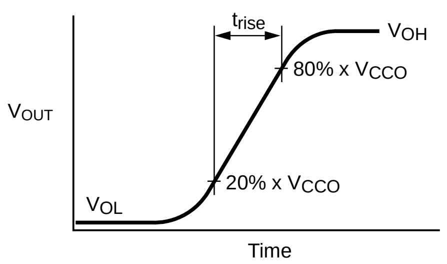


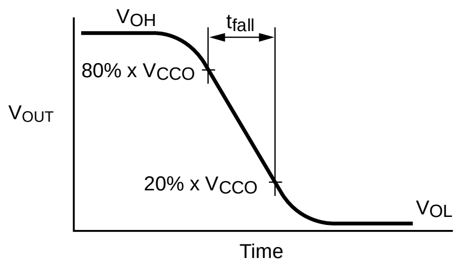
Figure 11. 3-STATE Output High Enable Time[15]

Symbol	V_{CC}
V_{mi}[16]	V_{CCI} / 2
V_{mo}	V_{CCO} / 2
V_X	0.5 x V_{CCO}
V_Y	0.1 x V_{CCO}



$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CCO}}{t_{RISE}}$$

Figure 12. Active Output Rise Time and Dynamic Output Current High



$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CCO}}{t_{FALL}}$$

Figure 13. Active Output Fall Time and Dynamic Output Current Low

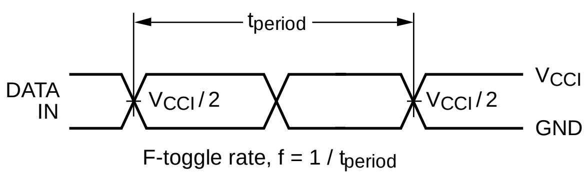
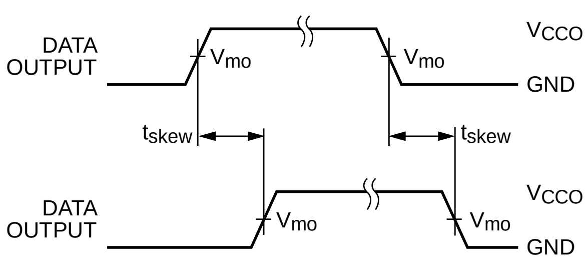


Figure 14. Maximum Data Rate (or F-Toggle) in MHz



$t_{skew} = (t_{pHLmax} - t_{pHLmin})$ or $(t_{pLHmax} - t_{pLHmin})$

Figure 15. Output Skew Time

Notes:

15. Input $t_R = t_F$ = 2.0ns, 10% to 90% at V_{IN} = 1.65V to 1.95V;
    Input $t_R = t_F$ = 2.0ns, 10% to 90% at V_{IN} = 2.3 to 2.7V;
    Input $t_R = t_F$ = 2.5ns, 10% to 90%, at V_{IN} = 3.0V to 3.6V only;
    Input $t_R = t_F$ = 2.5ns, 10% to 90%, at V_{IN} = 4.5V to 5.5 only.
16. $V_{CCI} = V_{CCA}$ for control pin OE or $V_{mi} = (V_{CCA} / 2)$.

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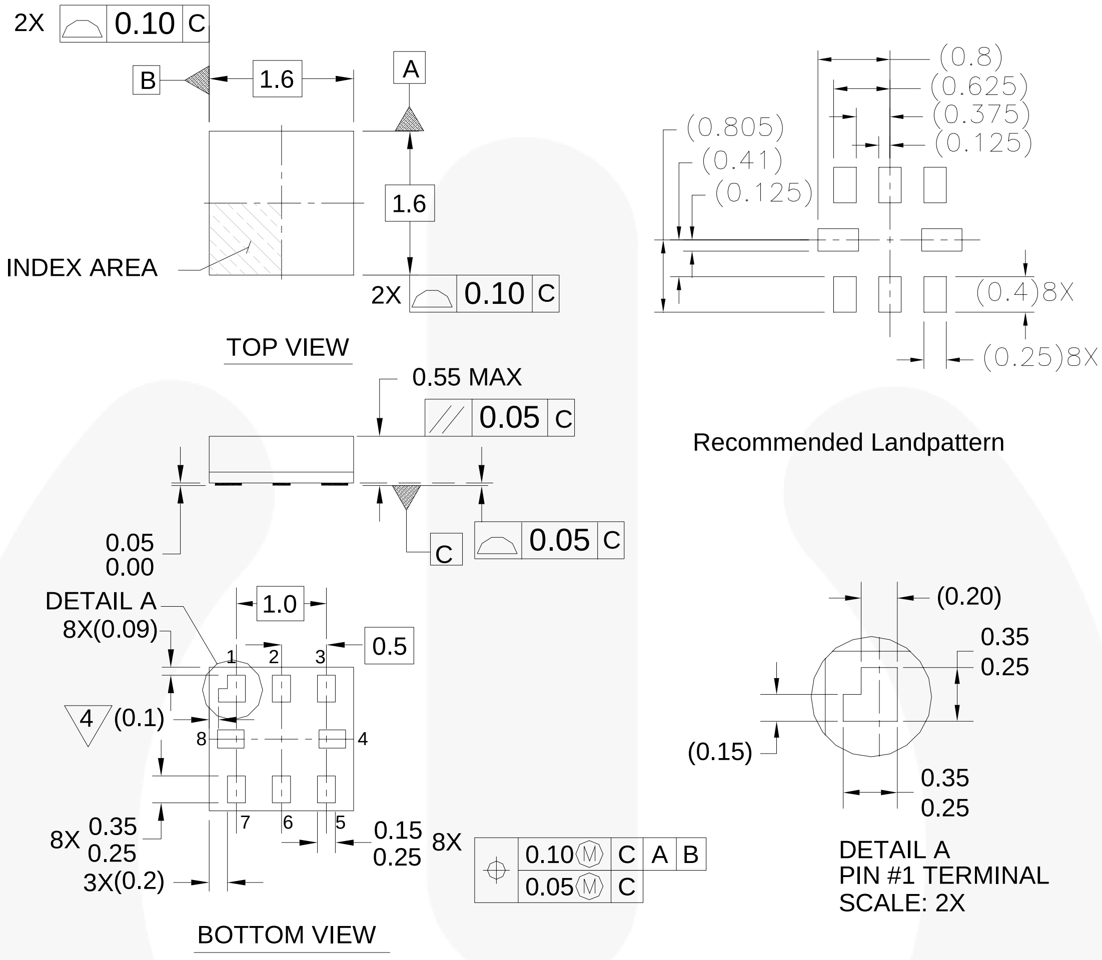
Physical Dimensions



Notes:
1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 16. 8-Lead MicroPak™, 1.6mm Wide

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Tape & Reel Format for MicroPak™

Always visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

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