

# MOSFET – P-Channel, QFET®

**-200 V, -11.5 A, 470 mΩ**

## FQB12P20

### General Description

These P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

### Features

- -11.5 A, -200 V,  $R_{DS(on)} = 0.47 \Omega @ V_{GS} = -10 V$
- Low Gate Charge (Typical 31 nC)
- Low  $C_{rss}$  (typical 30 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	FQB12P20	Unit
$V_{DSS}$	Drain-Source Voltage	-200	V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ C$ ) – Continuous ( $T_C = 100^\circ C$ )	-11.5	A
		-7.27	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	-46	A
$V_{GSS}$	Gate-Source Voltage	+30	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	810	mJ
$I_{AR}$	Avalanche Current (Note 1)	-11.5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	12	mJ
$dv/dt$	Peak Diode Recovery dv/dt (Note 3)	-5.5	V/ns
	Power Dissipation ( $T_A = 25^\circ C$ ) * Power Dissipation ( $T_C = 25^\circ C$ ) – Derate above $25^\circ C$	3.13	W
		120	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

\*When mounted on the minimum pad size recommended (PCB Mount)

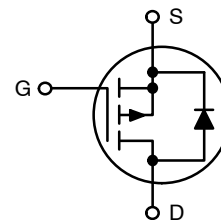
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 9.2 mH$ ,  $I_{AS} = -11.5 A$ ,  $V_{DD} = -50 V$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ C$
3.  $I_{SD} \leq -11.5 A$ ,  $di/dt \leq 300 A/\mu s$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ C$



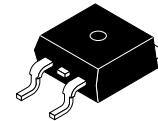
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$V_{DSS}$	$R_{DS(ON)} MAX$	$I_D MAX$
-200 V	$0.47 \Omega @ -10 V$	-11.5 A

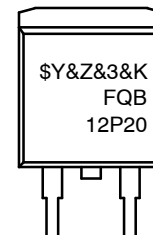


**P-CHANNEL MOSFET**



**D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)  
CASE 418AJ**

### MARKING DIAGRAM



FQB12P20 = Specific Device Code  
\$Y = ON Semiconductor Logo  
&Z = Assembly Plant Code  
&3 = Digit Date Code  
&K = Lot Run Traceability Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FQB12P20

## THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	–	1.04	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	–	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	–	62.5	°C/W

\*When mounted on the minimum pad size recommended (PCB Mount)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-200	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	–	–	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	–	–	-1	$\mu\text{A}$
		$V_{DS} = -160\text{ V}, T_C = 125^\circ\text{C}$	–	–	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-3.0	–	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -5.75\text{ A}$	–	0.36	0.47	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -5.75\text{ A}$ (Note 4)	–	6.4	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	920	1200	pF
$C_{oss}$	Output Capacitance		–	190	250	pF
$C_{rss}$	Reverse Transfer Capacitance		–	30	40	pF

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -100\text{ V}, I_D = -11.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	–	20	50	ns
$t_r$	Turn-On Rise Time		–	195	400	ns
$t_{d(off)}$	Turn-Off Delay Time		–	40	90	ns
$t_f$	Turn-Off Fall Time		–	60	130	ns
$Q_g$	Total Gate Charge	$V_{DS} = -160\text{ V}, I_D = -11.5\text{ A},$ $V_{GS} = -10\text{ V}$ (Note 4, 5)	–	31	40	nC
$Q_{gs}$	Gate-Source Charge		–	8.1	–	nC
$Q_{gd}$	Gate-Drain Charge		–	16	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current		–	–	–11.5	A
I <sub>SM</sub>	Maximum Pulsed Drain–Source Diode Forward Current		–	–	–46	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = –11.5 A	–	–	–5.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = –11.5 A, dI <sub>F</sub> / dt = 100 A/μs (Note 4)	–	180	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	1.44	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width  $\leq 300\text{ }\mu\text{s}$ , Duty cycle  $\leq 2\%$

5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

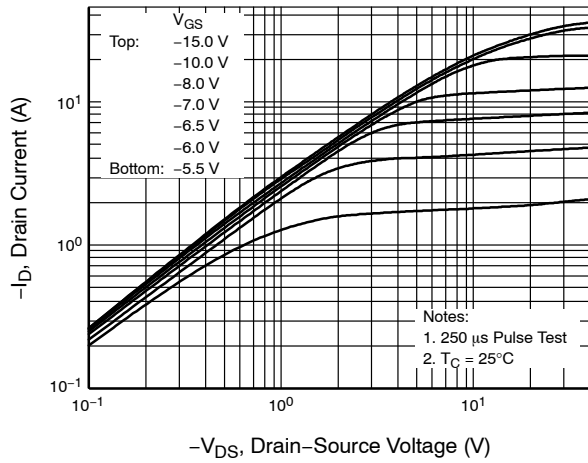


Figure 1. On Characteristics

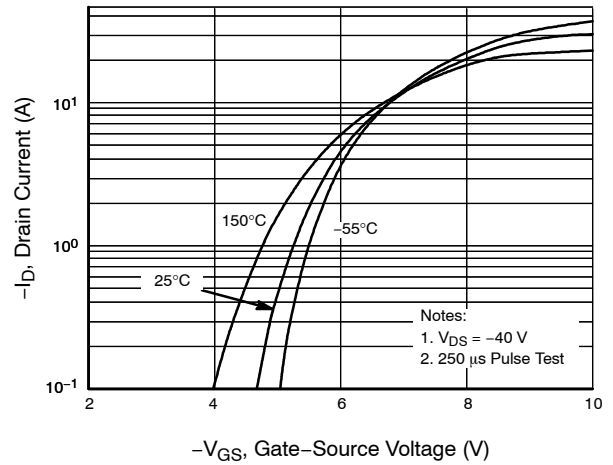


Figure 2. Transfer Characteristics

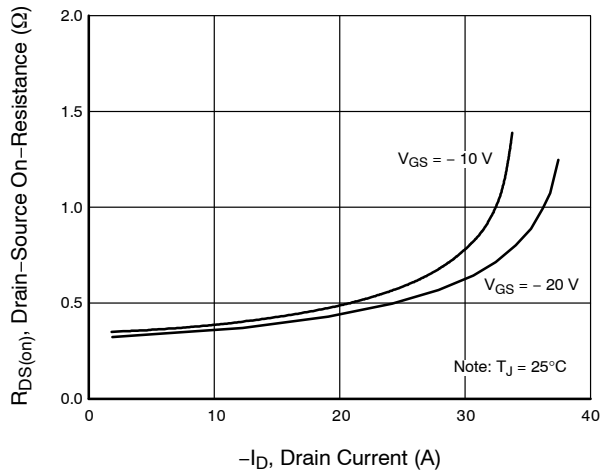


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

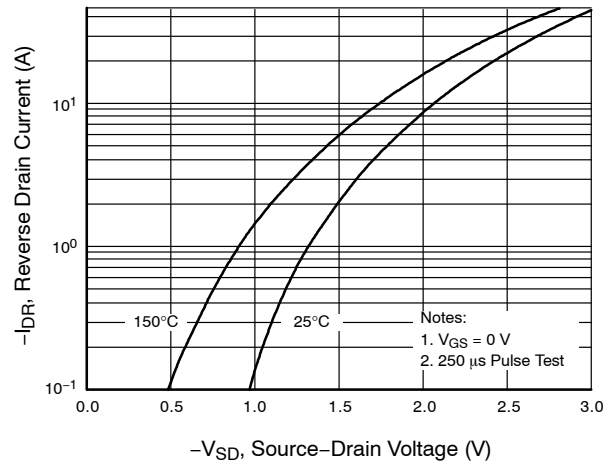


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

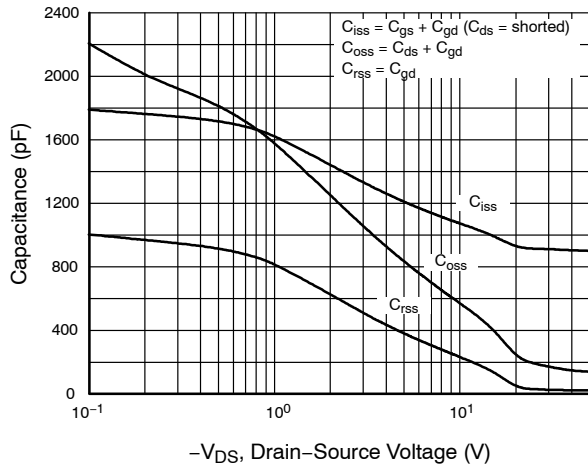


Figure 5. Capacitance Characteristics

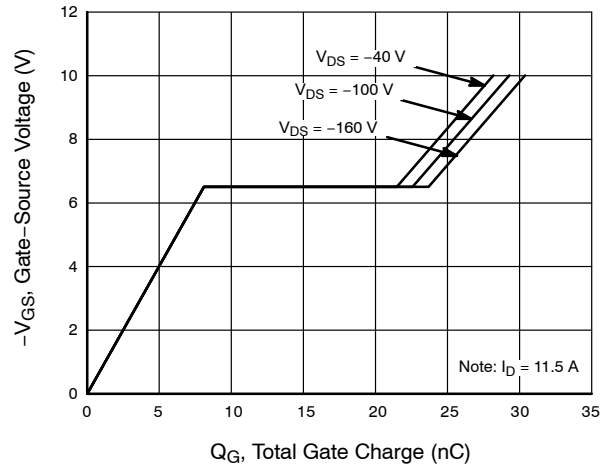


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

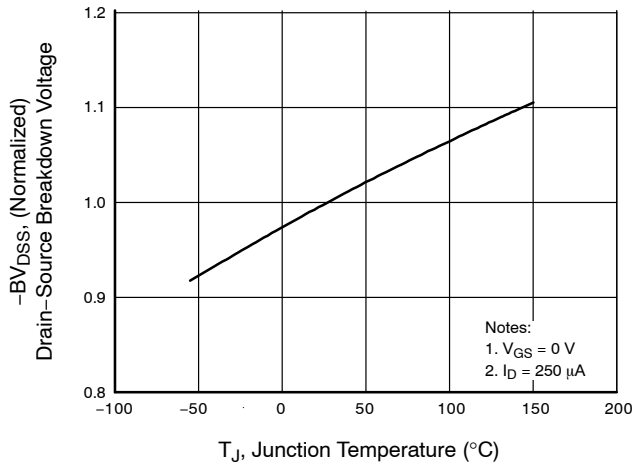


Figure 7. Breakdown Voltage Variation vs. Temperature

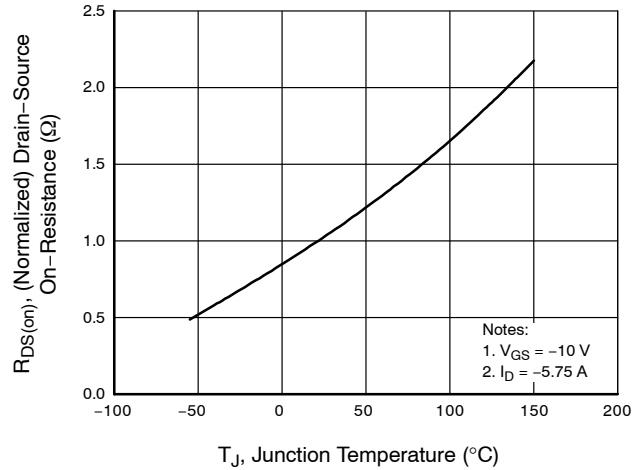


Figure 8. On-Resistance Variation vs. Temperature

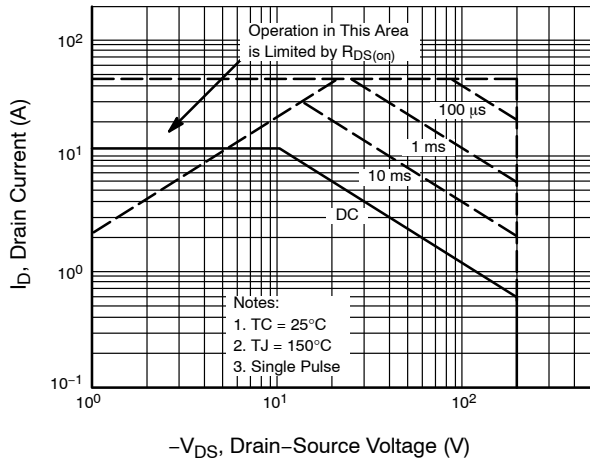


Figure 9. Maximum Safe Operating Area

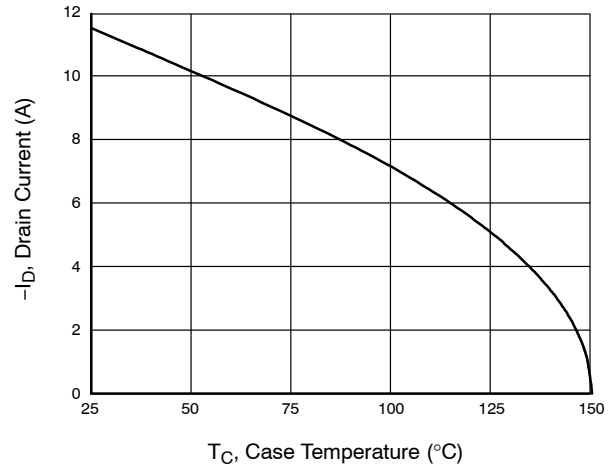


Figure 10. Maximum Drain Current vs. Case Temperature

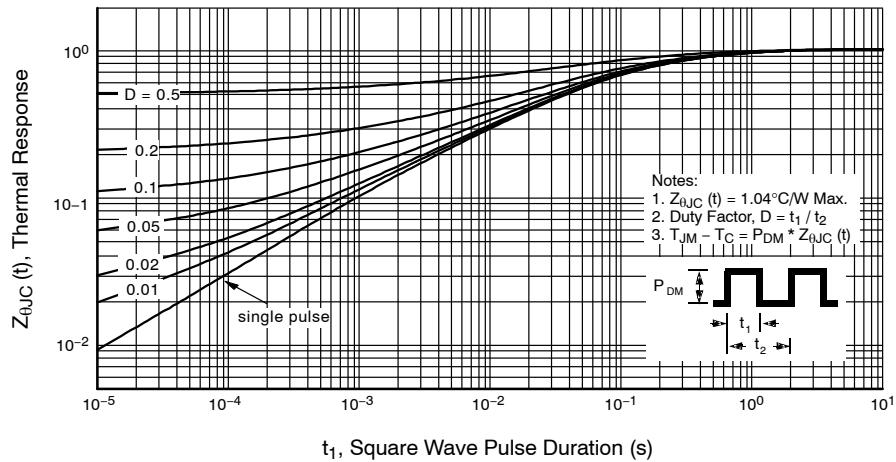


Figure 11. Capacitance Characteristics

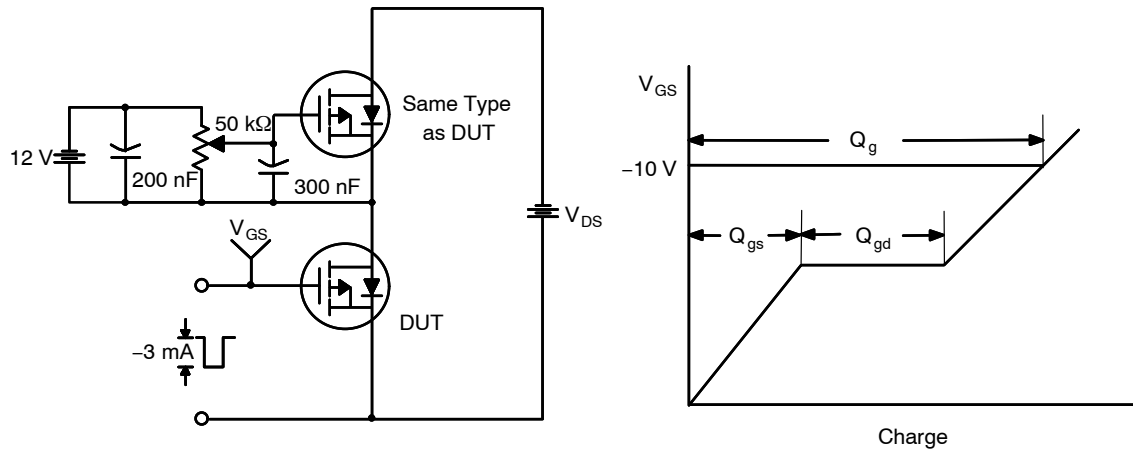


Figure 12. Gate Charge Test Circuit & Waveform

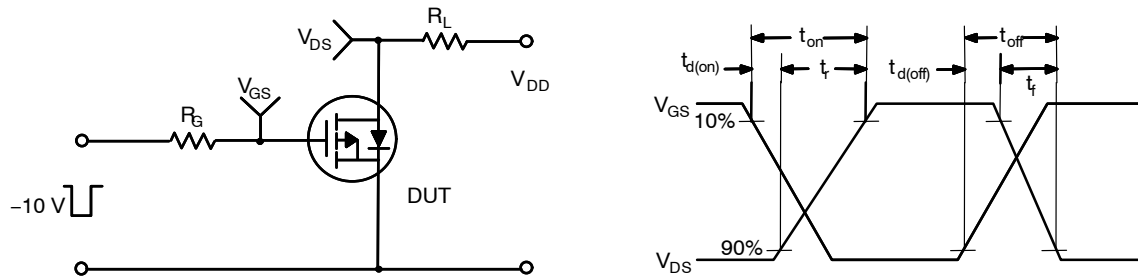


Figure 13. Resistive Switching Test Circuit & Waveforms

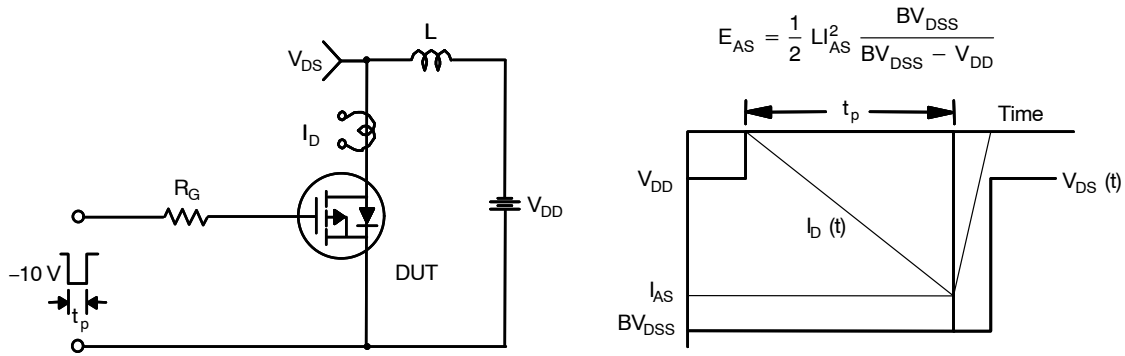


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

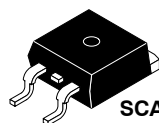
The circuit diagram shows a DUT (Device Under Test) connected to a driver. The driver is an N-channel MOSFET with gate resistor  $R_G$  and gate voltage  $V_{GS}$ . The DUT is an N-channel MOSFET with drain-source voltage  $V_{DS}$  and drain-source current  $I_{SD}$ . The DUT is connected to a load inductor  $L$  and a DC supply  $V_{DD}$ . The driver's gate is driven by a pulse with duty cycle  $D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$ . The waveforms show  $V_{GS}$  (Driver) as a pulse,  $I_{SD}$  (DUT) as a current pulse with reverse current  $I_{RM}$  and forward current  $I_{FM}$ , and  $V_{DS}$  (DUT) as a voltage pulse with forward voltage drop and recovery  $dv/dt$ .

## PACKAGE MARKING AND ORDERING INFORMATION

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

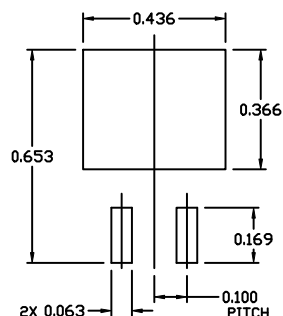
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SCALE 1:1

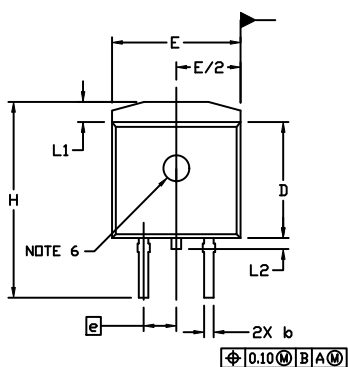
## D<sup>2</sup>PAK-3 (TO-263, 3-LEAD) CASE 418AJ ISSUE E

DATE 25 OCT 2019



### RECOMMENDED MOUNTING FOOTPRINT

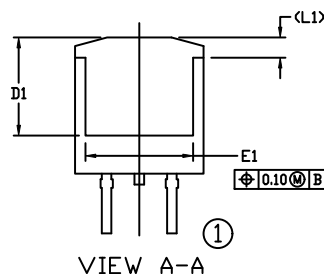
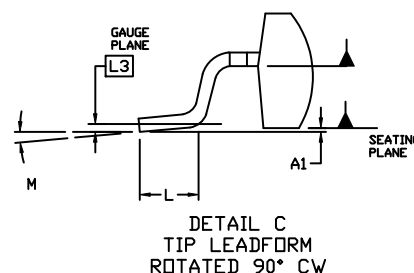
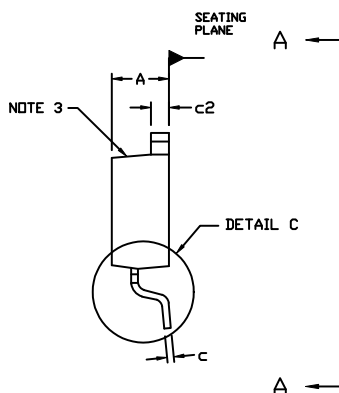
■ For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SD-106/D.



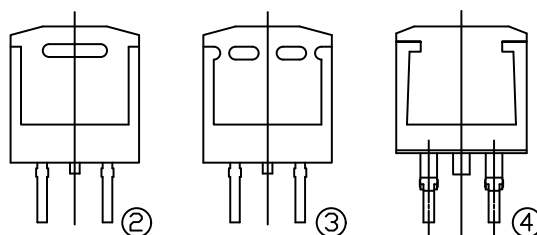
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	-8°	8°	-8°	8°

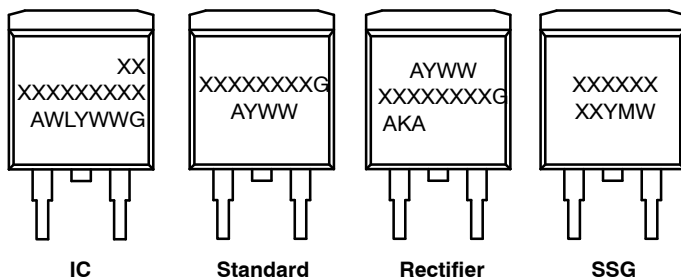


VIEW A-A



VIEW A-A  
OPTIONAL CONSTRUCTIONS

### GENERIC MARKING DIAGRAMS\*



IC

Standard

Rectifier

SSG

XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
W = Week Code (SSG)  
M = Month Code (SSG)  
G = Pb-Free Package  
AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D <sup>2</sup> PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 1

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