FAIRCHILD SEMICONDUCTOR™

July 1992
Revised August 2000

100391
Low Power Single Supply Hex TTL-to-PECL Translator

General Description

The 100391 is a hex translator for converting TTL logic levels to F100K PECL logic levels. The unique feature of this translator, is the ability to do this translation using only one +5V supply. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. A common enable (E), when LOW, holds all inverting outputs HIGH and all non-inverting inputs LOW.

The 100391 is ideal for those mixed PECL/TTL applications which only have +5V supply available. When used in the differential mode, the 100391, due to its high common mode rejection, overcomes voltage gradients between the TTL and PECL ground systems.

Features

- Operates from a single +5V supply
- Differential PECL outputs
- 2000V ESD protection
- Companion chip to 100390 hex PECL-to-TTL translator

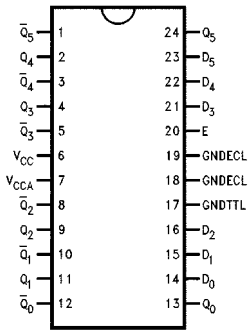
Ordering Code:

Order Number	Package Number	Package Description
100391SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100391PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100391QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100391QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (–40°C to +85°C)

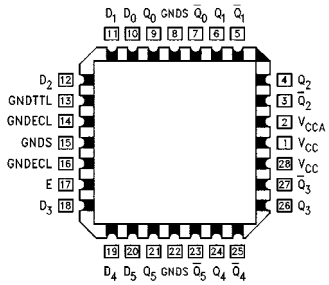
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

24-Pin DIP and SOIC



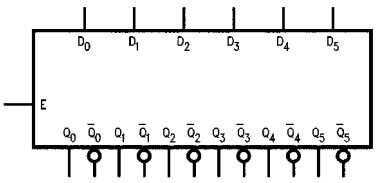
28-Pin PLCC



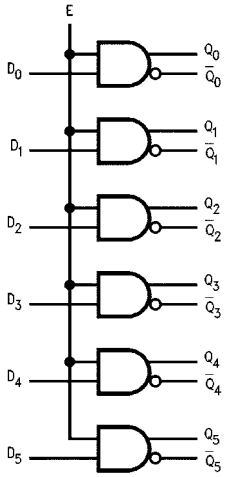
Pin Descriptions

Pin Names	Description
D_0 - D_5	Data Inputs (TTL)
Q_0 - Q_5	Data Outputs (PECL)
$\overline{Q}_0$ - $\overline{Q}_5$	Inverting Data Outputs (PECL)
E	Enable Input (TTL)

Logic Symbol



Logic Diagram



Truth Table

Inputs		Outputs	
D_n	E	Q_n	$\overline{Q}_n$
H	H	H	L
L	H	L	H
H	L	L	H
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note 1)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Pin Potential to Ground Pin (V_{CC})	−0.5V to +7.0V
PECL Output Current	
(DC Output HIGH)	−50 mA
TTL Input Voltage (Note 2)	−0.5V to +7.0V
TTL Input Current (Note 2)	−30 mA to + 5.0 mA
ESD (Last Passing Voltage)	
(Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Industrial	−40°C to +85°C
Commercial	0°C to +85°C
Supply Voltage (V_{CC})	4.5V to 5.5V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

TTL-to-PECL DC Electrical Characteristics (Note 4)

V_{CC} = +5.0V ± 10%, GND = 0V, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	V_{CC}– 1025	V_{CC}– 955	V_{CC}– 870	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL\ (min)}$
V_{OL}	Output LOW Voltage	V_{CC}– 1890	V_{CC} – 1705	V_{CC} – 1620	mV	Loading with 50Ω to V_{CC} – 2V
V_{OHC}	Output HIGH Voltage Corner Point High	V_{CC} – 1035			mV	V_{IN} = $V_{IH(min)}$ or $V_{IL\ (max)}$ Loading with 50Ω to V_{CC} – 2V
V_{OLC}	Output LOW Voltage Corner Point Low			V_{CC} – 1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input LOW Current			10	µA	V_{IN} = +2.7V
	Breakdown Test			20	µA	V_{IN} = +5.5V
I_{IL}	Input LOW Current Dn E	 –0.8 –4.2			mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2			V	I_{IN} = –18 mA
I_{CC}	V_{CC} Supply Current	32		69	mA	Inputs OPEN

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PDIP AC Electrical Characteristics

V_{CC} = 5.0V ± 10%

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.40	0.35	1.30	0.40	1.30	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.40	1.50	0.45	1.40	0.50	1.40	ns	Figures 1, 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	Figures 1, 2

Commercial Version (Continued)
SOIC and PLCC AC Electrical Characteristics

V_{CC} = 5.0V ± 10%

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.40	0.35	1.30	0.40	1.30	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.40	1.50	0.45	1.40	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		750		750		750	ps	PLCC Only (Note 5)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		700		700		700	ps	PLCC Only (Note 5)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		450		450		450	ps	PLCC Only (Note 5)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		525		525		525	ps	PLCC Only (Note 5)

Note 5: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

PLCC DC Electrical Characteristics (Note 6)

V_{CC} = +5.0V ± 10%, GND = 0V

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	V_{CC} − 1085	V_{CC} − 870	V_{CC} − 1025	V_{CC} − 870	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL\ (min)}$
V_{OL}	Output LOW Voltage	V_{CC} − 1830	V_{CC} − 1575	V_{CC} − 1830	V_{CC} − 1620	mV	Loading with 50Ω to V_{CC} − 2V
V_{OHC}	Output HIGH Voltage	V_{CC} − 1095		V_{CC} − 1035		mV	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$ Loading with 50Ω to V_{CC} − 2V
V_{OLC}	Output LOW Voltage		V_{CC} − 1565		V_{CC} − 1610	mV	
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	
V_{IH}	Input HIGH Current		10		10	µA	V_{IN} = +2.7V
	Breakdown Test		20		20	µA	V_{IN} = +5.5V
I_{IL}	Input LOW Current						
	D_n	−0.8		−0.8		mV	V_{IN} = +0.5V
	E	−4.2		−4.2			
V_{FCD}	Input Clamp Diode Voltage	−1.2		−1.2		V	I_{IN} = −18 mA
I_{CC}	V_{CC} Supply Current	29	69	29	69	mA	Inputs OPEN

Note 6: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PLCC AC Electrical Characteristics

V_{CC} = +5.0V ± 10%, GND = 0V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.20	1.50	0.35	1.30	0.40	1.30	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.35	1.60	0.45	1.40	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	

Switching Waveforms

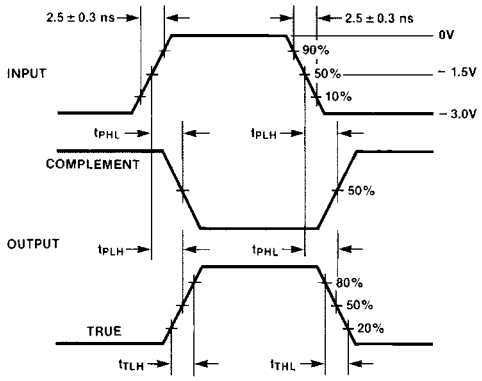


FIGURE 1. Propagation Delay, Cut-Off and Transition Times

Test Circuit

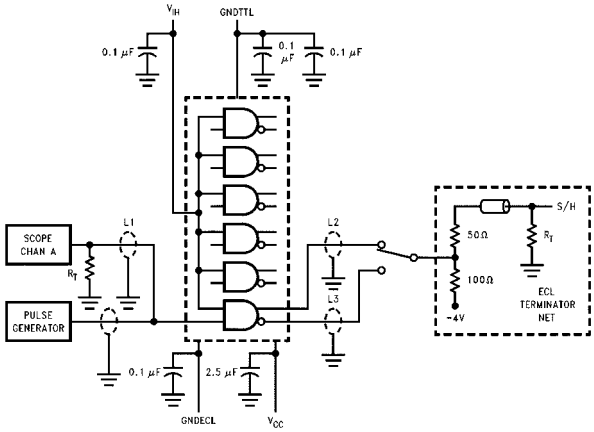


FIGURE 2. AC Test Circuit

Notes:

$V_{CC} = V_{CCA} = +2V$, GNDPECL = GNGTTL = 30.V

$V_{IH} = 0V$, $V_{IL} = -3V$

L1, L2 and L3 = equal length 50Ω impedance lines

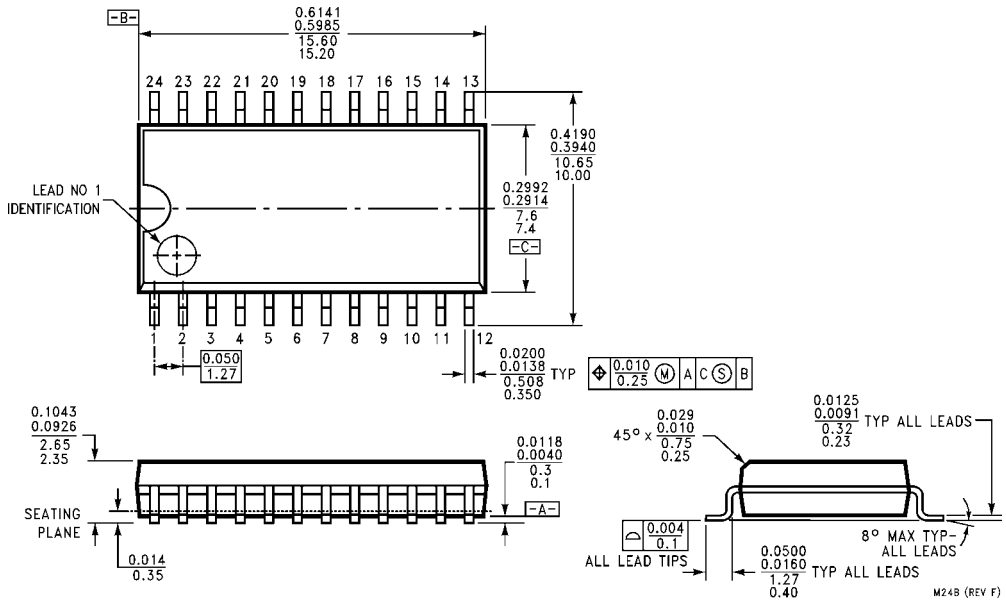
$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC}, V_{EE} and V_{TTL}

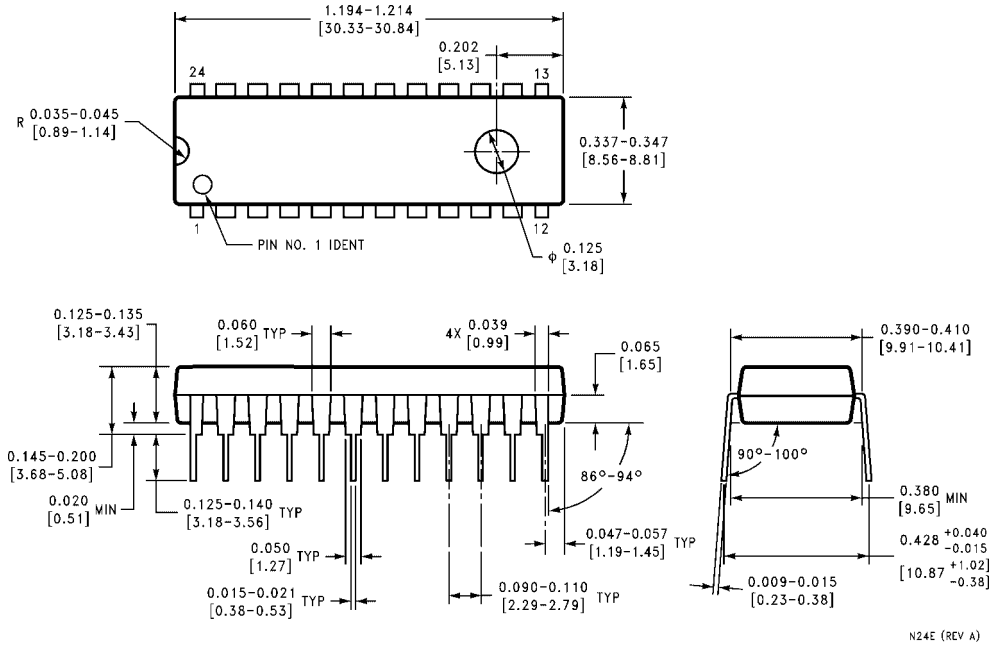
All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Physical Dimensions inches (millimeters) unless otherwise noted

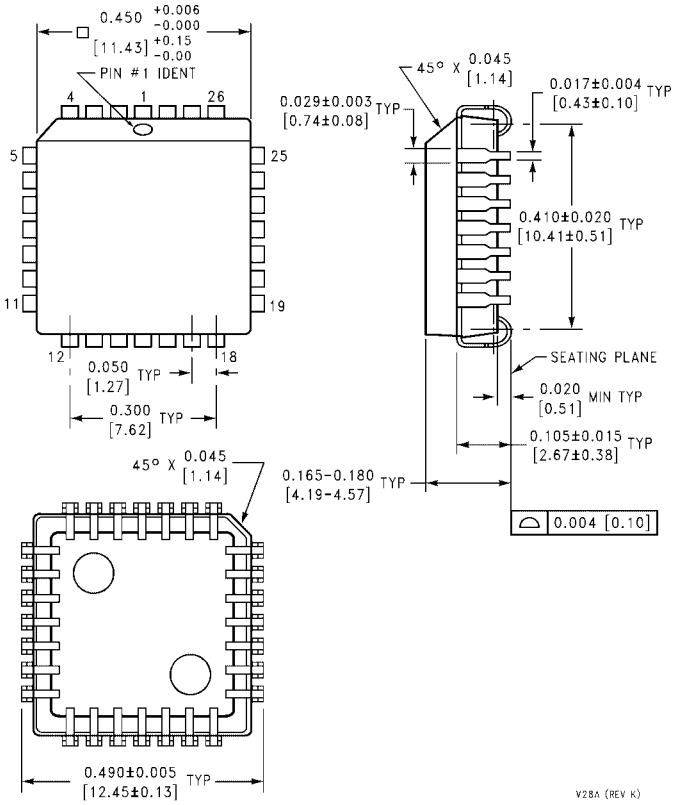


28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com