MOTOROLA Freescale Semiconductor, Inc.

Semiconductor Technical Data

Advance Information **Dual High Side Switch for H-Bridge Automotive Applications**

This device is a dual high side switch for automotive applications which incorporates a dual low side switch control feature. This device is designed to monitor two low side switches for typical DC-motor control in an H-Bridge configuration. It can be directly interfaced with a microcontroller for control and diagnostic functions, is PWM capable and has a self-adjusted switching speed for minimizing electromagnetic emission.

The High Side block incorporates two 15m Rdson N-Channel power Mosfets with senses and a control circuitry. Each output of this high side block is protected against short to gnd and load shorts, and has over temperature detection with hysteresis. It includes a current recopy feature for monitoring the load current. The control circuitry also has an overvoltage detector which turns off the bridge and protects the load in case of Vbat exceeding 28V.

The low side control block is able to drive 2 low sides switches in a H-bridge configuration and protects them in case of short circuit. This, in combination with the High side protection, fully protects the H-bridge from shorted loads, shorts to Vbat and shorts to GND.

- This device offers a very low quiescent current in standby mode.
- 10 Amps Nominal DC Current
- •35 Amps Maximum Peak Current
- •DC Voltage from -0.3V to 40V
- Operating Voltage from 8 to 28V
- Overvoltage Detection : Switch Off when Vbat Exceed 28V
- •High Side and Low Side Overcurrent protection
- Operating Junction Temperature 40°C to 150°C
- Rdson 15mΩ max at 25C° per Mosfet
- •DC to 30kHz PWM Capability
- Standby Mode with Low Standby Current
- •Junction to Case Thermal Resistance : 2°C/W
- ESD protection 2kV
- Current Recopy to Monitor the High-Side Current
- Common diagnostic output







This document contains information on a new product. Specifications and information herein are subject to change without police More Information On This Product,

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PINS FUNCTION DESCRIPTION

| Pin No. | Name/Function | Description |
|------------------------|---|--|
| ТАВ | V _{bat} Supply Voltage | The backside TAB is connected to the power supply of the MC33486DH. In addition to its supply function, the tab contributes to the thermal behaviour of the device by conducting the heat from the switching MOSFET to the printed circuit board. |
| 5,6,7,8 13,14,15,16 | OUT1 OUTPUT Channel 1 OUT 2 OUTPUT Channel 2 | Pins 5, 6,7,8 are the source of the output1 15mOhm High-side MOSFET1. Pins 13,14,15 are source of the output 2 15mOhm High-side MOSFET2. They are respectively controlled via the IN1 and IN2 pins. These outputs are current limited and thermally protected |
| 3 18 | IN 1 INPUT Channel 1 IN 2 INPUT Channel 2 | These are the device input pins which directly control their associated outputs. The levels are CMOS compatible. When the input is a logic low, the associated output is low (High Side OFF and Low Side ON). Each input pin has an internal active pull down, so that it will not float if disconnected. |
| 19 | St Status for both Channels | The Status output is an open drain indication that goes active low when a fault mode (Short to gnd/Vbat, Overtemp) is detected by the device on either one channel or both simultaneously. Its internal structure is an open drain architecture with an internal clamp at 6V. An external pull up resistor connected to Vdd (5V) is needed. See Functional Truth Table. |
| 4 17 | GLS1 GLS2 | These pins have to be connected to the gate of each Low Side. When the input (INx) is logic High, the associated GLS is grounded to turn off the external FET. |
| 20 | Wake | This pin is a digital input . When Wake is a logic low, the device's bias current draw is at a minimum. If Wake is a logic high, the part is operationnal. Wake pin has a pull down resistor. |
| 2 | Cur R Load Current Sense | The Current Sense pin deliver a ratioed amount (1/3700) of the sum of the High Side currents that can be used to generate signal ground referenced output voltages for use by the microcontroller. |
| 9, 10, 11, 12, | NC Not Connected | These pins are not used. |
| 1 | GND GROUND | This is the Ground pin of the device. |

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| AAXIMUM RATINGS | Semic | ònducto | or, Inc. |
|---|--|-------------------|----------|
| Parameter | Symbol | Value | Unit |
| Power Supply Voltage : Continuous/ Pulse | Vbat | - 0.3 to + 40 | V |
| Out1, Out2 to Vbat voltage : Continuous/ Pulse | Vout | - 0.3 to + 40 | V |
| IN1, IN2, Wake, ST Input DC voltage : Continuous/ Pulse | Vin | -0.3 to + 7 | V |
| IN1, IN2, Wake Input Current | lin | +/- 5 | mA |
| ESD all Pins Human Body Model (note1) Machine Model (note2) | V _{esd1} V _{esd2} | +/-2000 +/-200 | V V |
| Output DC Output Current, 1 Channel ON, Ta=85°C (note4) | loudc | 10 | А |
| Output Current : Pulse (Note 3) | loutp | 35 | А |
| | | 1 | |

THERMAL RATINGS

| Junction Temperature | Tj | - 40 to +150 | °C |
|---|-------|--------------|------|
| Storage Temperature Range | Tst | - 65 to +150 | °C |
| Thermal resistance junction to case | Rthjc | 2 | °C/W |
| Thermal resistance junction to ambient (Note 4) | Rthja | 25 | °C/W |
| Power dissipation at Tcase 140°C (Note 5) | Pd | 5 | W |

NOTES : 1. ESD1 testing is performed in accordance with the Human Body Model (Czap = 100pF, Rzap = 1500Ω) 2. ESD2 testing is performed in accordance with the Machine Model (Czap = 100pF, Rzap = 0Ω)

3. During load in rush current.

4. Device mounted on dual side printed circuit board with 70μm copper thickness and 10cm² copper heat sink (2.5 cm² on top side and 7.5 cm² on down side).

5. Assuming a 150°C maximum junction temperature.

ELECTRICAL CHARACTERISTICS High Side Block

T_i from - 40°C to +150°C, V_{bat} from 9V to 16V, unless otherwise noted.Typical values reflect approximate mean at 25°C, nominal V_{bat}, at time of device characterization.

| Description | Symbol | CI | naracterist | lics | Unit | Conditions | |
|--|--------------------|------|-------------|------|------|---|--|
| Description | Symbol | Min. | Тур. | Max. | Onic | | |
| SUPPLY CHARACTERISTICS | | | • | • | | | |
| Nominal Operating Voltage | V _{bat} | 8 | | 28 | V | Functional to truth table until overvoltage threshold | |
| Standby Current | I _{stdby} | | | 10 | μΑ | Vbat < 13.5V, wake=0, IN1=IN2=0 | |
| Supply Current in Operation Mode | I _{on} | | 9 | 15 | mA | No PWM, IN1or IN2=5V, Wake=5V | |
| Supply Current in Operation Mode | I _{tbd} | | 15 | | mA | PWM=20kHz, d=50% | |
| STATIC OUTPUT CHARACTERISTICS | | | | • | | | |
| High Side Drain to Source On Resistance | R _{dson} | | 12 | 15 | mΩ | lout =5A, $T_j = 25^{\circ}C$ | |
| High Side Drain to Source On Resistance | R _{dson} | | 21 | 30 | mΩ | lout = 5A, V_{bat} > 9V & T_j = 150°C | |
| High Side Body Diode Voltage (Out to Vbat) | V_{bd} | | | 0.7 | V | @ lout=-5A, Tj = 150°C | |
| Low Side Gate output Voltage | Vgs | | | 14 | V | Internally clamped | |

| | | С | haracterist | ics | | |
|--|----------------------------|----------------|-------------|-----------|------------|---|
| Description | Symbol | Min. Typ. Max. | | Unit | Conditions | |
| INPUTS CHARACTERISTICS IN1, IN2, Wak | e | | | | | |
| Input low levels | Vil | | | 1.5 | V | |
| Input high levels | Vih | 3.5 | | | v | |
| Input Hysteresis | Vhyst | 0.2 | 0.6 | 1 | v | IN1 and IN2 pins only |
| Logic Input Current | lin | 1 | | | μA | Vin = 1.5V |
| Logic Input Current | lin | | | 50 | μA | Vin = 3.5V |
| STATUS CHARACTERISTICS | 11 | | | | | |
| Status Voltage | Vst | | | 0.5 | V | Ist=1mA, output in fault |
| Status Leakage | Istlk | | | 10 | μA | Vst=5V |
| OVERLOAD PROTECTION CHARACTERIS | TICS | | | | | 1 |
| High Side Output Current Shutdown | l _{lim} | 20 | 35 | 50 | A | |
| High Side Overcurrent Shutdown Delay | tllim | | 3 | 20 | μs | From short to output shutdown |
| Low Side Overcurrent detection Vout to gnd | V _{out-} fault | 1 | 2 | 3 | V | If the low side is ON (GLS>4.3V). This is a inferred overcurrent con dition |
| Low Side Overcurrent detection Vout to gnd Shutdown Delay | t _{out-fault} | | 3 | 10 | μs | |
| Thermal Shutdown | T _{shut} | 150 | 175 | | °C | |
| Thermal Shutdown Hysteresis | T _{hyst} | | 10 | | °C | |
| Under Voltage Shutdown Threshold | Vuv | 6 | | 8 | V | |
| Under Voltage Shutdown hysteresis | Vuv-hyst | | 0.15 | | V | |
| Over Voltage Shutdown Threshold | Vov | 27 | 29 | 31 | V | |
| Over Voltage Shutdown hysteresis | Vov-hyst | | 0.15 | | V | |
| CURRENT RECOPY CHARACTERISTICS | | | | | 1 | 1 |
| Current Recopy Ratio | Cr | | 3700 | | | lout from 4A to 8A Tj -40°C to 105°C |
| Current Recopy Ratio Accuracy lout from 4A to 8A lout from 8A to 20A | Cr-ac | -15 -10 | | 15 10 | % | Tj <125°C Garanteed by design |
| Current Recopy Clamp Voltage | Vclst | 6 TBC | 9 | 11 TBC | V | Current mirror=10mA No external resistor on Cur R pin |
| SWITCHING CHARACTERISTICS | <u> </u> | | 1 | 1 | <u>ı</u> | 1 |
| High Speed Mode to Low Speed Mode transition pulse width | tsmod | 150 | 250 | 350 | μs | |
| Gate Low Side Rise Time | Tpsrls | | 3.6 | | μs | From 10% to 90% Vout, Load=30 |
| Gate Low Side Fall Time | Tnsrls | | 4.9 | | μs | From 90% to 10% Vout, Load=30 |

| | | | | | ., | | |
|--|-----------------|------|-------------|------|------|---------------------------------------|--|
| Description | Symbol | Cł | naracterist | ics | Unit | Conditions | |
| Description | Symbol | Min. | Тур. | Max. | Unit | Conditions | |
| High Side Positive Slew Rate | Thr | | 10 | | V/µs | From 10% to 65% Vout, Load=3 Ω | |
| High Side Negative Slew Rate | Thf | | 40 | | V/µs | From 90% to 35% Vout, Load=3 Ω | |
| High Side Turn on Delay Time | thdon | | 2.5 | | μs | To 10% Vout, Load=3Ω | |
| High Side Turn off Delay Time | thdoff | | 1.5 | | μs | To 90% Vout, Load=3 Ω | |
| LOW SPEED MODE SWITCHING CHARACTERISTICS | | | | | | | |
| High Side Maximum Output Positive Slew Rate | lr | | 1.0 | | V/µs | From 10% to 65% Vout, Load=3 Ω | |
| High Side Maximum Output Negative Slew Rate | T _{lf} | | 0.5 | | V/µs | From 90% to 35% Vout, Load=3 Ω | |
| High Side Turn on Delay TIme | tldon | | 10 | | μs | To 10% Vout, Load=3Ω | |
| High Side Turn off Delay Time | tloff | | 80 | | μs | To 90% Vout, Load=3Ω | |

FUNCTIONAL TRUTH TABLE

| Standard HBridge Conditions | In1 | ln 2 | Wake | Out1 | Out2 | GLS1 | GLS2 | St | Comment |
|-----------------------------|-----|------|------|------|------|------|------|----|---------------------------|
| | Х | х | 0 | Z | Z | L | L | 1 | Standby Mode |
| | 0 | 0 | 1 | L | L | Н | н | 1 | Brake to Ground |
| Normal Operation | 1 | 0 | 1 | Н | L | L | н | 1 | Direction 1 |
| | 0 | 1 | 1 | L | Н | н | L | 1 | Direction 2 |
| | 1 | 1 | 1 | н | Н | L | L | 1 | Not Recommended Note 1 |
| Undervoltage | Х | х | 1 | Z | Z | L | L | 1 | Note 2 |
| Overvoltage | Х | х | 1 | L | L | Н | н | 1 | Note 2 |
| Overtemp HS1 | Н | L | 1 | L | L | L | L | 0 | Note 3 |
| Overtemp HS2 | L | Н | 1 | L | L | L | L | 0 | Note 3 |
| Overcurrent HS1 | 1 | х | 1 | Z | Х | L | Х | 0 | Note 4 |
| Overcurrent HS2 | Х | 1 | 1 | Х | Z | х | L | 0 | Note 4 |
| Overcurrent LS1 | Х | х | 1 | Z | Z | L | L | 0 | Note 5 |
| Overcurrent LS2 | Х | Х | 1 | Z | Z | L | L | 0 | Note 5 |

L = 'Low level' ; H = 'High level' ; X = 'don't care' ; Z = 'High Impedance'

NOTES :

NOTES :
1. It is not recommended to short the motor to Vbat. If in this mode an overvoltage condition occured, this would damaged the DHSB.
2.Once the overvoltage condition or undervoltage condition is removed, the H-Bridge recovers its normal operation mode.
3.When the thermal shutdown is reached on one of the High Side MOSFET, both half bridges are turned off with the motor tied to ground. When the overtemperature condition is finished, the H-bridge recover it previous normal operation mode.
4. The High Side MOSFET HSx which experienced an overcurrent is latched off. The corresponding output OUTx is open. Once the High Side overcurrent condition is removed, the input INx has to to be reset in order to recover the normal operation mode.
5. When a short to Vbat of one of the Low sides occurs, both outputs are opened to prevent the motor from running. Once the Low side overcurrent is removed, the input INx of the half bridge wich experienced the fault has to be reset in order to recover the normal operation mode.

DEVICE DESCRIPTION

Introduction

These devices are intended for full H-bridge automotive applications. The bridge is partitioned into three blocks, the DHSB and two low side MOSFETS, each block has a dedicated package.

The DHSB incorporates two 15m ohm N-channel high side power MOSFETS, high side current sensing , fault protection and low side gate drivers. The inputs are CMOS compatible, so they can directly interface with a microncontroller. The low side gate drivers control and protect the two external low sides. When the three blocks are combined the outputs (OUT1 and OUT2) are fully protected against shorts to GND, Shorts to Vbat, shorted loads, over/ under voltage and over temperature.

Power supply

The device can be directly connected to the power supply line. The device has a standby mode (Wake at low logic level) with a ultra low consumption (10uA max). In operation when inputs are active, the supply current is up to 20mA.

With the high current and fast switching ability of the DHSB it is recommended that sufficient capacitance (tens of microfarads) be placed between Vbat and gnd of the IC. This will help to insure the power supply stays within the specified limits.

Reverse battery protection.

The device cannot sustain more than 1.5V of a reverse battery conditions because of the two body diodes of the power MOSFETs, which are forward biased during a reverse battery condition. A specific protection must be implemented.

Figure 1. i Reverse Battery protection schematic



A reverse battery component might be needed in the gnd pin of the application (i.e diode or Mosfet) in order to achieve both reverse battery and negative transient pulses immunity.

If a polarized capacitor is used, it can be placed as shown in Figure 1. .

Loss of ground protection

As shown in the Figure 1., a loss of ground has no bad impact on the DHSB, since the ground pin of the device is the same as the ground of the low side.

Over/Under Voltage Protection

If the battery voltage falls to a level below 8.0V, the outputs are turned low (Low Sides ON) in a low speed mode. The DHSB goes back into normal operation mode as soon as the Vbat rise above the undervoltage threshold. The undervoltage protection circuitry has hysteresis.

The control circuitry also has an overvoltage detection which turns the Low sides ON and protects the load in case of Vbat exceeding 28V.The gate drivers will also be clamped to 14V to protect the external low side FETs. The Low sides remain in the ON state, until the over-voltage condition is removed.

Undervoltage and Overvoltage are not reported on the status output.

Self-adjusted switching speed mode

This feature allows for reduction in EMC and power dissipation depending on the application. The DHSB has two switching speeds (high and low) depending on the input pulse width. The high speed condition is active when the delay between two consecutive input edges is below 280us. The low speed mode is active when the delay between two consecutive input edges is above 280us. The 280us delay corresponds about to a 2kHz frequency with a duty cycle of 50%.

Current Recopy

This feature provides a current mirror with the ratio of 1/ 3700 of the high side output current. An external resistor must be connected to the Cur R pin and then tied to a microcontroller A/D input for analog voltage measurement. The Cur R pin is internally clamped (Vclst) to protect the MCU A/D input.

Figure 2. Current Recopy Principle.



In case a ground shift occurs between the MCU and the DHSB, the amplifier A (see Figure 2.), will adapt its output to keep the same I copy. Of course the shift has to keep between +/- 1V.

Status

The device has a single status pins which reports over temperature and/or over current faults. See the Functional Truth Table for all faults that are reported on this signal pin. This pin is an open drain structure and needs an external pull up resistor.

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DEVICE DESCRIPTION

Overtemperature Protection

The DHSB incorporates over-temperature protection. Overtemperature detection occurs when an internal high side is in the on state. When an over-temperature condition occurs, both outputs are affected. Both outputs are turned off to protect the DHSB from damage (Low sides ON). The overtemperature protection circuitry incorporates hysteresis. Overtemperature fault condition is reported on the status output.

High side overcurrent protection

This device incorporates a current shutdown threshold of 35A typical. When this limit is reached due to an overload condition or a short to ground, the faulty output is tri-stated. To clear the fault the input (Inx) line needs to return low then on the next high transition the output will be enabled.

This information is reported on the status output.

Low side block

The low side block has control circuitry for two external N-Channel power MOSFET's. The low side control circuitry is PWM capable and protects the Low side MOSFETS in case of overcurrent (short to Vbat). This information is reported on the status output.

The low side Gate controls are clamped at14V maximum to protect the gates of the Low Sides.

During normal operation, the outputs OUT1 and OUT2 are driven by the high side. The low side Gate driver's will only turn on when the Drain voltage (same connection as OUT1 or 2) of the internal high sides is less than 2V, which prevent any cross-conduction in the bridge.

Low Side Overcurrent Protection

Unlike the high side overcurrent circuitry, this overcurrent protection does not measure the current , but measures the effect of current on the low side through a condition : Vgs > 4.3V and Vds >2V. When this set of conditions occur for at least 8us (blanking time), both outputs OUT1 and OUT2 are tri-stated. The full bridge is tri-stated to prevent the motor for running in case of short to Vbat.

As Vgs and Vds are measured in respect to the DHSB's ground pin, it is essential that the low side source are connected to this same ground, in order to prevent false overcurrent detection due to ground shifts.

Package

The high side block is assembled into a power surface mount package. This package offers high thermal performances, and high current capabilities. It offers 10 pins on each package sides, and one additional connection which is the package heat sink (called pin 21). The heat sink acts as the device power Vbat connection.

Soldering Information

This device is packaged in a Surface Mount Power package indended to be soldered directly on the Printed Circuit Board.

This device was qualified according to JEDEC standards JESD22-A113-B and J-STD-020A with the reflow conditions applicable for packages with thickness above 2.5mm :

Convection 220°C +5/-0°C VPR 215-219°C

IR / Convection 220°C +5/-0°C

The maximum peak temperature during the soldering process should not exceed 220°C (+5°C/-0°C). The time at maximum temperature should range from 10 to 40s max.

Thermal Management

The junction to case thermal resistance is $2^{\circ}C/W$ maximum. The junction to ambient thermal resistance is dependant on the mounting technology, and if an additional heat sink is used. One of the most commonly used mounting technique consists of using the printed circuit board and the copper lines as heat sink.

Figure 2 is an example of printed circuit board layout. It has a total of 10 cm^2 additional copper on two sides (2.5 cm² on the top side and 7.5 cm² on the down side).

Figure 3. .Printed Board Layout Example (not to scale)



With the above layout, thermal resistance junction to ambient of 25° C/W can be achieved. This value being splitted into :

. junction to case : Rthjc = $2^{\circ}C/W$

. case to ambient : Rthca = $23 \circ C/W$.

Lower value can be reached with the help of larger and thicker copper metal, higher number of thermal via from top to bottom side pcb and the use of additional thermal via from the circuit board to the module case.

Thermal model

The junction to ambient thermal resistance of the circuit mounted on a printed circuit board can be splitted into two main parts: junction to case and case to ambient resistances.

A simplified steady state model is shown in figure 3 below.

Figure 4. Simplified Thermal Model (Electrical Equivalent)



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The use of this model is similar to the electrical Ohm law (voltage = resistance X current), where:

. Voltage represents temperature

. Current represents power dissipated by the device

. Resistance represents thermal resistance.

We finally got :

Temperature or delta temperature = Power Dissipation times Thermal resistance, that is : $^{\circ}C = W ^{\circ} x C/W$.

Any node temperature can easily be calculated knowing the amount of power flowing through the thermal resistances.

Example :

1. Numerical value.

. Junction to case thermal resistance : 2°C/W (Rthjc)

. Power into the switch : assuming the device is driving 8 amps at 150°C junction temperature (Rdson at 150°C is $40m\Omega$) the total power dissipation is : 0.04*8*8 = 2.56W

. Case to ambient thermal resistance (Rthca) : 20°C/W

2. Results.

- . Junction to case delta temp : 5°C (2.5W x 2°C/W)
- . Case delta temp from ambient : 50°C (20°C/W x 2.5W)
- . Actual junction temperature node will be :
- $50^{\circ}C + 5^{\circ}C = 55^{\circ}C$ above the ambient temperature.

Assuming an 85°C ambient temperature, the junction temperature is a t : 85 + 55 = 140°C.

The above example take into account the junction to ambient thermal resistance, assuming that the ambient temp is 85°C. In the case where the device plus its printed circuit board are located inside a module, the ambient temp of the module should be taken into account. Or an additional thermal resistance from inside module to external ambient temperature must be added. The calculation method remains the same.

The low side block is packaged into D²PAK or DPAK package. Thermal resistance junction to case is approx. 2°C/W. The junction to ambient thermal resistance follows the same rules as for the high side block, and is in the same range.

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