

74F38

Quad 2-input NAND buffer (open collector)

Rev. 3 — 10 January 2014

Product data sheet

1. General description

The 74F38 provides four 2-input NAND functions with open-collector outputs.

2. Features and benefits

- Industrial temperature range available (–40 °C to +85 °C)

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|-------|--|----------|
| | Temperature range | Name | Description | Version |
| N74F38N | 0 °C to +70 °C | DIP14 | plastic dual in-line package; 14 leads (300 mil) | SOT27-1 |
| I74F38N | –40 °C to +85 °C | | | |
| N74F38D | 0 °C to +70 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| I74F38D | –40 °C to +85 °C | | | |



4. Functional diagram

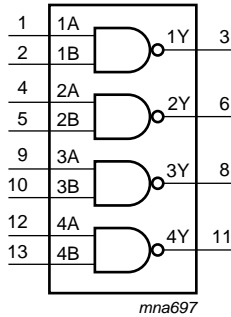


Fig 1. Logic symbol

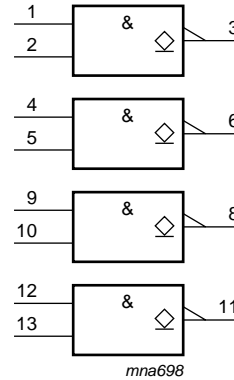


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

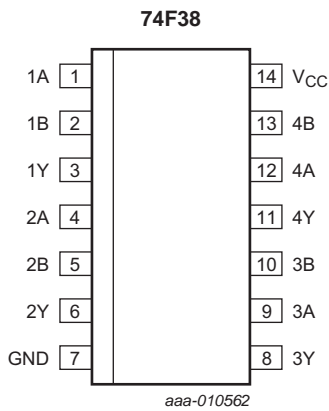


Fig 3. Pin configuration DIP14 and SO14 package

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description | Unit load HIGH/LOW | Load value ^{[1][2]} HIGH/LOW |
|-----------------|--------------|----------------|-----------------------|--|
| 1A, 2A, 3A, 4A | 1, 4, 9, 12 | data input | 1.0/2.0 | 20 μ A/1.2 mA |
| 1B, 2B, 3B, 4B | 2, 5, 10, 13 | data input | 1.0/2.0 | 20 μ A/1.2 mA |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output | OC/106.7 | OC/64 mA |
| GND | 7 | ground (0 V) | - | - |
| V _{CC} | 14 | supply voltage | - | - |

[1] One FAST Unit Load (UL) is defined as 20 μ A in HIGH state, 0.6 mA in LOW state.

[2] OC = open collector.

6. Functional description

Table 3. Function table^[1]

| Input | | Output |
|-------|----|--------|
| nA | nB | nY |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|------------------------|----------------------|---------------------|-----------------|------|
| V _{CC} | supply voltage | | -0.5 | +7.0 | V |
| V _I | input voltage | | ^[1] -0.5 | +7.0 | V |
| V _O | output voltage | output in HIGH-state | ^[1] -0.5 | V _{CC} | V |
| I _{IK} | input clamping current | V _I < 0 V | -30 | +5 | mA |
| I _O | output current | output in LOW-state | - | 128 | mA |
| T _{amb} | ambient temperature | in free-air | ^[2] | | |
| | | commercial | 0 | 70 | °C |
| | | industrial | -40 | +85 | °C |
| T _{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------|------------|-----|-----|-----|------|
| V_{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | | - | - | 4.5 | V |
| I_{IK} | input clamping current | | -18 | - | - | mA |
| I_{OL} | LOW-level output current | | - | - | 64 | mA |

9. Static characteristics

Table 6. Static characteristics

| Symbol | Parameter | Conditions | 25 °C | | | 0 °C to +70 °C | | Unit |
|----------|--------------------------|--|-------|--------------------|-----|----------------|------|---------------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V_{IK} | input clamping voltage | $V_{CC} = 4.5 \text{ V}$; $I_{IK} = -18 \text{ mA}$ | -1.2 | -0.73 | - | -1.2 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 4.5 \text{ V}$; $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.0 \text{ V}$ $I_{OL} = 64 \text{ mA}$ | - | - | - | - | - | |
| | | $V_{CC} = \pm 10 \%$ | - | - | - | - | 0.55 | V |
| | | $V_{CC} = \pm 5 \%$ | - | 0.42 | - | - | 0.55 | V |
| I_I | input leakage current | $V_{CC} = 0 \text{ V}$; $V_I = 7.0 \text{ V}$ | - | - | - | - | 100 | μA |
| I_{IH} | HIGH-level input current | $V_{CC} = 5.5 \text{ V}$; $V_I = 2.7 \text{ V}$ | - | - | - | - | 20 | μA |
| I_{IL} | LOW-level input current | $V_{CC} = 5.5 \text{ V}$; $V_I = 0.5 \text{ V}$ | - | - | - | -20 | - | μA |
| I_{CC} | supply current | $V_{CC} = 5.5 \text{ V}$ | - | - | - | - | - | |
| | | $V_I = \text{GND}$ | - | 4 | - | - | 7 | mA |
| | | $V_I = 4.5 \text{ V}$ | - | 22 | - | - | 30 | mA |

[1] All typical values are measured at $V_{CC} = 5 \text{ V}$.

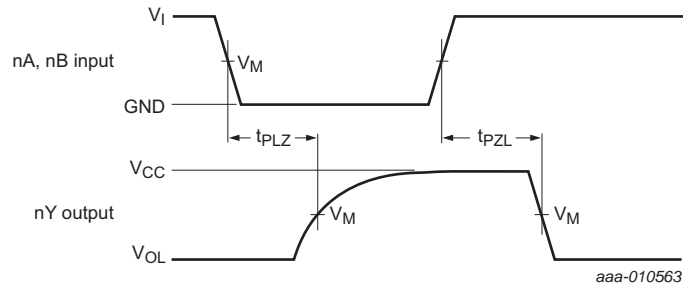
10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0 \text{ V}$. Test circuit is shown in [Figure 6](#).

| Symbol | Parameter | Conditions | 25 °C; $V_{CC} = 5.0 \text{ V}$ | | | 0 °C to +70 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ | | -40 °C to +85 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ | | Unit |
|-----------|------------------------------------|---|------------------------------------|------|------|---|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_{PZL} | OFF-state to LOW propagation delay | nA, nB to nY; see Figure 4 | 1.5 | 3.0 | 5.0 | 1.5 | 5.5 | 1.5 | 6.0 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | nA, nB to nY; see Figure 4 | 7.5 | 10.0 | 12.5 | 7.5 | 13.0 | 7.5 | 14.5 | ns |

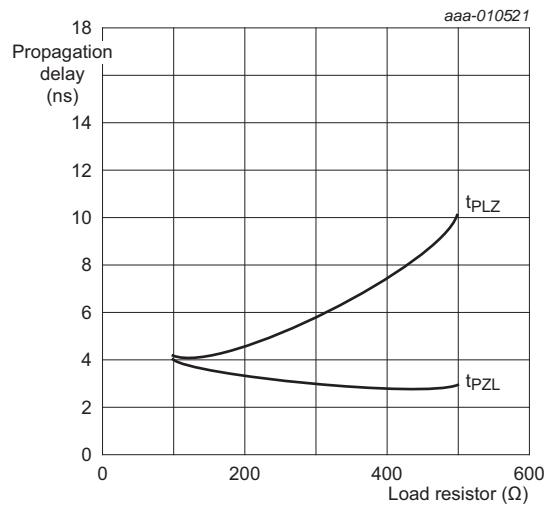
11. Waveforms



$V_M = 1.5\text{ V}$

V_{OL} is a typical output voltage level that occurs with the output load.

Fig 4. Propagation delay for inverting outputs



When using open collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLZ} . For example, changing the specified pull-up resistor value from 500 Ω to 100 Ω improves the t_{PLZ} up to 50% with only a slight increase in the t_{PZL} . However, if the value of the pull-up resistor is changed, the user must ensure that the total I_{OL} current through the resistor and the total I_{IL} of the receivers, does not exceed the I_{OL} minimum specification.

Fig 5. Typical propagation delays versus load for open collector outputs

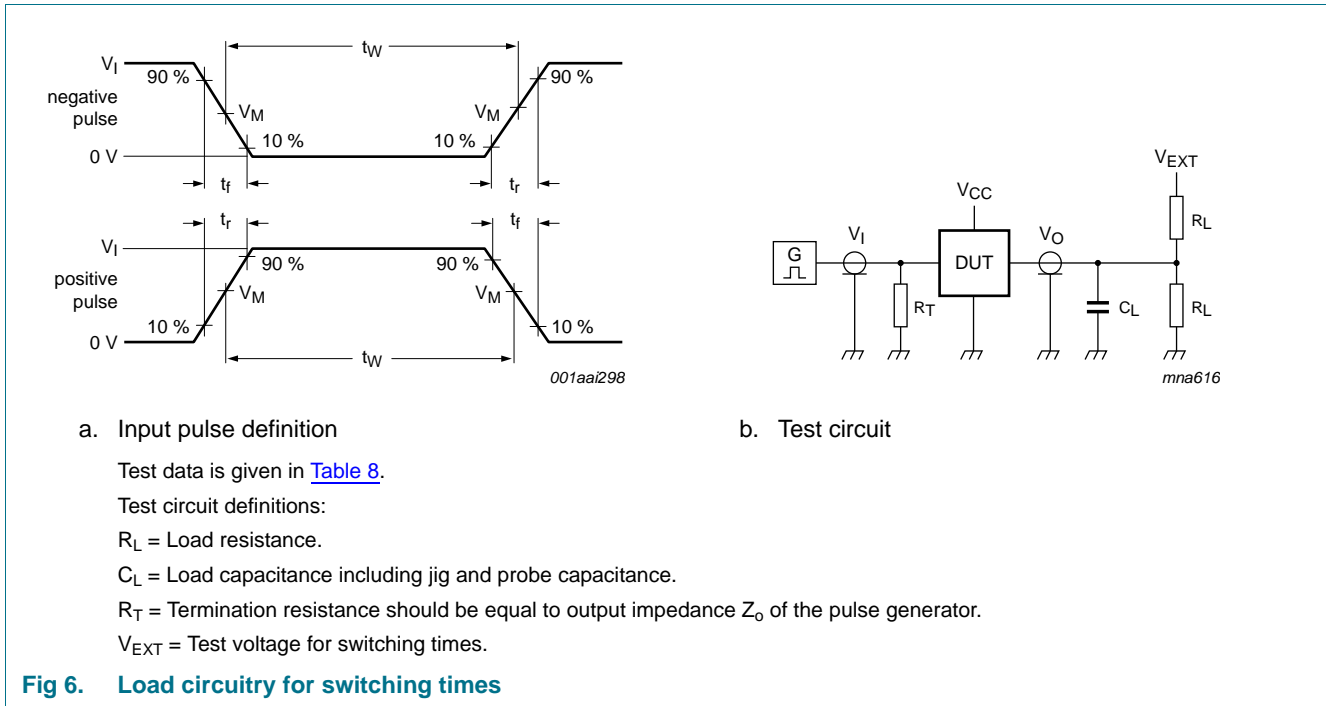


Table 8. Test data

| Input | | | | Load | | V_{EXT} |
|-------|-------|--------|---------------|-------|--------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PZL}, t_{PLZ} |
| 3.0 V | 1 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | 7.0 V |

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

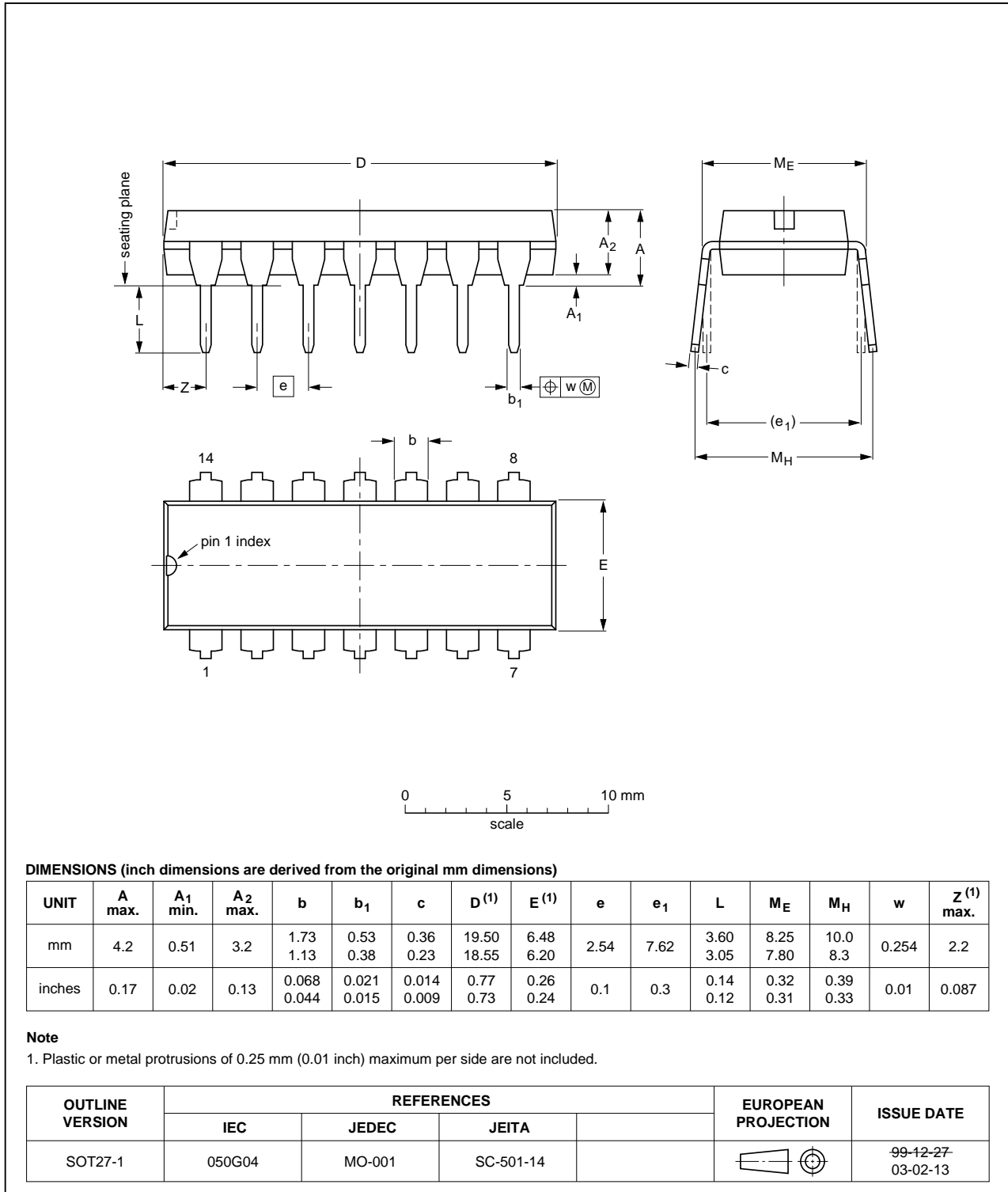


Fig 7. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

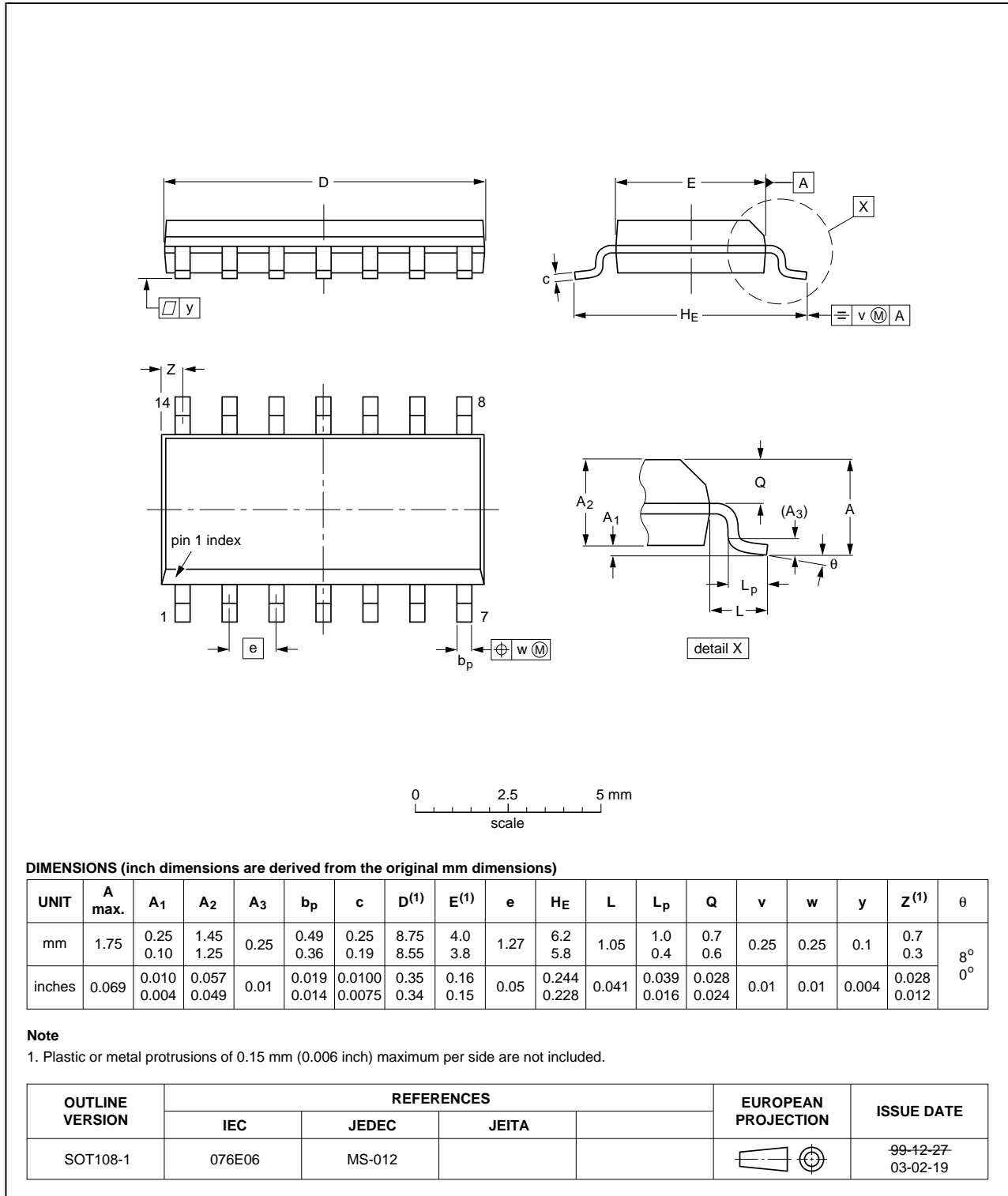


Fig 8. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--------------|---|---------------|------------|
| 74F38 v.3 | 20140110 | Product data sheet | - | 74F38 v.2 |
| Modifications: | | <ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate.General update of values | | |
| 74F38 v.2 | 19901004 | Product specification | - | - |

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|-----------------------------------|-------------------------------|---|
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