74AHC1G07

Buffer with open-drain output

Rev. 8 — 25 February 2019 Product data sheet

1. General description

74AHC1G07 is a high-speed Si-gate CMOS device. It provides a non-inverting buffer.

The output of this device is open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

The 74AHC1G07 has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

2. Features and benefits

- High noise immunity
- Low power dissipation
- ESD protection:
  - HBM JESD22-A114E: exceeds 2000 V
  - MM JESD22-A115-A: exceeds 200 V
  - CDM JESD22-C101C: exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G07GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHC1G07GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

4. Marking

Table 2. Marking codes

Type number	Marking [1]
74AHC1G07GW	AS
74AHC1G07GV	A07

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

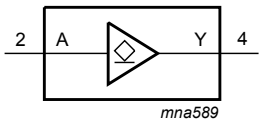


Fig. 1. Logic symbol

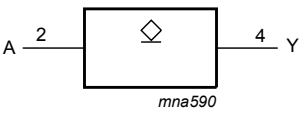


Fig. 2. IEC logic symbol

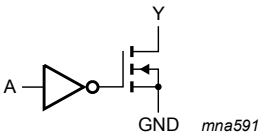


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

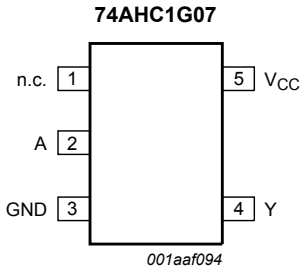


Fig. 4. Pin configuration SOT353-1 (TSSOP5) and SOT753 (SC-74A)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V_{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
A	**Y**
L	L
H	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V		-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V	[1]	-	±20	mA
I_O	output current	V_O > -0.5 V		-	±25	mA
V_O	output voltage	active mode	[1]	-0.5	+7.0	V
		high-impedance mode	[1]	-0.5	+7.0	V
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For both TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		high-impedance mode	0	-	6.0	V
T_{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	ns/V
		V_{CC} = 5.0 V ± 0.5 V	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.25		±2.5		±10.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	-	10	-	20	µA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

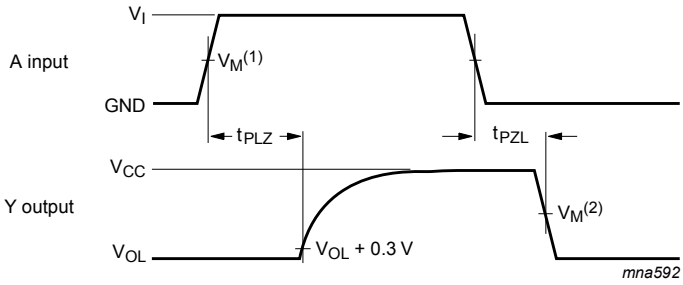
Table 8. Dynamic characteristics

GND = 0 V; $t_r = t_f$ = ≤ 3.0 ns. For test circuit see Fig. 6.

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PZL}	OFF-state to LOW propagation delay	A to Y; see Fig. 5									
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[1]	-	3.5	5.6	1.0	6.3	1.0	7.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	[1]	-	5.0	8.0	1.0	9.0	1.0	10.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[2]	-	2.5	3.9	1.0	4.6	1.0	4.9	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[2]	-	3.6	5.5	1.0	6.5	1.0	7.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	A to Y; see Fig. 5									
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[1]	-	5.8	7.9	1.0	8.4	1.0	8.9	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	[1]	-	8.3	11.5	1.0	12.0	1.0	12.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[2]	-	4.2	5.1	1.0	5.6	1.0	6.1	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[2]	-	6.0	7.5	1.0	8.0	1.0	8.5	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[3]	-	5	-	-	-	-	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V.
[2] Typical values are measured at V_{CC} = 5.0 V.
[3] C_{PD} is used to determine the dynamic power dissipation P_D (µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts

11.1. Waveforms and test circuit

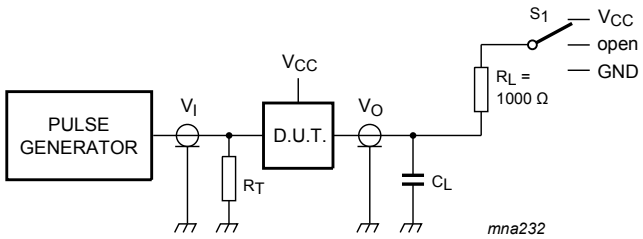


Measurement points are given in Table 9.

Fig. 5. Input (A) to output (Y) propagation delays

Table 9. Measurement point

Input		Output
V_I	$V_M^{(1)}$	$V_M^{(2)}$
GND to V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 8.

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

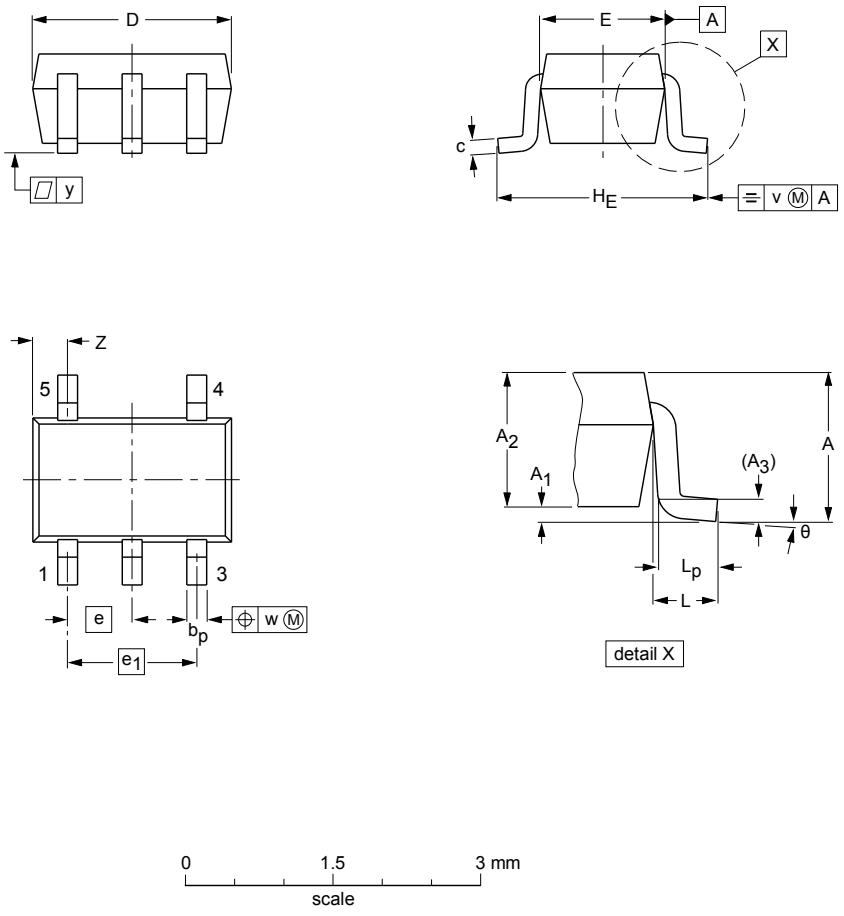
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

For t_{PLZ}, t_{PZL}, S_1 = V_{CC}

Fig. 6. Test circuit for measuring switching times

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

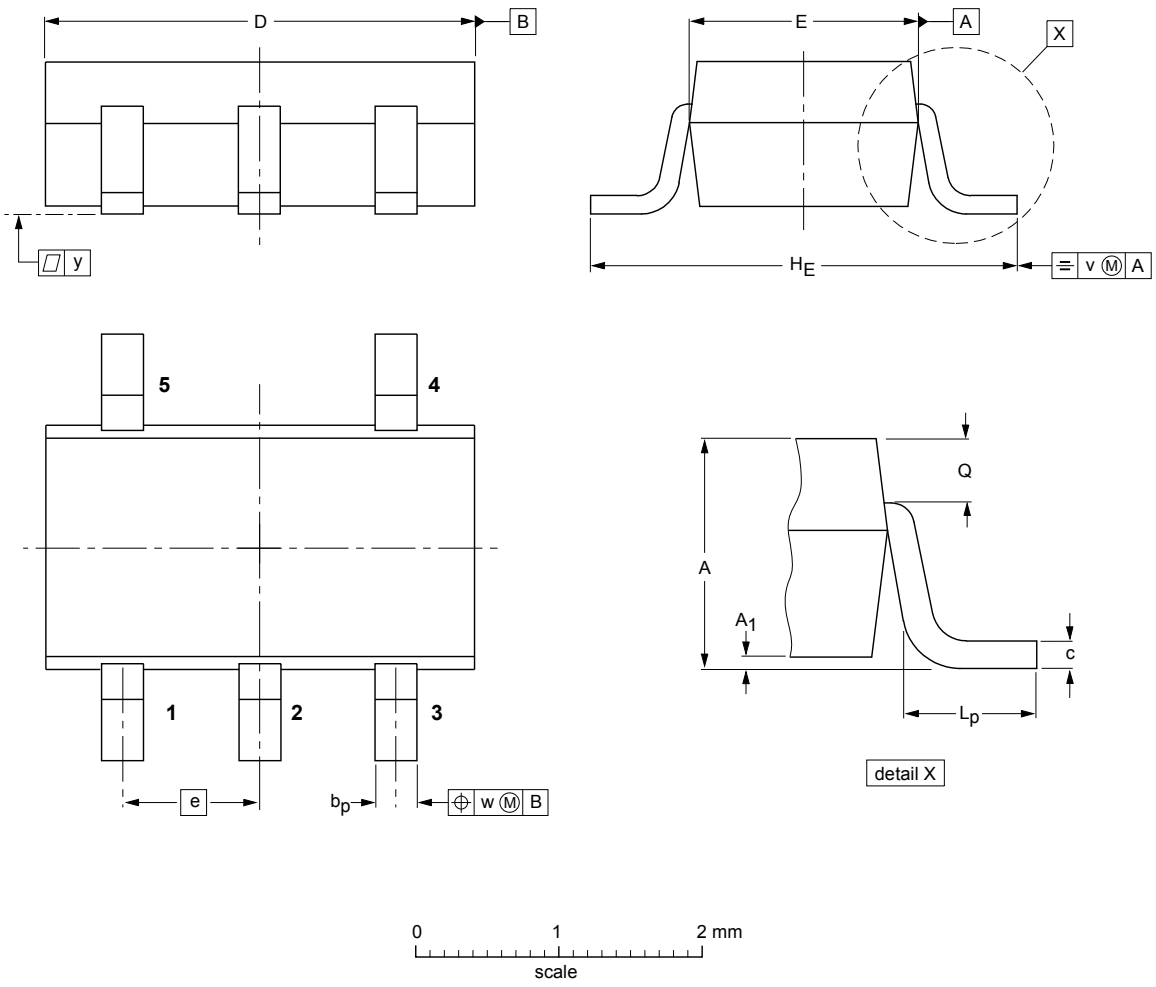
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~00-09-01~~ 03-02-19

Fig. 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 8. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC1G07 v.8	20190225	Product data sheet	-	74AHC_AHCT1G07 v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74AHCT1G07GW (SOT353-1) and 74AHCT1G07GV (SOT753) removed.			
74AHC_AHCT1G07 v.7	20141118	Product data sheet	-	74AHC_AHCT1G07 v.6
Modifications:	• Section 4: table note added.			
74AHC_AHCT1G07 v.6	20070607	Product data sheet	-	74AHC_AHCT1G07 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package SOT353 changed to SOT353-1 in Section 3 and Section 12. • Quick reference data and Soldering sections removed.			
74AHC_AHCT1G07 v.5	20021002	Product specification	-	74AHC_AHCT1G07 v.4
74AHC_AHCT1G07 v.4	20020606	Product specification	-	74AHC_AHCT1G07 v.3
74AHC_AHCT1G07 v.3	20020221	Product specification	-	74AHC_AHCT1G07 v.2
74AHC_AHCT1G07 v.2	20010209	Product specification	-	74AHC_AHCT1G07 v.1
74AHC_AHCT1G07 v.1	20000502	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 25 February 2019