

Single Channel Low power Comparator

FEATURES ($V^+ = 5V, V^- = 0V, T_a = 25^\circ C$)

- Guaranteed Temperature: $-40^\circ C$ to $+125^\circ C$
- Input Offset Voltage: 3mV max.
- Supply Current: 0.5mA max.
- Operating Voltage: $+2V$ to $+36V$ or $\pm 1V$ to $\pm 18V$
- Integrated EMI filter
- Low-level Output Voltage: 80mV typ. ($I_{sink} = 4mA$)
- Response Time: 1.3 μs typ.
- Open Collector Output
- GND sensing
- Internal ESD protection: Human Body Model $\pm 2000V$ typ.
- Package:
 - NJM8190: SOT-23-5, SC-88A
 - NJM8191: SOT-23-5, SC-88A, DFN6-G1 (ESON6-G1)

GENERAL DESCRIPTION

The NJM8190/NJM8191 are single comparators designed specifically to operate wide range of supply voltage and temperature.

These comparators featured low input offset voltage of 3mV max. low supply current of 0.5mA max. DC characteristics are also 100% tested and guaranteed from -40 to $125^\circ C$.

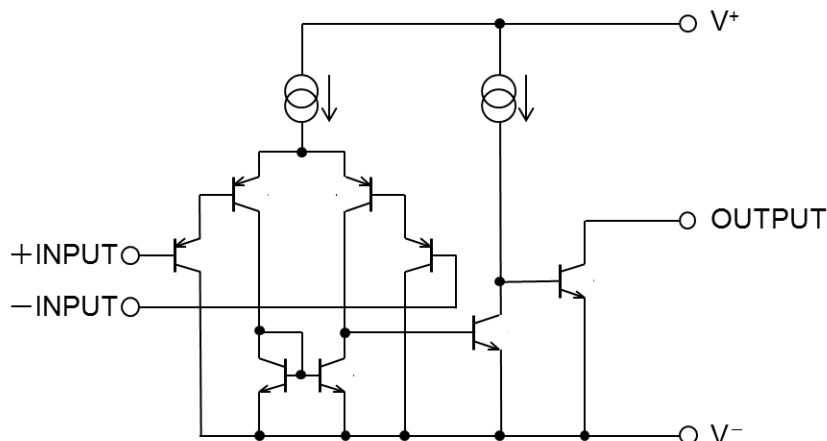
The NJM8190/NJM8191 are available in DFN6-G1(1616) of small size Package, significantly reducing the required portable application's board area.

PIN CONFIGURATION

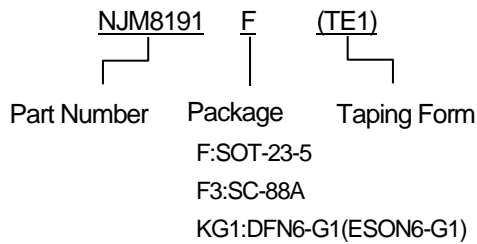
Parts Number	NJM8190F	NJM8190F3	NJM8191F	NJM8191F3	NJM8191KG1
Package Outline	SOT-23-5	SC-88A	SOT-23-5	SC-88A	DFN6-G1(*)
Pin Function	<p>(Top View) Pin 1: OUTPUT Pin 2: V^- Pin 3: -INPUT Pin 4: +INPUT Pin 5: V^+</p>	<p>(Top View) Pin 1: -INPUT Pin 2: V^- Pin 3: +INPUT Pin 4: OUTPUT Pin 5: V^+</p>	<p>(Top View) Pin 1: -INPUT Pin 2: V^- Pin 3: +INPUT Pin 4: OUTPUT Pin 5: V^+</p>	<p>(Top View) Pin 1: V^+ Pin 2: N.C. Pin 3: OUTPUT Pin 4: +INPUT Pin 5: -INPUT Pin 6: V^-</p>	<p>(Top View) Pin 1: V^+ Pin 2: N.C. Pin 3: OUTPUT Pin 4: +INPUT Pin 5: -INPUT Pin 6: V^-</p>

(*)Connect to exposed pad to V^-

EQUIVALENT CIRCUIT



■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJM8190F	SOT-23-5	yes	yes	Sn2Bi	A5V	15	3,000
NJM8190F3	SC-88A	yes	yes	Sn2Bi	2A	7.5	3,000
NJM8191F	SOT-23-5	yes	yes	Sn2Bi	A5U	15	3,000
NJM8191F3	SC-88A	yes	yes	Sn2Bi	29	7.5	3,000
NJM8191KG1	DFN6-G1	yes	yes	Sn2Bi	8191	3.5	3,000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+ - V^-$	36	V
Differential Input Voltage	V_{ID}	± 36	V
Input Voltage ⁽¹⁾	V_{IN}	$V^- - 0.3$ to $V^+ + 36$	V
Output Terminal Input Voltage ⁽²⁾	V_o	$V^- - 0.3$ to $V^+ + 36$	V
Short-Circuit Output Current to V^+ ⁽³⁾		Infinite	
Power Dissipation($T_a=25^\circ\text{C}$)	P_D	(2-layer / 4-layer)	mW
SOT-23-5 ⁽⁴⁾		480 / 650	
SC-88A ⁽⁴⁾		360 / 490	
DFN6-G1(ESON6-G1) ⁽⁵⁾		330 / 1200	
Junction Temperature	T_{jmax}	+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 55 to +150	$^\circ\text{C}$

(1) Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V^+ .

(2) Output voltage is the voltage should be allowed to apply to the output terminal independent of the magnitude of V^+ .

(3) Short-circuits from the output to V^+ can cause excessive heating and potential destruction.

(4) Short-circuit can cause excessive heating and destructive dissipation. Values are typical.

(5) Mounted on glass epoxy board. (76.2x114.3x1.6mm:based on EIA/JDEC standard, 2Layers FR4)

Mounted on glass epoxy board. (76.2x114.3x1.6mm:based on EIA/JDEC standard, 4Layers FR4), internal Cu area: 74.2 x 74.2mm

(6) Mounted on glass epoxy board. (101.5x114.5x1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

Mounted on glass epoxy board. (101.5x114.5x1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

*For 4Layers: Applying 99.5x99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient thermal resistance SOT-23-5 ⁽⁷⁾ SC-88A ⁽⁷⁾ DFN6-G1(ESON6-G1) ⁽⁸⁾	θ_{ja}	(2-layer / 4-layer) 260 / 195 355 / 260 385 / 110	$^{\circ}\text{C/W}$
Junction-to-Top of package characterization parameter SOT-23-5 ⁽⁷⁾ SC-88A ⁽⁷⁾ DFN6-G1(ESON6-G1) ⁽⁸⁾	ψ_{jt}	(2-layer / 4-layer) 68 / 58 91 / 74 65 / 26	$^{\circ}\text{C/W}$

(7) Mounted on glass epoxy board. (76.2x114.3x1.6mm:based on EIA/JDEC standard, 2Layers FR4)

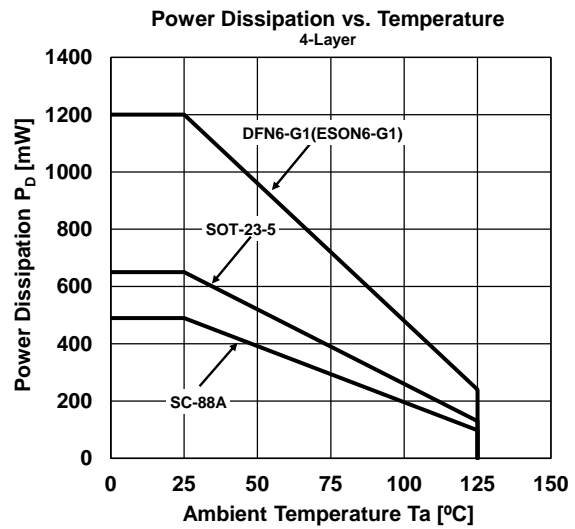
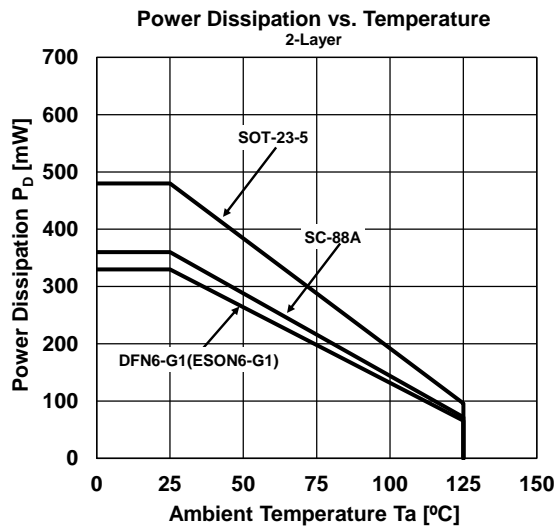
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*For 4Layers: Applying 99.5x99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+ - V$	2 to 36	V
Operating Ambient Temperature	T_{opr}	- 40 to +125	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $V^+=5V$, $V=0V$, $R_L=OPEN$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP.	MAX.	UNIT
Input Offset Voltage ⁽¹⁾	V_{IO}	$T_a=25^\circ C$	—	0.5	3	mV
		$T_a=-40^\circ C$ to $125^\circ C$	—	—	4	mV
Input Offset Current	I_{IO}	$T_a=25^\circ C$	—	0.5	50	nA
		$T_a=-40^\circ C$ to $125^\circ C$	—	—	150	
Input Bias Current ⁽²⁾	I_B	$T_a=25^\circ C$	—	20	250	
		$T_a=-40^\circ C$ to $125^\circ C$	—	—	400	
Common Mode Input Voltage	V_{ICM}	$V^+=30V$, $T_a=25^\circ C$	0	—	$V^+-1.5$	V
		$V^+=30V$, $T_a=-40$ to $125^\circ C$	0	—	$V^+-2.0$	
Open-Loop Voltage Gain	A_V	$V^+=15V$, $R_L=15k\Omega$, $V_o=1V$ to $11V$	50	200	-	V/mV
Supply Current	I_{SUPPLY}	$T_a=25^\circ C$	—	0.3	0.5	mA
		$T_a=-40$ to $125^\circ C$	—	—	0.9	
		$V^+=30V$, $T_a=25^\circ C$	—	0.4	1.2	
		$V^+=30V$, $T_a=-40$ to $125^\circ C$	—	—	1.5	
Differential Input Voltage Range ⁽³⁾	V_{ID}		—	—	V^+	V
Low-level Output Voltage	V_{OL}	$V_{IN^+}=0V$, $V_{IN^-}=1V$, $I_{SINK}=4mA$, $T_a=25^\circ C$	—	80	400	mV
		$V_{IN^+}=0V$, $V_{IN^-}=1V$, $I_{SINK}=4mA$, $T_a=-40$ to $125^\circ C$	—	—	700	
Output Sink Current	I_{SINK}	$V_{IN^+}=0V$, $V_{IN^-}=1V$, $V_o=1.5V$	6	16	—	mA
Output Leakage Current	I_{LEAK}	$V^+=V_o=30V$, $V_{IN^+}=1V$, $V_{IN^-}=0V$, $T_a=25^\circ C$	—	0.1	—	nA
		$V^+=V_o=30V$, $V_{IN^+}=1V$, $V_{IN^-}=0V$, $T_a=-40$ to $125^\circ C$	—	—	1	μA
Response Time ⁽⁴⁾	t_{re}	$R_L=5.1k\Omega$ to V^+	—	1.3	—	μs
Large Signal Response Time	t_{RL}	$R_L=5.1k\Omega$ to V^+ $V_{ref}=1.4V$, TTL input	—	250	—	ns

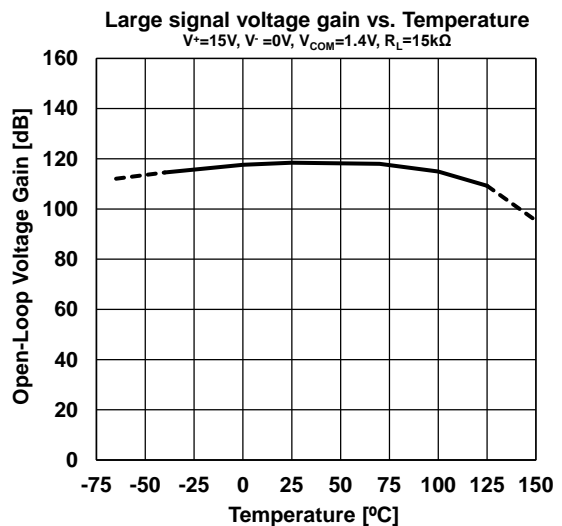
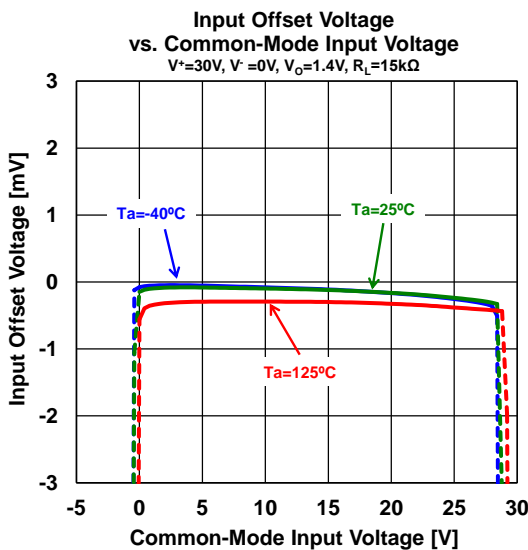
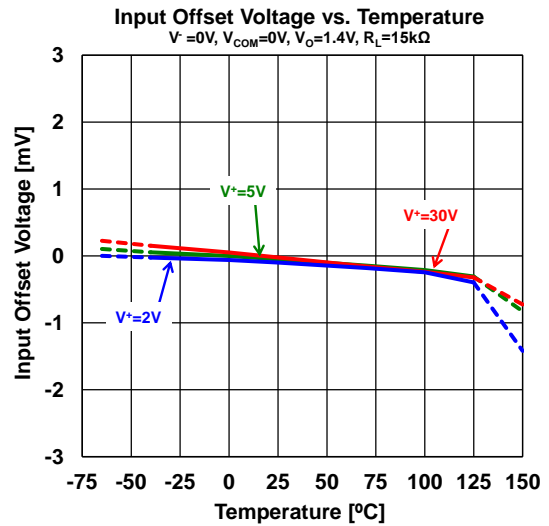
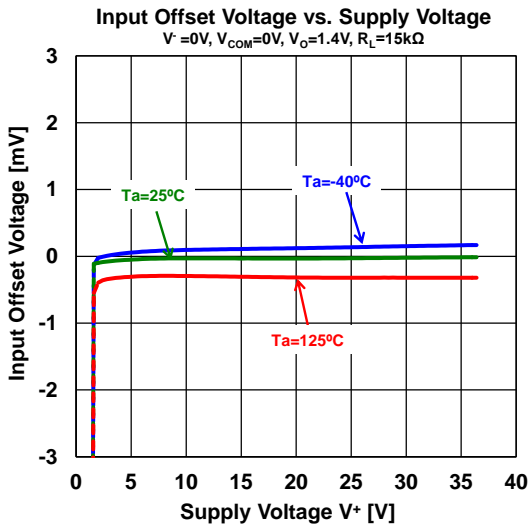
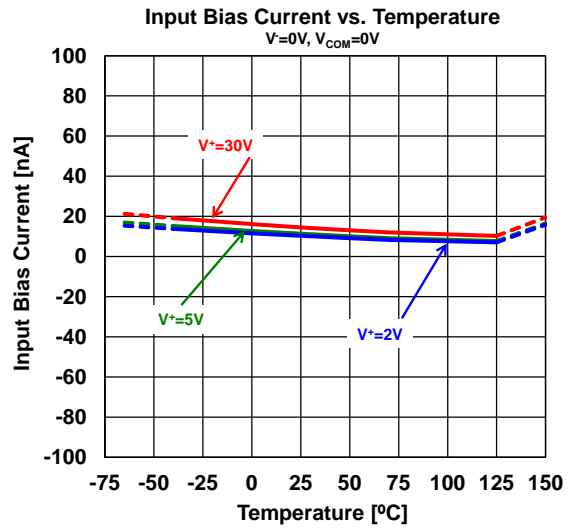
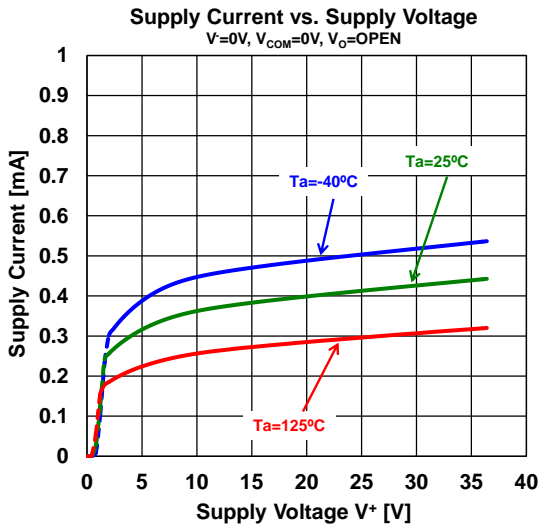
(1) $V_o=1.4V$, $R_s=0\Omega$, $5V < V^+ < 30V$, $0 < V_{ICM} < (V^+ - 1.5V)$.

(2) The direction of the input current is out of the IC due to the PNP input stage.

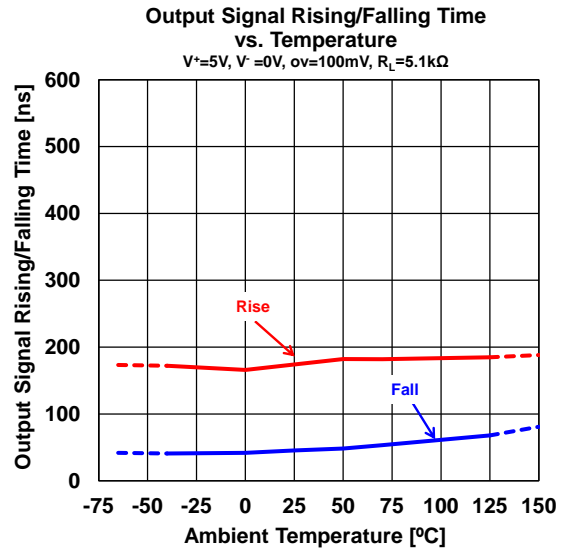
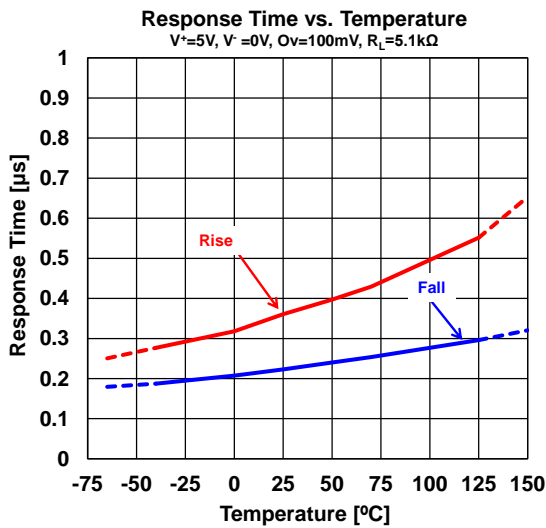
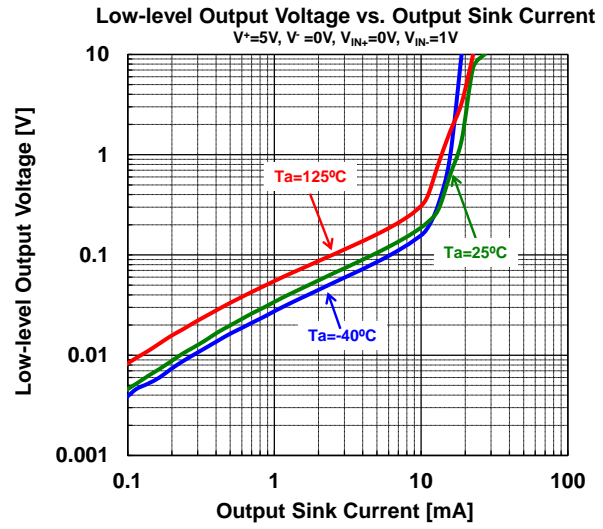
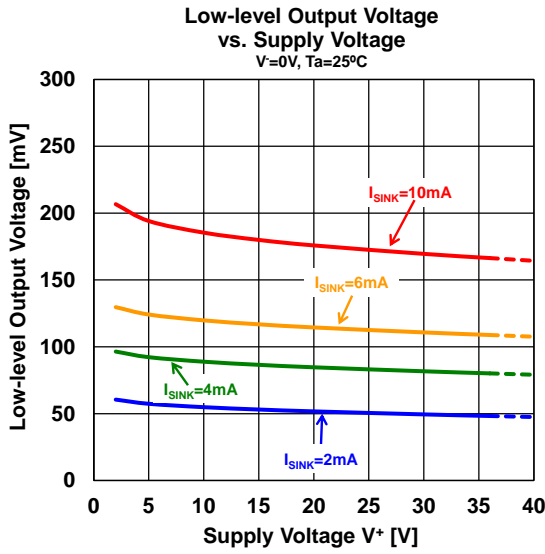
(3) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage must not be less than $-0.3V$ (or $0.3V$ below the negative power supply, if used).

(4) The response time specified is for a $100mV$ input step with $5mV$ overdrive.

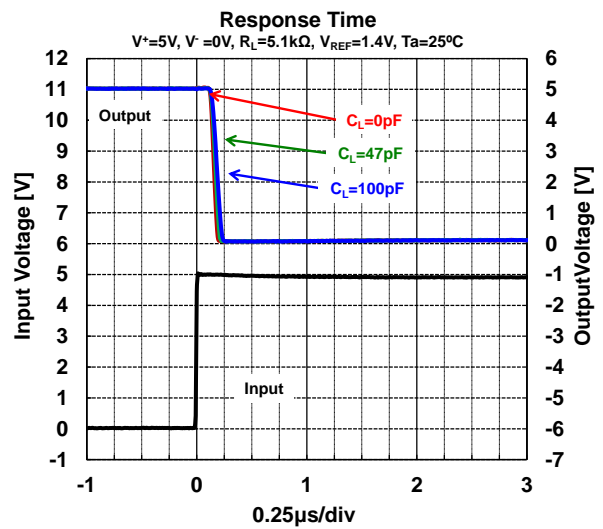
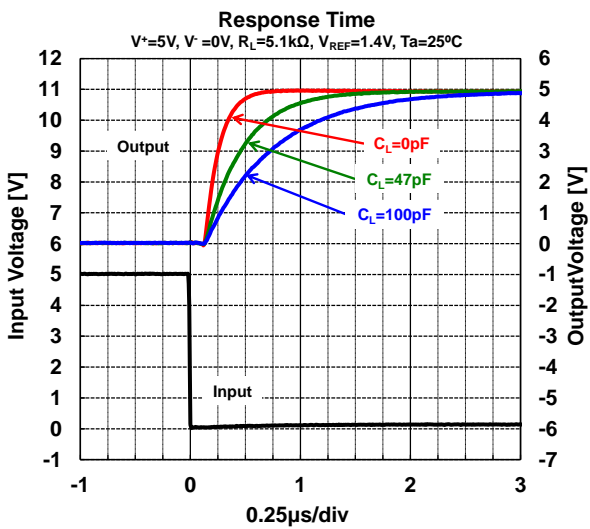
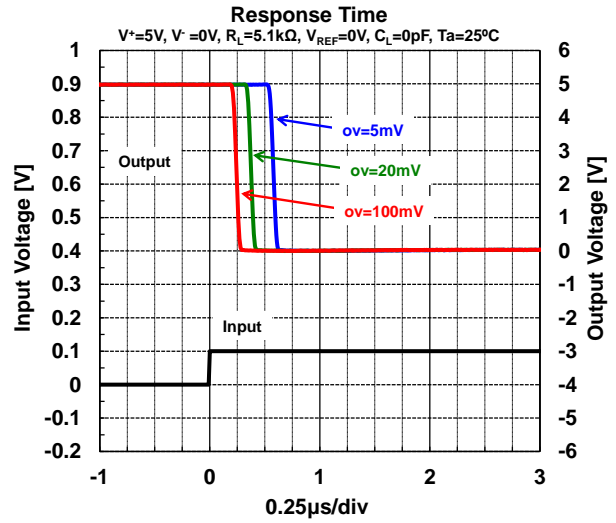
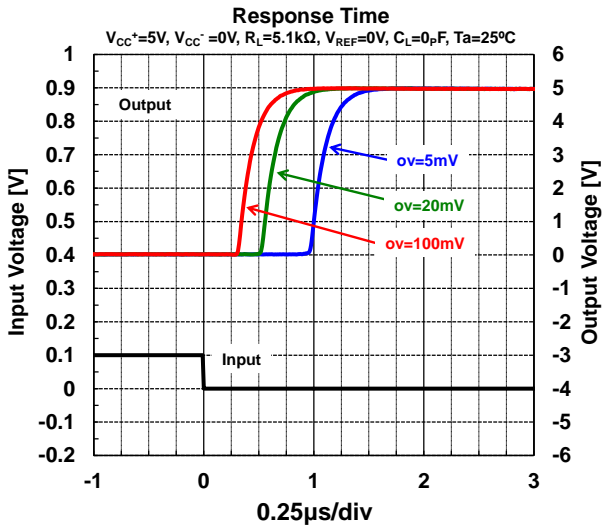
■ TYPICAL CHARACTERISTICS



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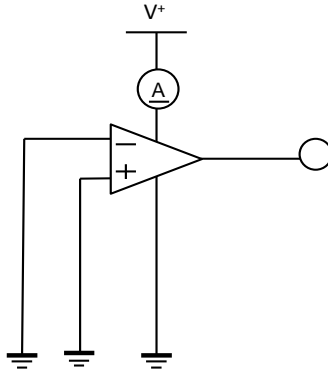
■ TYPICAL CHARACTERISTICS



■ TYPICAL TEST CIRCUIT

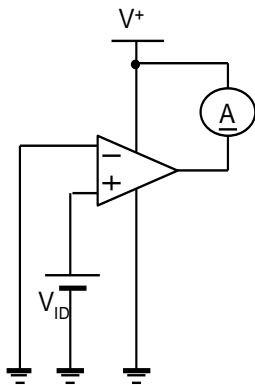
● Supply Current (I_{SUPPLY})

- $V^+ = 5V, V^- = 0V, T_a = 25^\circ C, -40$ to $125^\circ C$
- $V^+ = 30V, V^- = 0V, T_a = 25^\circ C, -40$ to $125^\circ C$



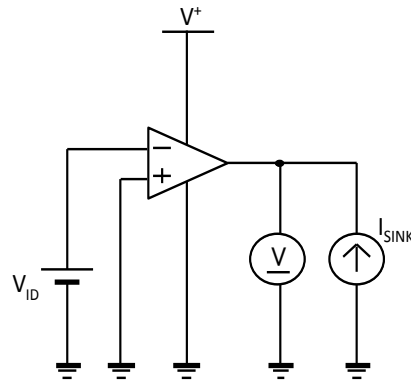
● Output Leakage Current (I_{LEAK})

- $V^+ = 30V, V^- = 0V, V_{IN+} = 1V, V_{IN-} = 0V, T_a = 25^\circ C, -40$ to $125^\circ C$



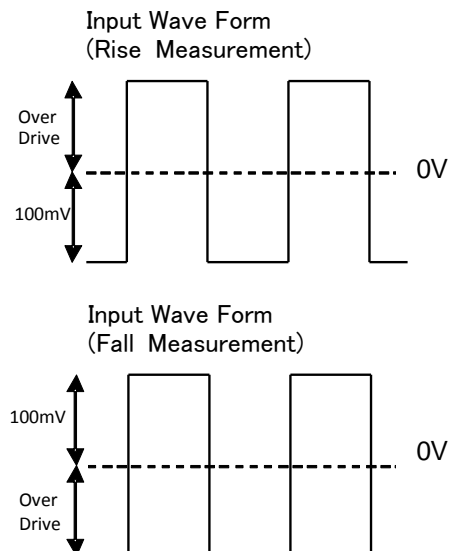
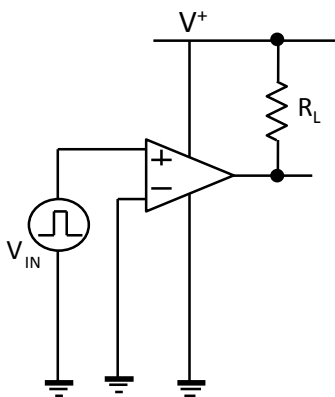
● Low-level Output Voltage (V_{OL})

- $V^+ = 5V, V^- = 0V, V_{IN+} = 0V, V_{IN-} = 1V, I_{SINK} = 4mA, T_a = 25^\circ C, -40$ to $125^\circ C$



● Response Time (t_{re})

- $V^+ = 5V, V^- = 0V, R_L = 5.1k\Omega$



■APPLICATION NOTE

EMIRR(EMI Rejection Ratio) Definition

EMIRR is a parameter indicating the EMI robustness of an comparator. The definition of EMIRR is given by the following a formula (1). We can grasp the tolerance of the RF signal by measuring an RF signal and offset voltage shift quantity.

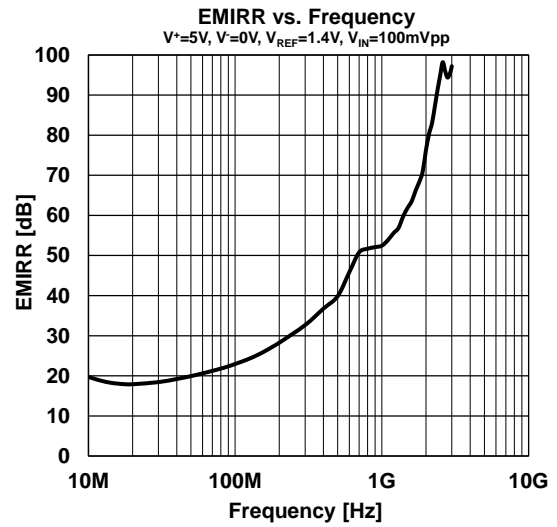
$$EMIRR = 20 \cdot \log \left(\frac{V_{RF_PEAK}}{|\Delta V_{IO}|} \right) \quad \dots(1)$$

V_{RF_PEAK} : RF Signal Amplitude [V_p]

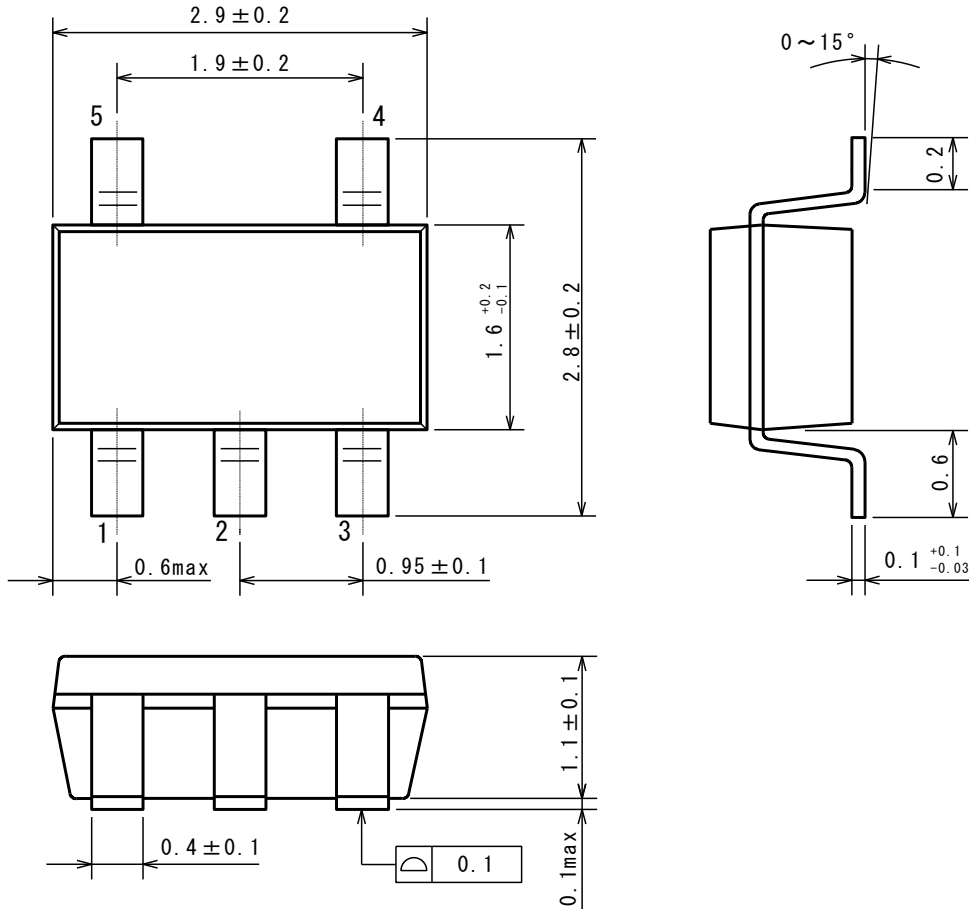
ΔV_{IO} : Input offset voltage shift quantity [V]

Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

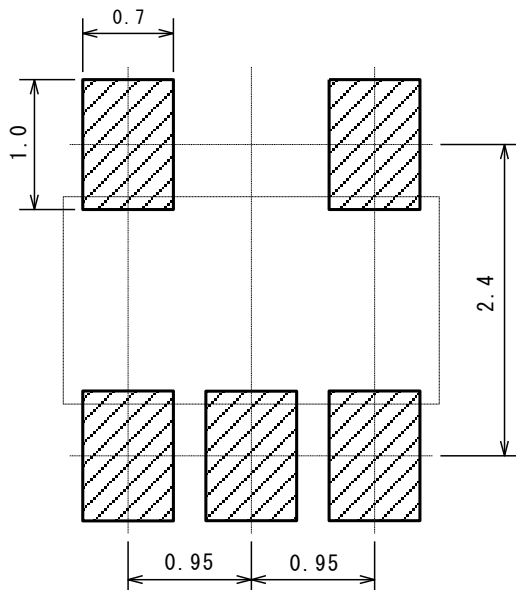
*For details, refer to " Application Note for EMI Immunity" in our HP: <http://www.njr.com/>



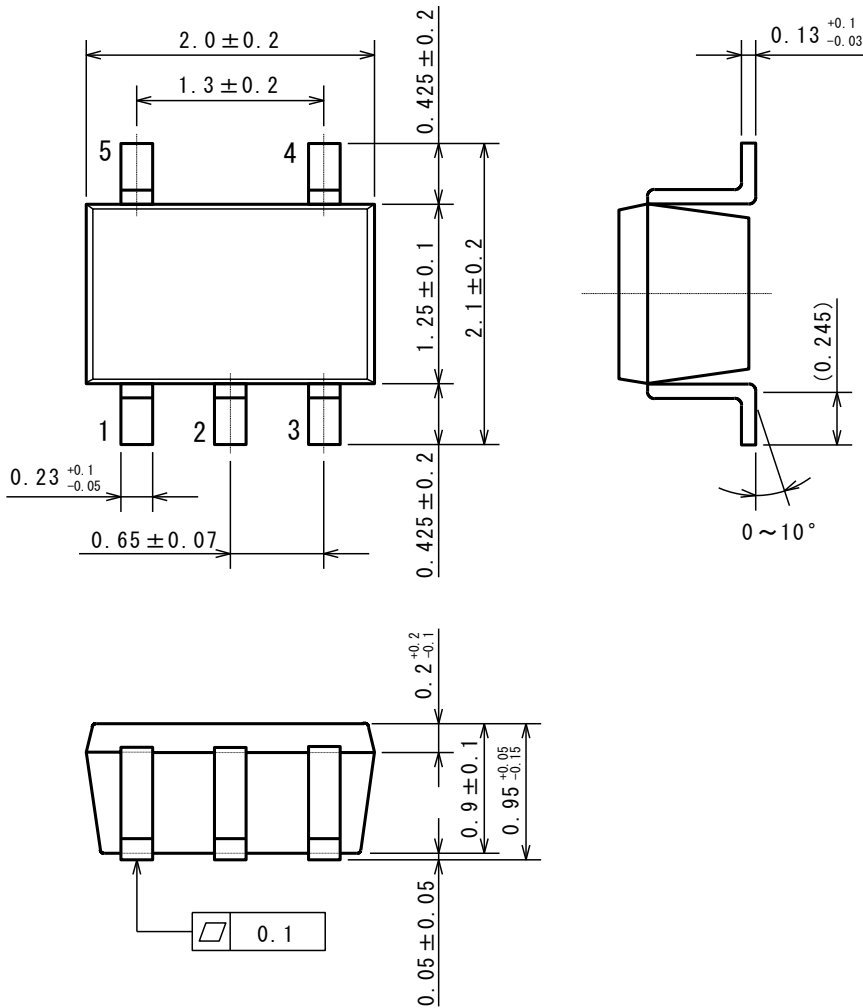
PACKAGE DIMENSIONS



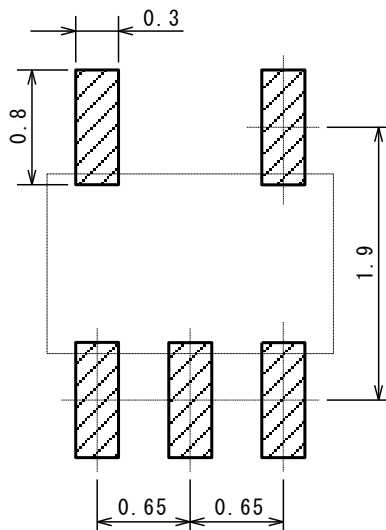
EXAMPLE OF SOLDER PADS DIMENSIONS



PACKAGE DIMENSIONS

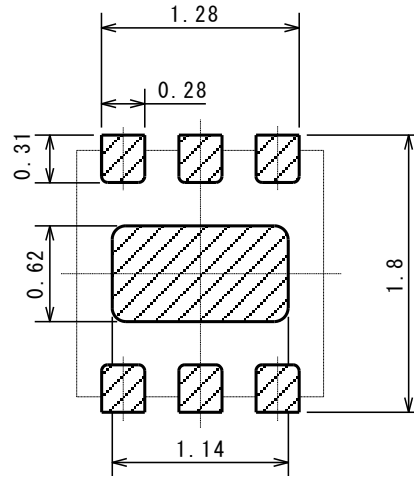
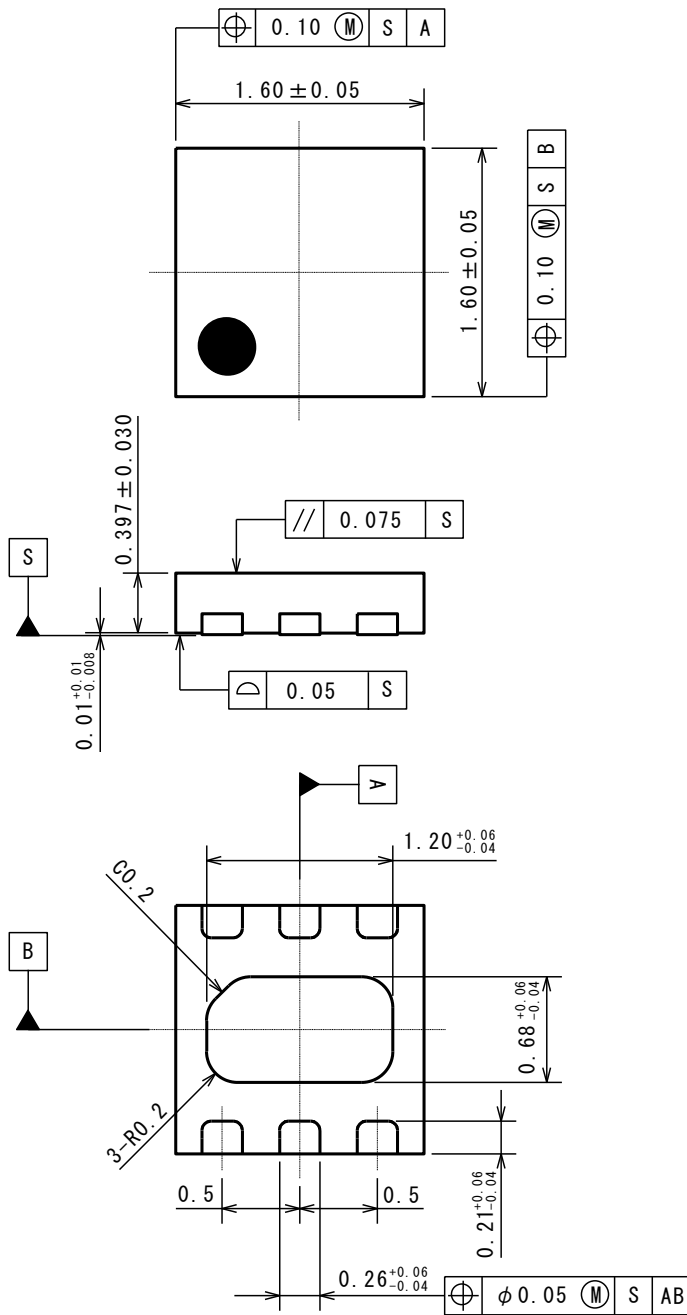


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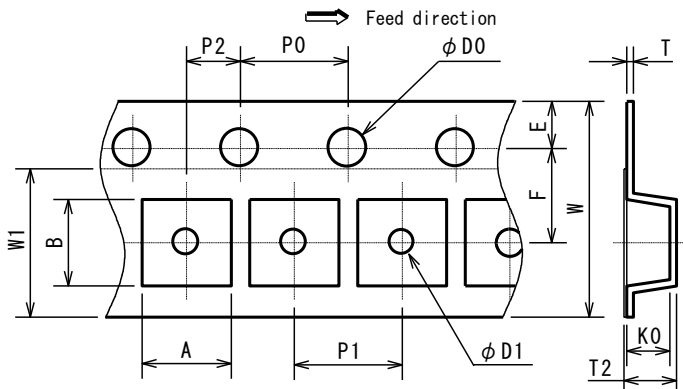
PACKAGE DIMENSIONS

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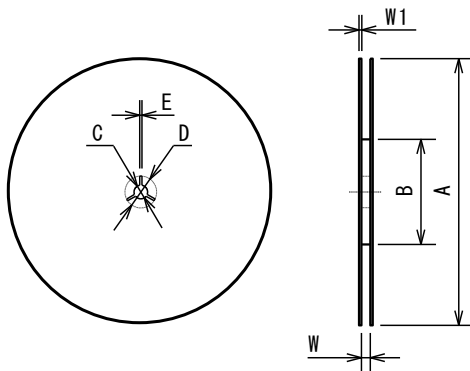
PACKING SPEC

TAPING DIMENSIONS



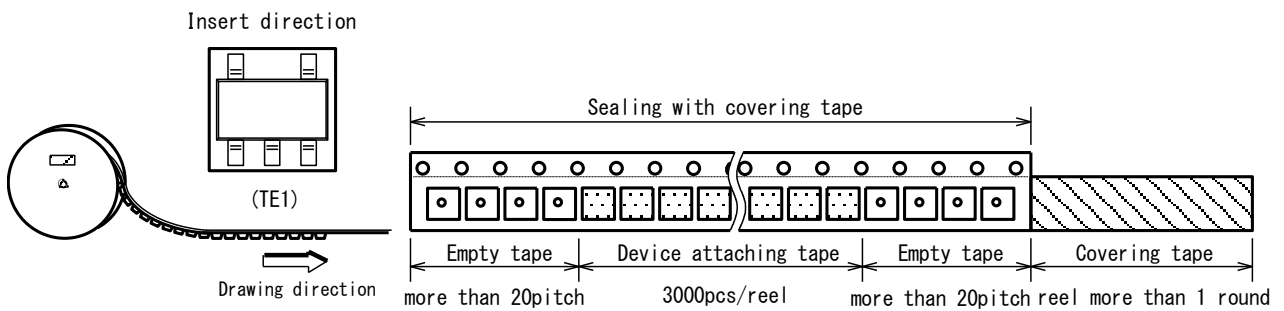
SYMBOL	DIMENSION	REMARKS
A	3.3±0.1	BOTTOM DIMENSION
B	3.2±0.1	BOTTOM DIMENSION
D0	1.55	
D1	1.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.82	
K0	1.5±0.1	
W	8.0±0.3	
W1	5.5	THICKNESS 0.1MAX

REEL DIMENSIONS

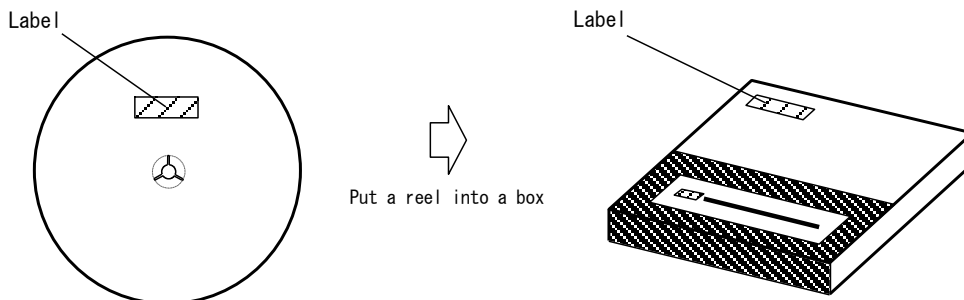


SYMBOL	DIMENSION
A	φ 180±1
B	φ 60±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9±0.5
W1	1.2±0.2

TAPING STATE

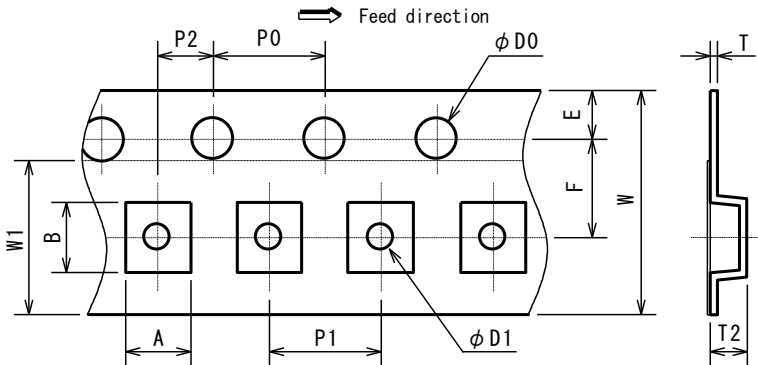


PACKING STATE



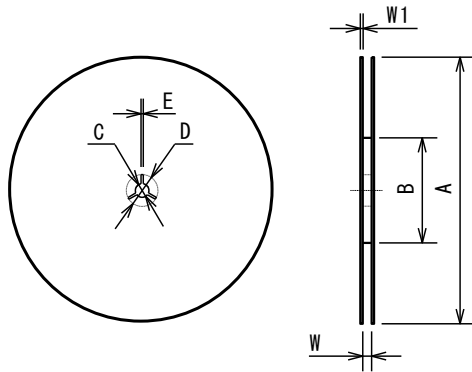
PACKING SPEC

TAPING DIMENSIONS



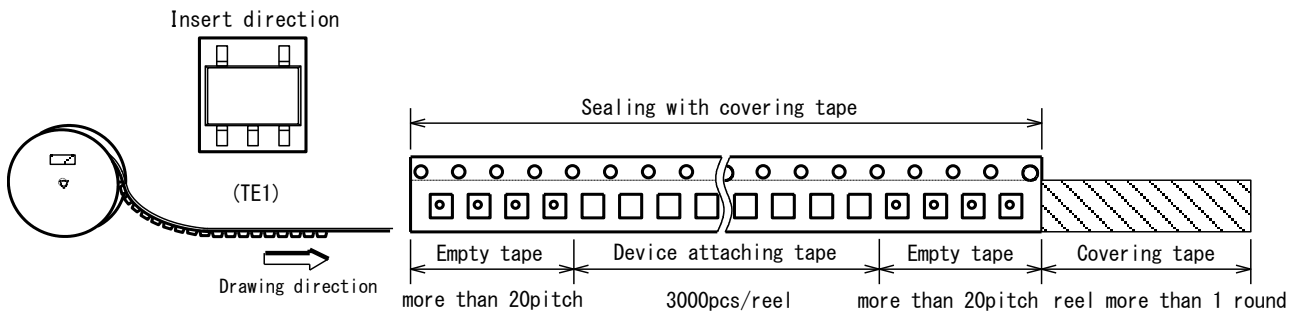
SYMBOL	DIMENSION	REMARKS
A	2.3±0.1	BOTTOM DIMENSION
B	2.5±0.1	BOTTOM DIMENSION
D0	1.55±0.05	
D1	1.05±0.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.3±0.1	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

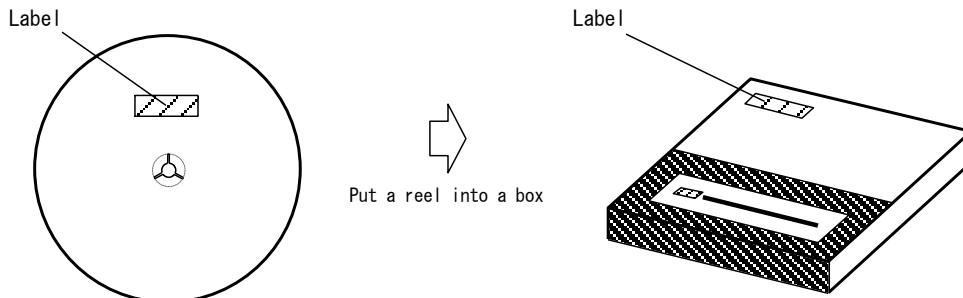


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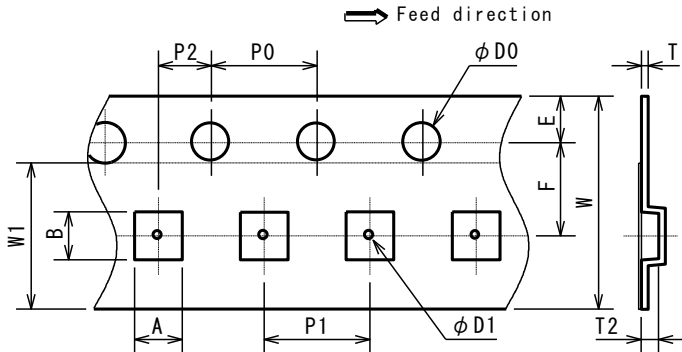


PACKING STATE



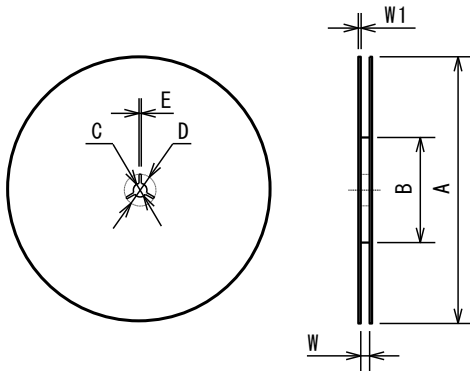
PACKING SPEC

TAPING DIMENSIONS



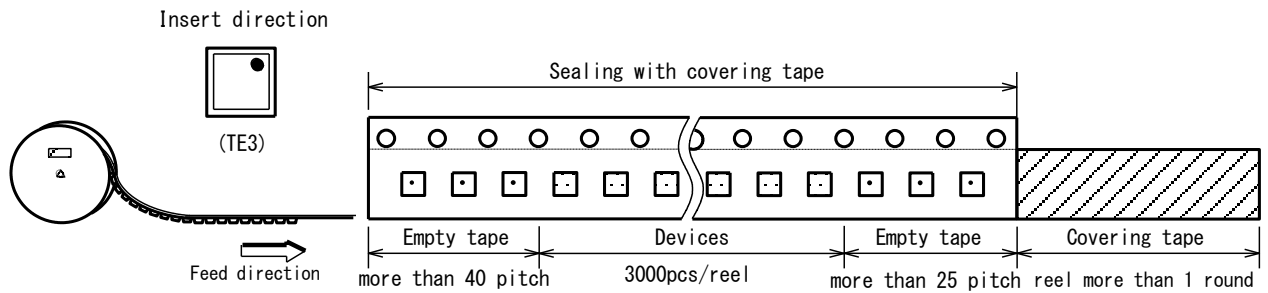
SYMBOL	DIMENSION	REMARKS
A	1.85±0.05	BOTTOM DIMENSION
B	1.85±0.05	BOTTOM DIMENSION
D0	1.5 ^{+0.1} ₀	
D1	0.5±0.1	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	0.65±0.05	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

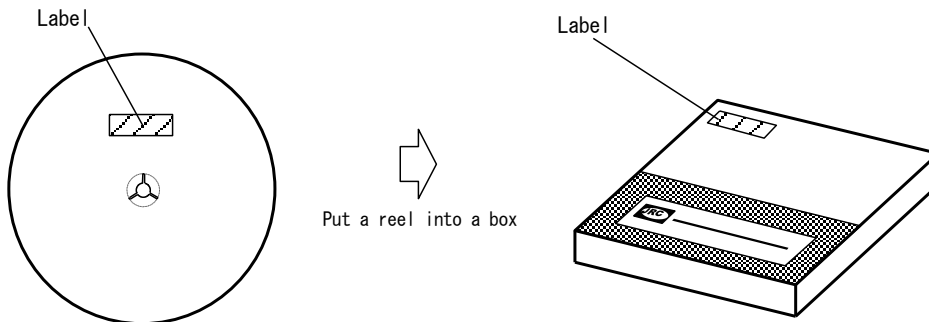


SYMBOL	DIMENSION
A	φ 180 ⁰ _{-1.5}
B	φ 60 ⁺¹ ₀
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9 ^{+0.3} ₀
W1	1.2

TAPING STATE

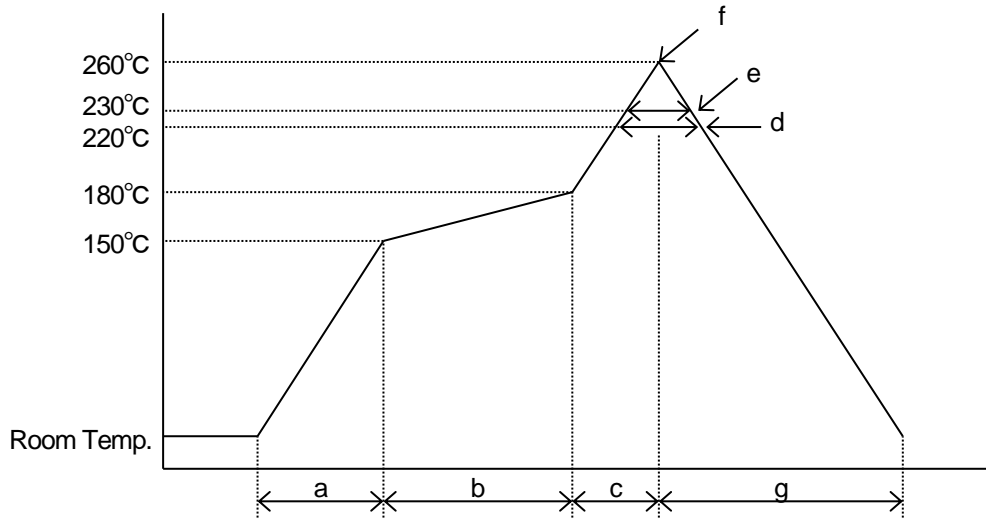


PACKING STATE



RECOMMENDED MOUNTING METHOD

*Recommended reflow soldering procedure



- a: Temperature ramping rate : 1 to 4°C/s
- b: Pre-heating temperature : 150 to 180°C
time : 60 to 120s
- c: Temperature ramp rate : 1 to 4°C/s
- d: 220°C or higher time : Shorter than 60s
- e: 230°C or higher time : Shorter than 40s
- f: Peak temperature : Lower than 260°C
- g: Temperature ramping rate : 1 to 6°C/s

*The temperature indicates at the surface of mold package.

REVISION HISTORY

Date	Revision	Changes
17.APR.2017	Ver.1.0	Initial Version

[CAUTION]

1. New JRC strives to produce reliable and high quality semiconductors. New JRC's semiconductors are intended for specific applications and require proper maintenance and handling. To enhance the performance and service of New JRC's semiconductors, the devices, machinery or equipment into which they are integrated should undergo preventative maintenance and inspection at regularly scheduled intervals. Failure to properly maintain equipment and machinery incorporating these products can result in catastrophic system failures
2. The specifications on this datasheet are only given for information without any guarantee as regards either mistakes or omissions. The application circuits in this datasheet are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.
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