



# BUK963R2-40B

## N-channel TrenchMOS logic level FET

13 March 2014

Product data sheet

### 1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 3. Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 4. Quick reference data

Table 1. Quick reference data

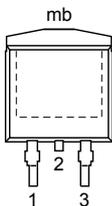
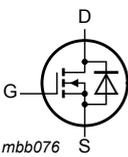
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	[1]	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>		-	-	300	W
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$		-	2.4	2.8	mΩ
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>		-	2.7	3.2	mΩ
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; V_{DS} = 32\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 13</a>		-	37	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped	-	-	1.2	J

[1] All individual parts of device must be  $\leq 175\text{ }^\circ\text{C}$  to achieve maximum current rating.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>D2PAK (SOT404)</b></p>	 <p>mbb076</p>
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK963R2-40B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK963R2-40B	BUK963R2-40B

## 8. Limiting values

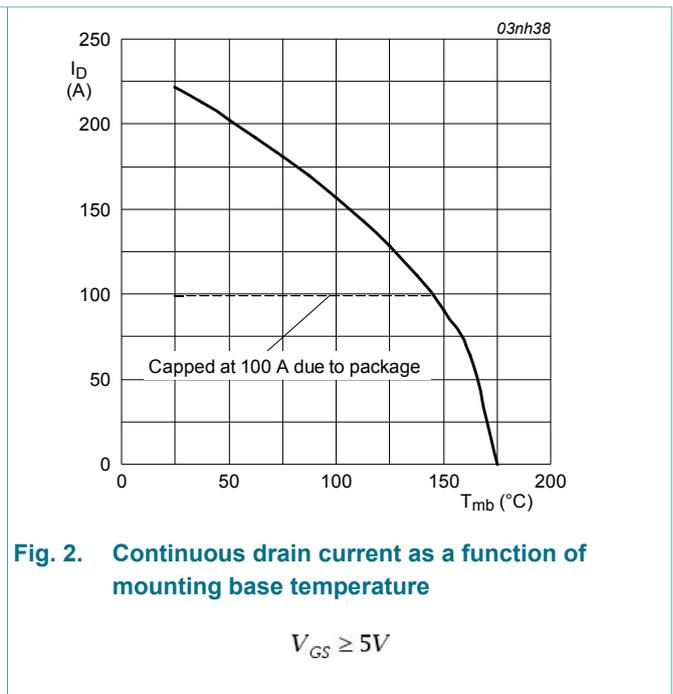
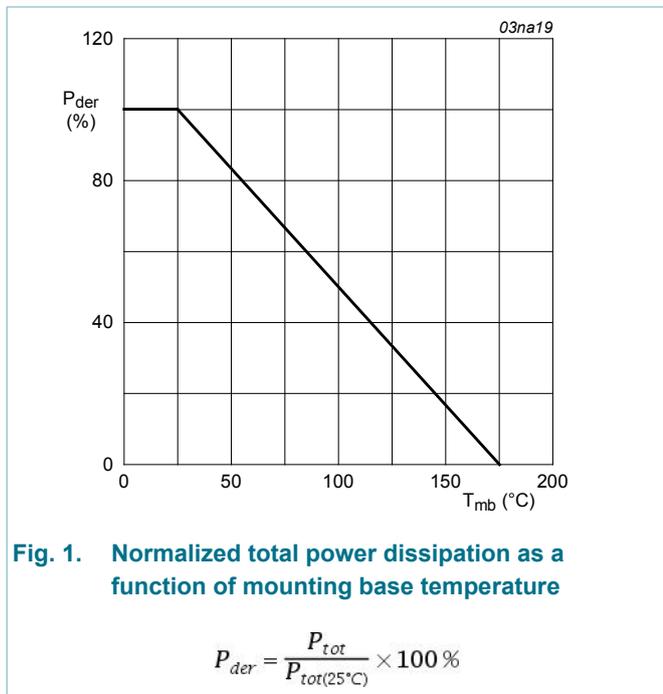
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>GS</sub>	gate-source voltage			-15	15	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	300	W
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	[1]	-	222	A
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; <a href="#">Fig. 2</a>	[2]	-	100	A
		T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	[2]	-	100	A
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; <a href="#">Fig. 3</a>		-	888	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	222	A
			[2]	-	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	888	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped		-	1.2	J

- [1] Current is limited by power dissipation chip rating.
- [2] All individual parts of device must be ≤ 175 °C to achieve maximum current rating.



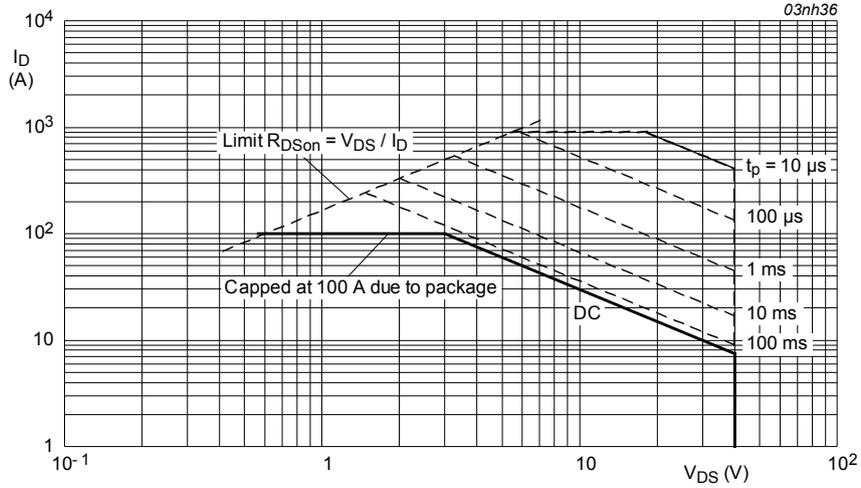


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}; I_{DM}$  is single pulse

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W

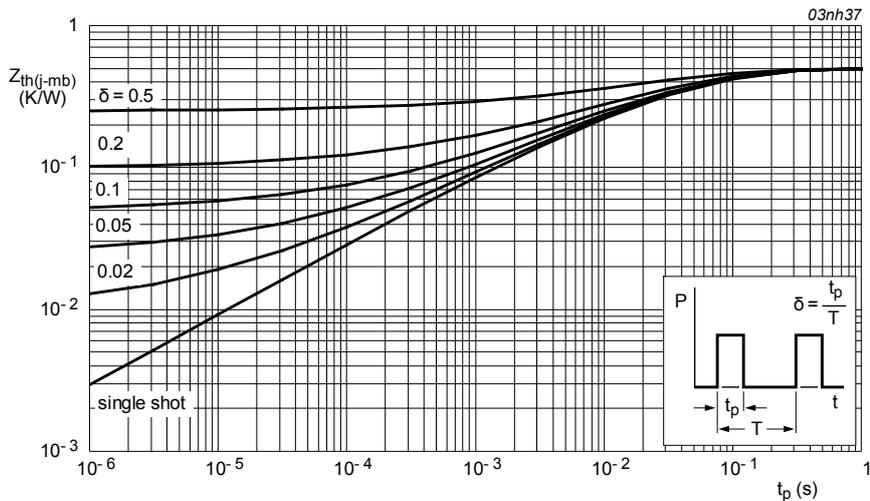


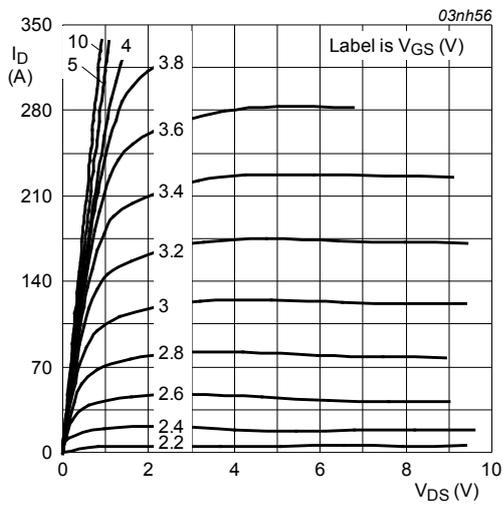
Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

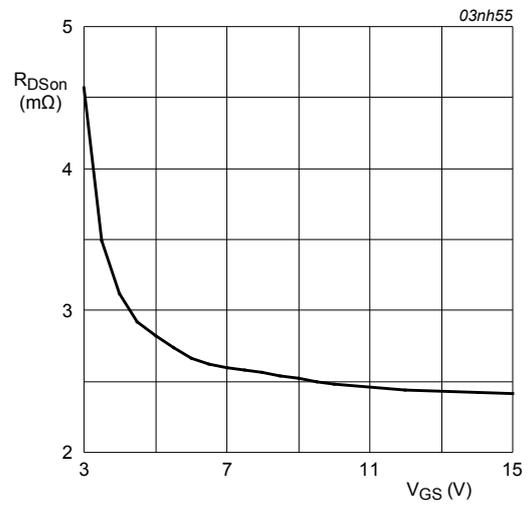
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	36	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	1.1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	-	2.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	2.4	2.8	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	3.5	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 11; Fig. 12</a>	-	-	6	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11; Fig. 12</a>	-	2.7	3.2	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13</a>	-	94	-	nC
$Q_{GS}$	gate-source charge		-	17	-	nC
$Q_{GD}$	gate-drain charge		-	37	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	-	7877	10502	pF
$C_{oss}$	output capacitance		-	1397	1676	pF
$C_{rss}$	reverse transfer capacitance		-	608	833	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ }^\Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ }^\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	68	-
$t_r$	rise time	-		268	-	ns
$t_{d(off)}$	turn-off delay time	-		257	-	ns
$t_f$	fall time	-		192	-	ns
$L_D$	internal drain inductance	from drain lead 6 mm from package to center of die; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		from upper edge of drain mounting base to center of die; $T_j = 25\text{ }^\circ\text{C}$	-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad; $T_j = 25\text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 40\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	70	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	127	-	nC



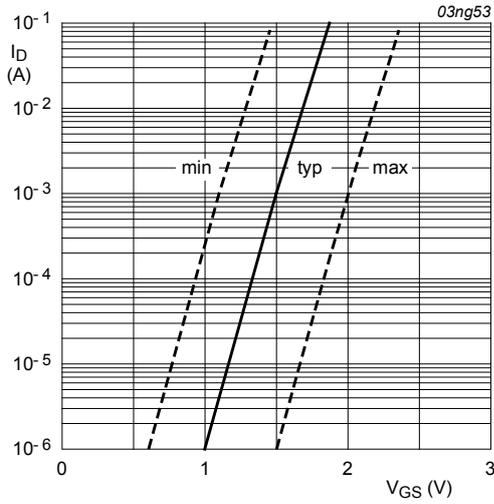
**Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values**

$T_j = 25\text{ }^\circ\text{C}$



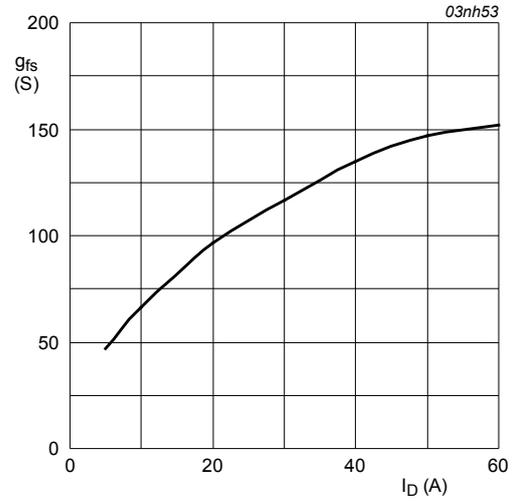
**Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$



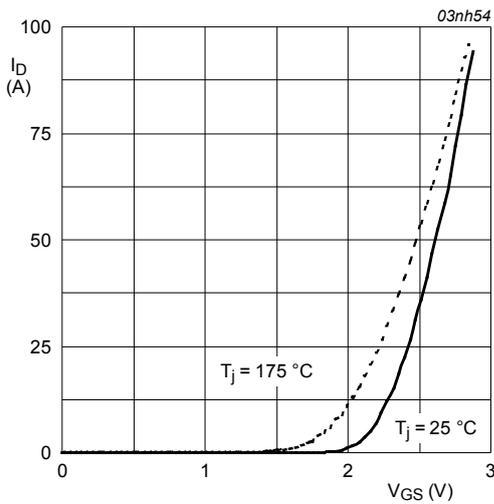
**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**

$$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$$



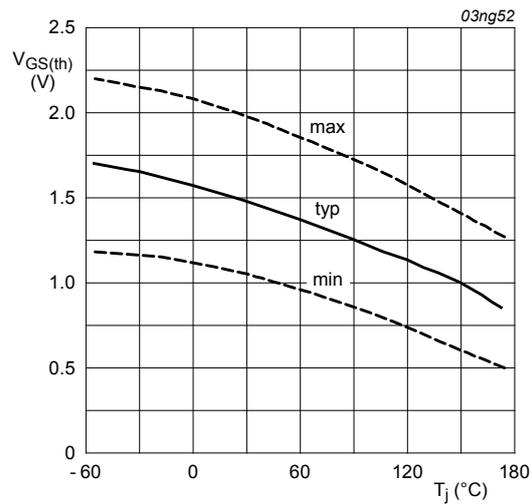
**Fig. 8. Forward transconductance as a function of drain current; typical values**

$$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$$



**Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

$$V_{DS} = 25\text{V}$$



**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

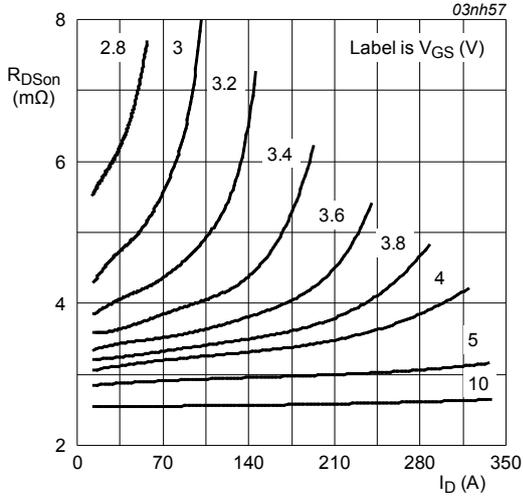


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

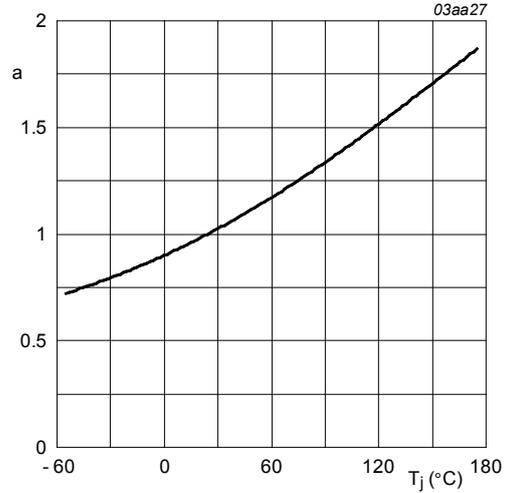


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

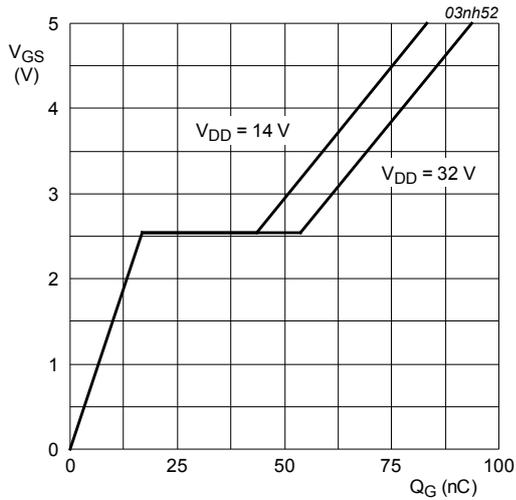


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$$

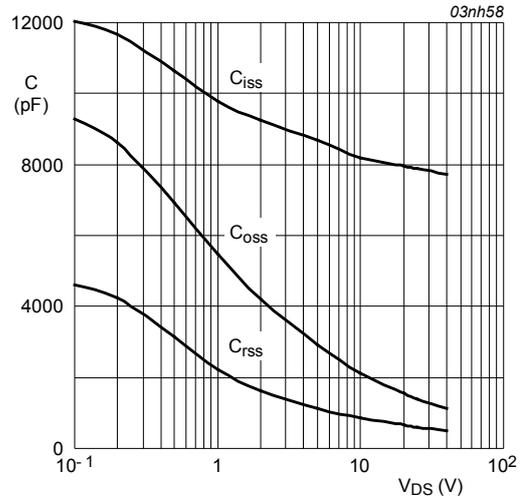
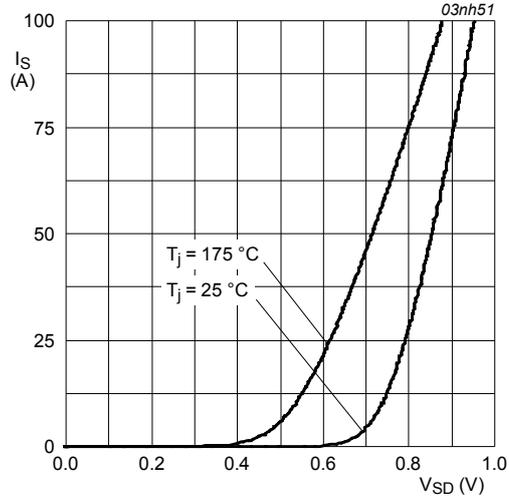


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

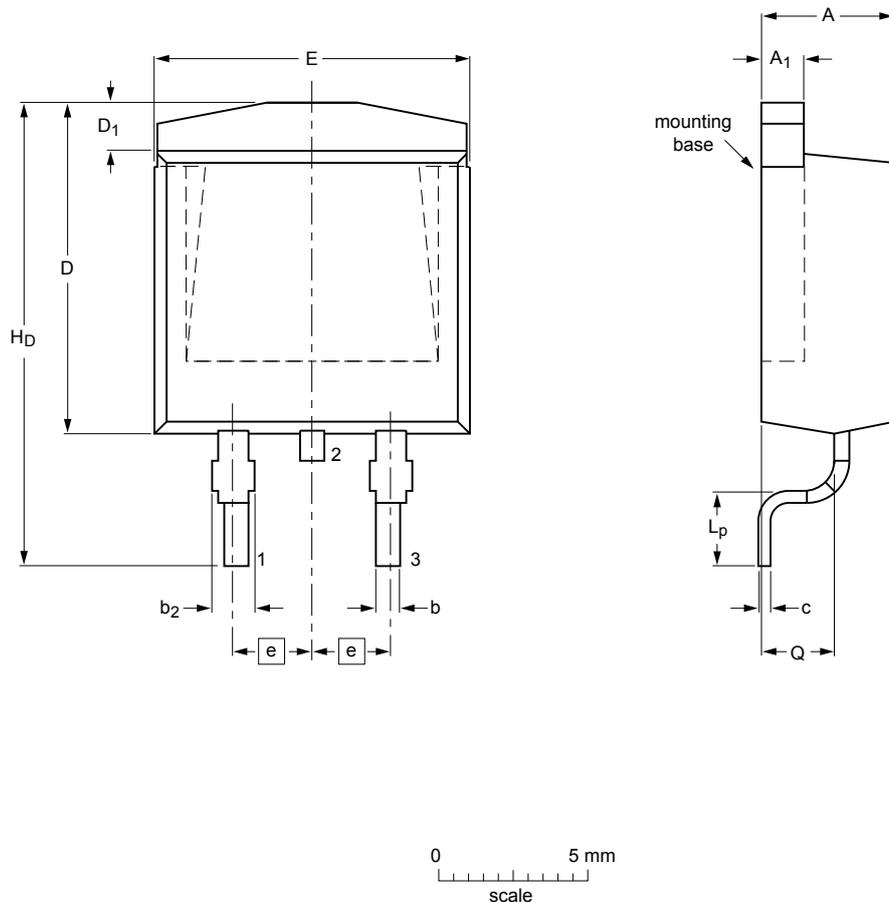


**Fig. 15. Source current as a function of source-drain voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	H <sub>D</sub>	L <sub>p</sub>	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 16. Package outline D2PAK (SOT404)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 13 March 2014