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Kind regards,

Team Nexperia

## INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC04 January 1995



Philips Semiconductors

**HEF4073B** 

gates

### **Triple 3-input AND gate**

#### DESCRIPTION

The HEF4073B provides the positive triple 3-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4073BP(N):	14-lead DIL; plastic
	(SOT27-1)
HEF4073BD(F):	14-lead DIL; ceramic (cerdip)
	(SOT73)
HEF4073BT(D):	14-lead SO; plastic
	(SOT108-1)

(): Package Designator North America



#### FAMILY DATA, I<sub>DD</sub> LIMITS category GATES

See Family Specifications

January 1995

HEF4073B

gates

## Triple 3-input AND gate

#### AC CHARACTERISTICS

 $V_{SS}$  = 0 V;  $T_{amb}$  = 25 °C;  $C_L$  = 50 pF; input transition times  $\leq$  20 ns

	V <sub>DD</sub> V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \to O_n$	5		55	110	ns	23 ns + (0,55 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>PHL</sub>	25	50	ns	14 ns + (0,23 ns/pF) C <sub>L</sub>
	15		20	40	ns	12 ns + (0,16 ns/pF) C <sub>L</sub>
	5		45	90	ns	13 ns + (0,55 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>PLH</sub>	20	40	ns	9 ns + (0,23 ns/pF) C <sub>L</sub>
	15		15	30	ns	7 ns + (0,16 ns/pF) C <sub>L</sub>
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>THL</sub>	30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>
	15		20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>
	5		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>TLH</sub>	30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>
	15		20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power	5	$600 \text{ f}_{i} + \Sigma \text{ (f}_{o}C_{L}) \times V_{DD}^{2}$	where
dissipation per	10	2700 f <sub>i</sub> + $\Sigma$ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	f <sub>i</sub> = input freq. (MHz)
package (P)	15	8400 f <sub>i</sub> + $\Sigma$ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	f <sub>o</sub> = output freq. (MHz)
			C <sub>L</sub> = load capacitance (pF)
			$\Sigma$ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs
			V <sub>DD</sub> = supply voltage (V)