

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4027B **flip-flops** Dual JK flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

Dual JK flip-flop

HEF4027B
flip-flops

DESCRIPTION

The HEF4027B is a dual JK flip-flop which is edge-triggered and features independent set direct (S_D), clear direct (C_D), clock (CP) inputs and outputs ($O, \bar{O}$). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

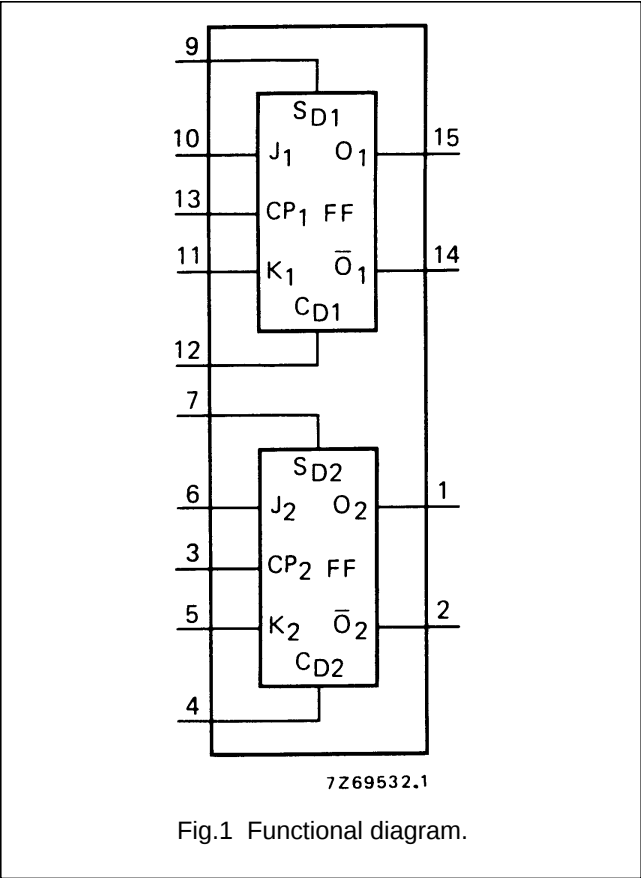


Fig.1 Functional diagram.

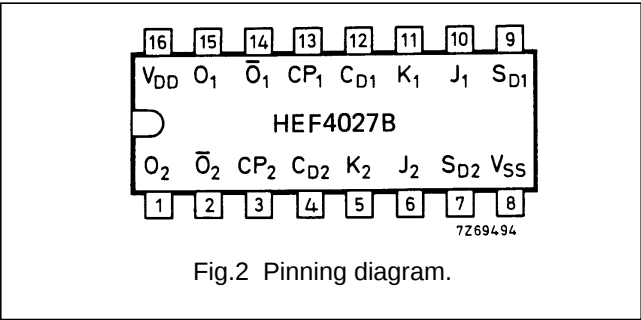


Fig.2 Pinning diagram.

FUNCTION TABLES

INPUTS					OUTPUTS	
S_D	C_D	CP	J	K	O	$\bar{O}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

INPUTS					OUTPUTS	
S_D	C_D	CP	J	K	O_{n+1}	$\bar{O}_{n+1}$
L	L	$\nearrow$	L	L	no change	
L	L	$\nearrow$	H	L	H	L
L	L	$\nearrow$	L	H	L	H
L	L	$\nearrow$	H	H	$\bar{O}_n$	O_n

Notes

- 1. H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- $\nearrow$ = positive-going transition
- O_{n+1} = state after clock positive transition

PINNING

- J,K synchronous inputs
- CP clock input (L to H edge-triggered)
- S_D asynchronous set-direct input (active HIGH)
- C_D asynchronous clear-direct input (active HIGH)
- O true output
- $\bar{O}$ complement output

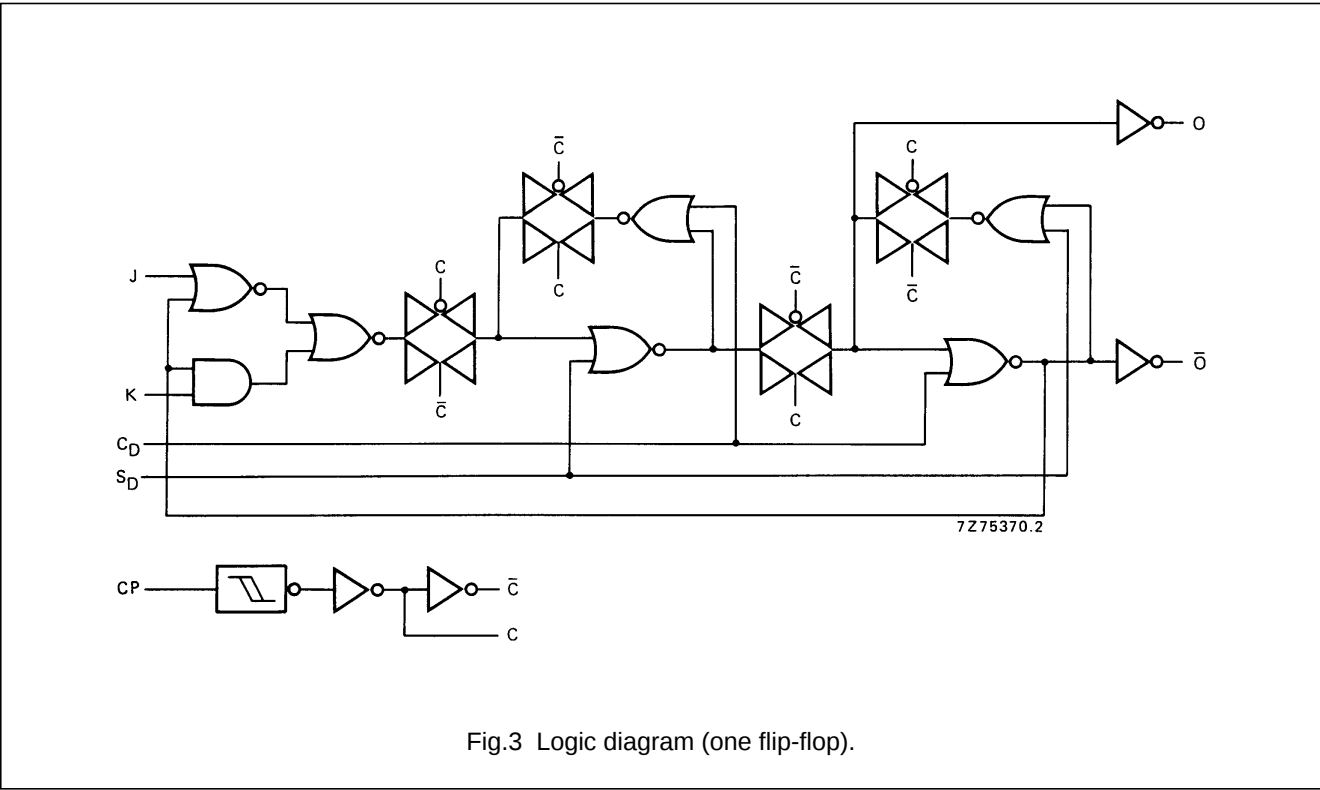
- HEF4027BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4027BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4027BT(D): 16-lead SO; plastic (SOT109-1)
- () : Package Designator North America

FAMILY DATA, I_{DD} LIMITS category FLIP-FLOPS

See Family Specifications

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AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
CP → O, $\bar{O}$	5			105	210 ns	78 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		40	80 ns	29 ns + (0,23 ns/pF) C _L
	15			30	60 ns	22 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			85	170 ns	58 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		35	70 ns	27 ns + (0,23 ns/pF) C _L
	15			30	60 ns	22 ns + (0,16 ns/pF) C _L
S _D → O	5			70	140 ns	43 ns + (0,55 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		30	60 ns	19 ns + (0,23 ns/pF) C _L
	15			25	50 ns	17 ns + (0,16 ns/pF) C _L
C _D → O	5			120	240 ns	93 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		45	90 ns	33 ns + (0,23 ns/pF) C _L
	15			35	70 ns	27 ns + (0,16 ns/pF) C _L
S _D → $\bar{O}$	5			140	280 ns	113 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C _L
	15			40	80 ns	32 ns + (0,16 ns/pF) C _L

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
C _D → $\overline{O}$ LOW to HIGH	5 10 15	t _{PLH}		75 35 25	150 ns 70 ns 50 ns	48 ns + (0,55 ns/pF) C _L 24 ns + (0,23 ns/pF) C _L 17 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5 10 15	t _{THL}		60 30 20	120 ns 60 ns 40 ns	10 ns + (1,0 ns/pF) C _L 9 ns + (0,42 ns/pF) C _L 6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5 10 15	t _{TLH}		60 30 20	120 ns 60 ns 40 ns	10 ns + (1,0 ns/pF) C _L 9 ns + (0,42 ns/pF) C _L 6 ns + (0,28 ns/pF) C _L
Set-up time J,K → CP	5 10 15	t _{SU}	50 30 20	25 10 5	ns ns ns	see also waveforms Figs 4 and 5
Hold time J,K → CP	5 10 15	t _{hold}	25 20 15	0 0 5	ns ns ns	
Minimum clock pulse width; LOW	5 10 15	t _{WCPL}	80 30 24	40 15 12	ns ns ns	
Minimum S _D , C _D pulse width; HIGH	5 10 15	t _{WSDH} , t _{WCDH}	90 40 30	45 20 15	ns ns ns	
Recovery time for S _D , C _D	5 10 15	t _{RSD} , t _{RCD}	20 15 10	-15 -10 -5	ns ns ns	
Maximum clock pulse frequency J = K = HIGH	5 10 15	f _{max}	4 12 15	8 25 30	MHz MHz MHz	
						see also waveforms Fig.4

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	900 f _i + Σ (f _o C _L) × V _{DD} ² 4 500 f _i + Σ (f _o C _L) × V _{DD} ² 13 200 f _i + Σ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

Dual JK flip-flop

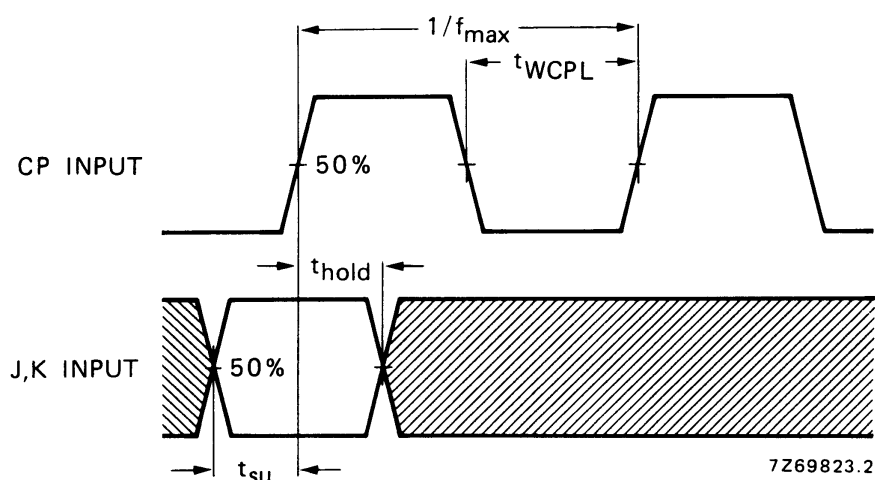
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Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

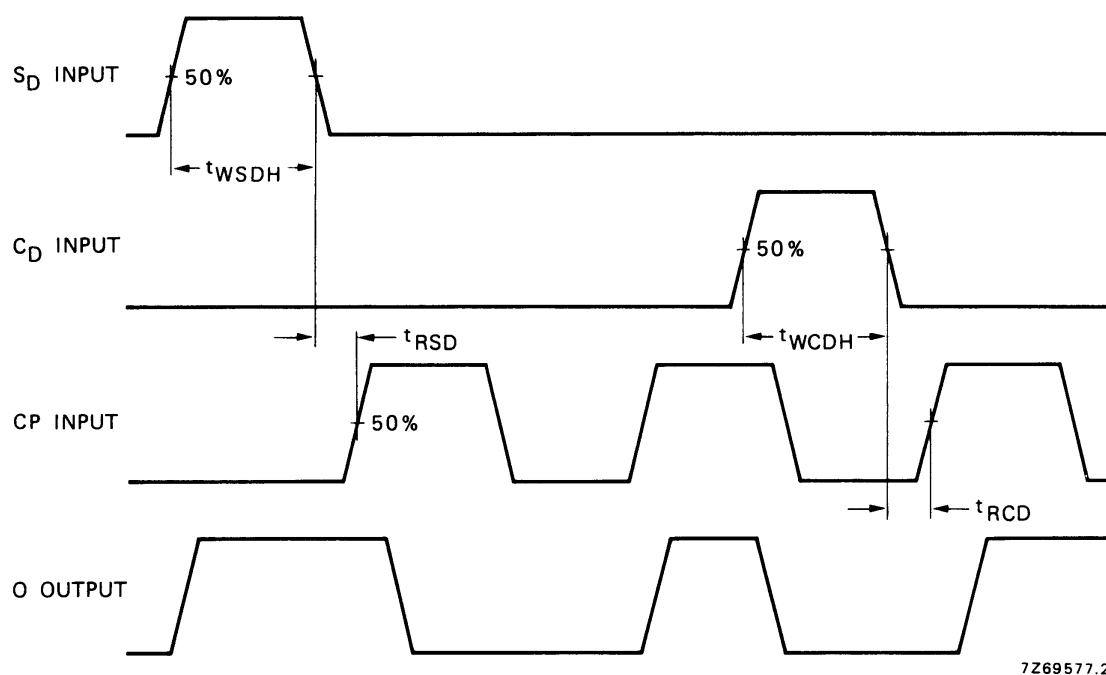


Fig.5 Waveforms showing recovery times for S_D and C_D ; minimum S_D and C_D pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4027B are:

- Registers
- Counters
- Control circuits