

74LV1T125

Single supply translating buffer/line driver; 3-state

Rev. 1 — 22 November 2017

Product data sheet

1 General description

The 74LV1T125 is a single, level translating buffer/line driver with 3-state output. The low threshold inputs support 1.8 V input logic at $V_{CC} = 3.3$ V and can be used in 1.8 V to 3.3 V level up translation. In addition, the 5 V tolerant input pins enable down translation (3.3 V to 2.5 V output at $V_{CC} = 2.5$ V). The 3-state output is controlled by the output enable input (\overline{OE}). A HIGH-level at \overline{OE} causes the output to assume a high-impedance OFF-state. The output level is referenced to the supply voltage and supports 1.8 V, 2.5 V, 3.3 V and 5.0 V CMOS levels. The wide V_{CC} range permits the generation of output levels to connect to controllers or processors.

2 Features and benefits

- Single supply voltage translator at 1.8 V, 2.5 V, 3.3 V and 5.0 V
- Up translation
 - 1.2 V to 1.8 V at $V_{CC} = 1.8$ V
 - 1.5 V to 2.5 V at $V_{CC} = 2.5$ V
 - 1.8 V to 3.3 V at $V_{CC} = 3.3$ V
 - 3.3 V to 5.0 V at $V_{CC} = 5.0$ V
- Down translation
 - 3.3 V to 1.8 V at $V_{CC} = 1.8$ V
 - 3.3 V to 2.5 V at $V_{CC} = 2.5$ V
 - 5.0 V to 3.3 V at $V_{CC} = 3.3$ V
- 5 V tolerant inputs
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - CDM JESD22-C101 exceeds 1 kV
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3 Applications

- Portable applications
- PC and notebooks
- Automotive
- Industrial controller
- Telecom

nexperia

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV1T125GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LV1T125GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.35 mm	SOT1226

5 Marking

Table 2. Marking

Type number	Marking code ^[1]
74LV1T125GW	SN
74LV1T125GX	SN

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6 Functional diagram

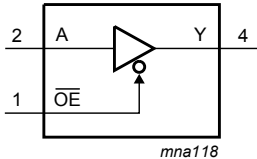


Figure 1. Logic symbol

The logic symbol shows a rectangular box with input A (pin 2) and output Y (pin 4). An enable input OE (pin 1) is shown with a bubble and an arrow pointing to the box. The symbol is labeled mna118.

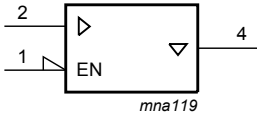


Figure 2. IEC logic symbol

The IEC logic symbol shows a rectangular box with input A (pin 2) and output Y (pin 4). An enable input EN (pin 1) is shown with a triangle pointing to the box. The symbol is labeled mna119.

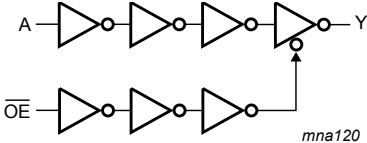
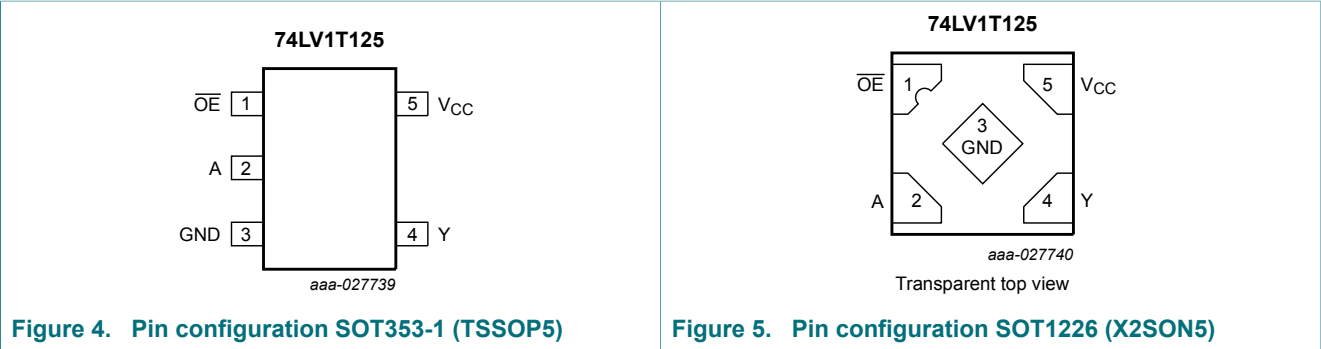


Figure 3. Logic diagram

The logic diagram shows the internal structure of the 74LV1T125. It consists of two 3-input NAND gates. The first NAND gate has inputs A and OE, and its output is Y. The second NAND gate has inputs A and OE, and its output is Y. The symbol is labeled mna120.

7 Pinning information

7.1 Pinning



7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$\overline{\text{OE}}$	1	output enable input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

8 Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
OE	A	Y
L	L	L
L	H	H
H	X	Z

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output HIGH or LOW state [2] [3]	-0.5	$V_{CC} + 0.5$	V
		output in 3-state or power-off state [2]	-0.5	4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-20	-	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$	-	± 20	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [4]	-	250	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

[3] This value is limited to 7 V maximum.

[4] For TSSOP5 packages: above 75 °C the value of P_{tot} derates linearly with 3.3 mW/K.
For X2SON5 package: above 70 °C the value of P_{tot} derates linearly with 3.1 mW/K.

10 Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.6	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.8$ V to 5.0 V	-	-	20	ns/V

11 Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.8 V	0.94	-	1.0	-	1.0	-	V
		V _{CC} = 2.0 V	0.99	-	1.03	-	1.03	-	V
		V _{CC} = 2.25 V to 2.5 V	1.135	-	1.18	-	1.18	-	V
		V _{CC} = 2.75 V	1.21	-	1.23	-	1.23	-	V
		V _{CC} = 3.0 V to 3.3 V	1.35	-	1.37	-	1.37	-	V
		V _{CC} = 3.6 V	1.47	-	1.48	-	1.48	-	V
		V _{CC} = 4.5 V to 5.0 V	2.02	-	2.03	-	2.03	-	V
		V _{CC} = 5.5 V	2.10	-	2.11	-	2.11	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 2.0 V	-	0.58	-	0.55	-	0.55	V
		V _{CC} = 2.25 V to 2.75 V	-	0.75	-	0.71	-	0.71	V
		V _{CC} = 3.0 V to 3.6 V	-	0.80	-	0.65	-	0.65	V
		V _{CC} = 4.5 V to 5.5 V	-	0.80	-	0.80	-	0.80	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ;							
		V _{CC} = 1.65 V to 5.5 V; I _O = -20 µA	V _{CC} -0.1	-	V _{CC} -0.1	-	V _{CC} -0.1	-	V
		V _{CC} = 1.65 V; I _O = -2 mA	1.28	-	1.21	-	1.21	-	V
		V _{CC} = 1.8 V; I _O = -2 mA	1.5	-	1.45	-	1.45	-	V
		V _{CC} = 2.3 V; I _O = -2.3 mA	2.0	-	2.0	-	2.0	-	V
		V _{CC} = 2.3 V; I _O = -3 mA	2.0	-	1.93	-	1.93	-	V
		V _{CC} = 2.5 V; I _O = -3 mA	2.25	-	2.15	-	2.15	-	V
		V _{CC} = 3.0 V; I _O = -3 mA	2.78	-	2.7	-	2.7	-	V
		V _{CC} = 3.0 V; I _O = -5.5 mA	2.6	-	2.49	-	2.49	-	V
		V _{CC} = 3.3 V; I _O = -5.5 mA	2.9	-	2.8	-	2.8	-	V
		V _{CC} = 4.5 V; I _O = -4 mA	4.2	-	4.1	-	4.1	-	V
		V _{CC} = 4.5 V; I _O = -8 mA	4.1	-	3.95	-	3.95	-	V
		V _{CC} = 5.0 V; I _O = -8 mA	4.6	-	4.5	-	4.5	-	V

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}							
		V _{CC} = 1.65 V to 5.5 V; I _O = 20 µA	-	0.1	-	0.1	-	0.1	V
		V _{CC} = 1.65 V; I _O = 2 mA	-	0.2	-	0.25	-	0.25	V
		V _{CC} = 2.3 V; I _O = 2.3 mA	-	0.1	-	0.15	-	0.15	V
		V _{CC} = 2.3 V; I _O = 3 mA	-	0.15	-	0.2	-	0.2	V
		V _{CC} = 3.0 V; I _O = 3 mA	-	0.1	-	0.15	-	0.15	V
		V _{CC} = 3.0 V; I _O = 5.5 mA	-	0.2	-	0.252	-	0.252	V
		V _{CC} = 4.5 V; I _O = 4 mA	-	0.15	-	0.2	-	0.2	V
		V _{CC} = 4.5 V; I _O = 8 mA	-	0.3	-	0.35	-	0.35	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	-	±1	-	±1	µA
I _{OZ}	OFF-state output current		-	±0.25	-	±2.5	-	±2.5	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 1.8 V, 2.5 V, 3.3 V, 5.0 V	-	1	-	10	-	10	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 1.8 V; V _I = 0.3 V or 1.1 V; I _O = 0 A; other pins at V _{CC} or GND	-	10	-	10	-	10	µA
		per input pin; V _{CC} = 5.5 V; V _I = 0.3 V or 3.4 V; I _O = 0 A; other pins at V _{CC} or GND	-	1.35	-	1.5	-	1.5	mA

12 Dynamic characteristics

Table 8. Dynamic characteristics

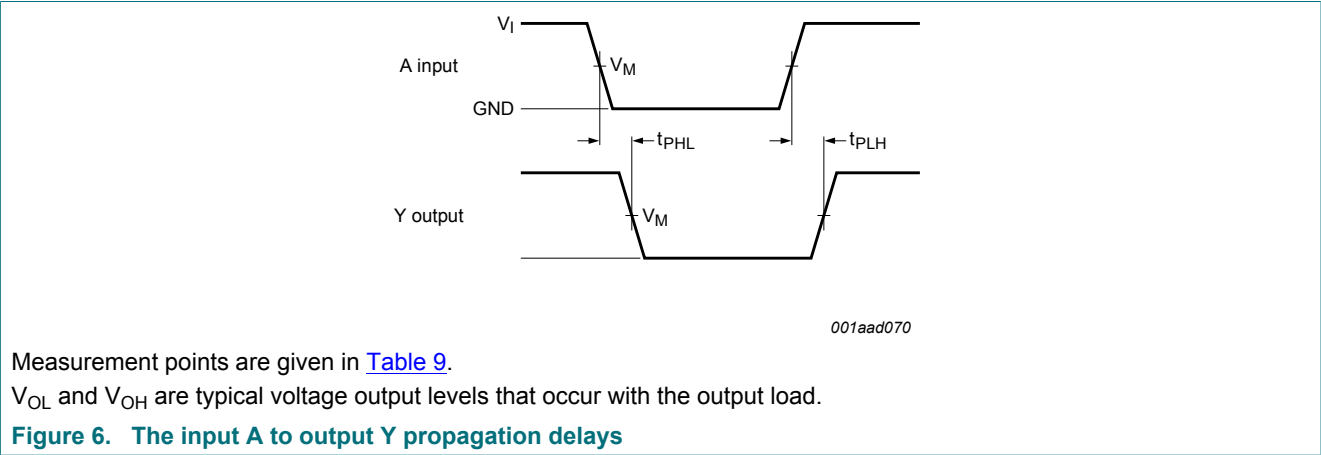
$GND = 0\text{ V}$. For test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +125 °C					Unit
			Min	Typ 25 °C	Max 25 °C	Max 85 °C	Max 125 °C	
t_{pd}	propagation delay	A to Y; see Figure 6 ^[1]						
		$V_{CC} = 1.8\text{ V}; C_L = 15\text{ pF}$	-	6.5	9.6	10.8	11.6	ns
		$V_{CC} = 1.8\text{ V}; C_L = 30\text{ pF}$	-	7.6	10.8	12.2	13.1	ns
		$V_{CC} = 2.5\text{ V}; C_L = 15\text{ pF}$	-	4.6	6.6	7.5	8.0	ns
		$V_{CC} = 2.5\text{ V}; C_L = 30\text{ pF}$	-	5.3	7.4	8.4	9.1	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	3.8	5.4	6.0	6.4	ns
		$V_{CC} = 3.3\text{ V}; C_L = 30\text{ pF}$	-	4.4	6.0	6.8	7.3	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	3.2	4.1	4.4	4.7	ns
		$V_{CC} = 5.0\text{ V}; C_L = 30\text{ pF}$	-	3.6	4.6	5.1	5.4	ns
t_{en}	enable time	\overline{OE} to Y; see Figure 7 ^[1]						
		$V_{CC} = 1.8\text{ V}; C_L = 15\text{ pF}$	-	7.8	10.7	12.1	12.9	ns
		$V_{CC} = 1.8\text{ V}; C_L = 30\text{ pF}$	-	9.0	12.6	14.3	15.3	ns
		$V_{CC} = 2.5\text{ V}; C_L = 15\text{ pF}$	-	5.5	7.1	8.0	8.6	ns
		$V_{CC} = 2.5\text{ V}; C_L = 30\text{ pF}$	-	6.3	8.3	9.3	10.0	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	4.5	5.6	6.3	6.8	ns
		$V_{CC} = 3.3\text{ V}; C_L = 30\text{ pF}$	-	5.1	6.4	7.2	7.7	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	3.2	4.1	4.6	4.8	ns
		$V_{CC} = 5.0\text{ V}; C_L = 30\text{ pF}$	-	3.7	4.7	5.3	5.5	ns
t_{dis}	disable time	\overline{OE} to Y; see Figure 7 ^[1]						
		$V_{CC} = 1.8\text{ V}; C_L = 15\text{ pF}$	-	7.6	9.7	10.7	11.3	ns
		$V_{CC} = 1.8\text{ V}; C_L = 30\text{ pF}$	-	10.5	12.9	14.0	14.7	ns
		$V_{CC} = 2.5\text{ V}; C_L = 15\text{ pF}$	-	5.5	7.0	7.7	8.1	ns
		$V_{CC} = 2.5\text{ V}; C_L = 30\text{ pF}$	-	7.4	9.0	10.0	10.3	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	4.5	5.8	6.4	6.7	ns
		$V_{CC} = 3.3\text{ V}; C_L = 30\text{ pF}$	-	5.9	7.5	8.1	8.6	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	4.0	5.5	5.9	6.2	ns
		$V_{CC} = 5.0\text{ V}; C_L = 30\text{ pF}$	-	5.0	6.5	6.9	7.3	ns

Symbol	Parameter	Conditions	-40 °C to +125 °C					Unit
			Min	Typ 25 °C	Max 25 °C	Max 85 °C	Max 125 °C	
C _I	input capacitance	V _I = V _{CC} or GND; V _{CC} = 3.3 V	-	1.5	10	10	10	pF
C _O	output capacitance	V _O = V _{CC} or GND; V _{CC} = 3.3 V	-	2.5	-	-	-	pF
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ; C _L = 30 pF; f = 10 MHz ^[2]						
		V _{CC} = 1.8 V	-	4.1	-	-	-	pF
		V _{CC} = 2.5 V	-	5.3	-	-	-	pF
		V _{CC} = 3.3 V	-	6.9	-	-	-	pF
		V _{CC} = 5.0 V	-	10.7	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}. t_{en} is the same as t_{PZL} and t_{PZH}. t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

12.1 Waveforms and test circuit



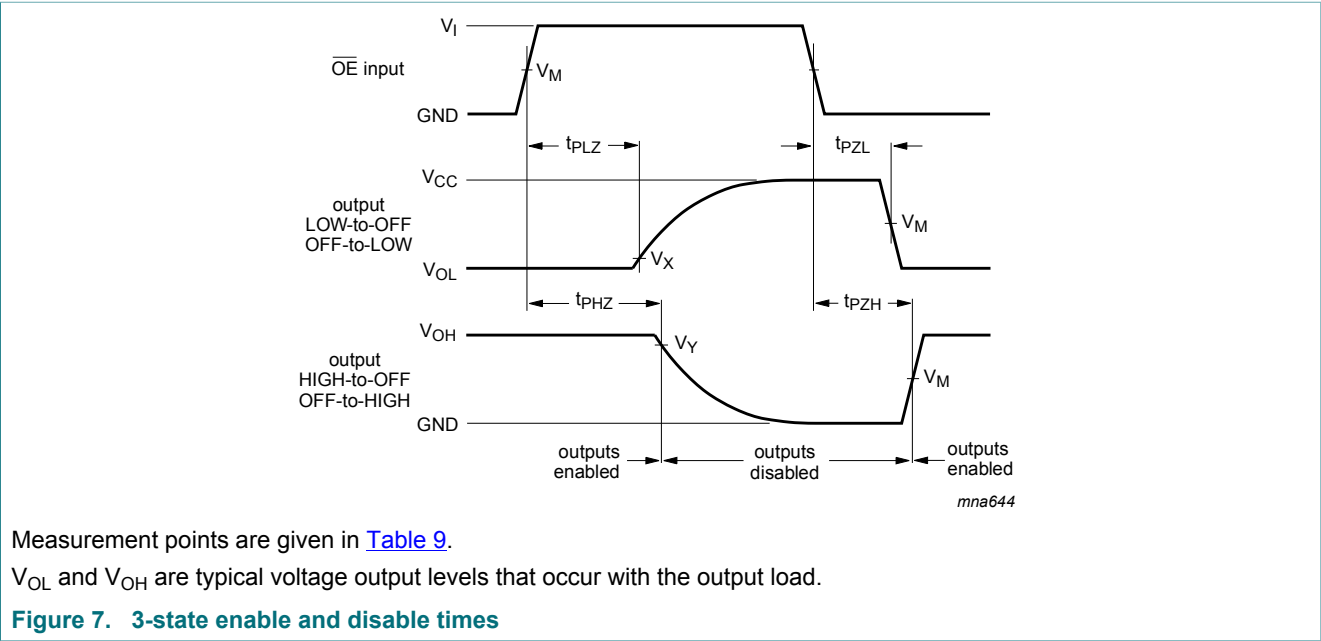


Table 9. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
$0.5V_I$	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

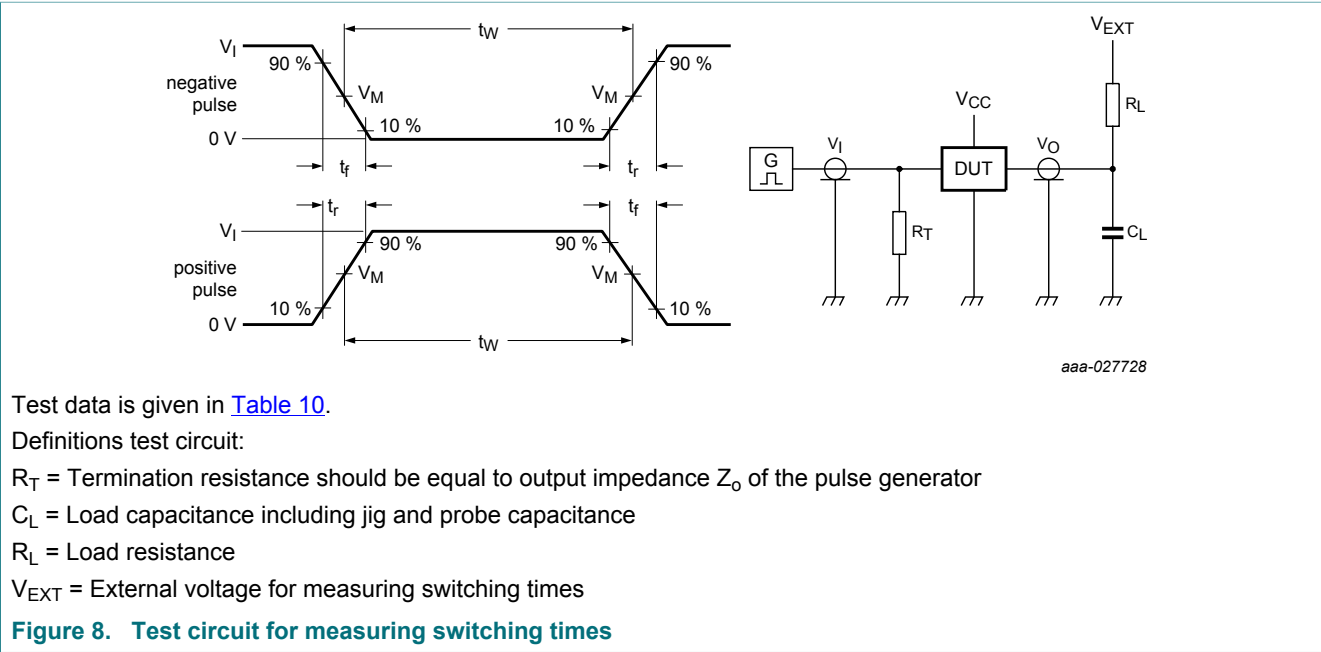


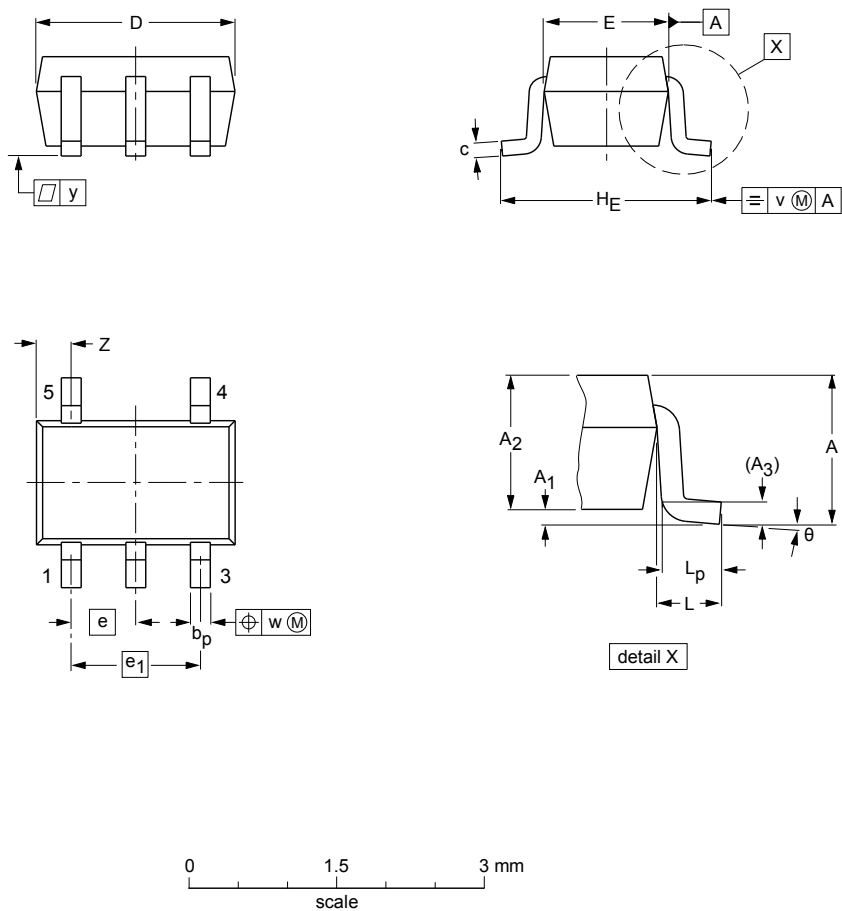
Table 10. Test data

Supply voltage	Input			Load	V_{EXT}			
V_{CC}	V_I	$\Delta t/\Delta V$ [1]	f_{max}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.8 V	V_{CC}	$\leq 1.0 \text{ ns/V}$	15 MHz	15 pF, 30 pF	1 k Ω	open	GND	V_{CC}
2.5 V	V_{CC}	$\leq 1.0 \text{ ns/V}$	25 MHz	15 pF, 30 pF	1 k Ω	open	GND	V_{CC}
3.3 V	3 V	$\leq 1.0 \text{ ns/V}$	50 MHz	15 pF, 30 pF	1 k Ω	open	GND	V_{CC}
5.0 V	3 V	$\leq 1.0 \text{ ns/V}$	50 MHz	15 pF, 30 pF	1 k Ω	open	GND	V_{CC}

[1] $dV/dt \geq 1.0 \text{ V/ns}$

13 Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm SOT353-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			00-09-01 03-02-19

Figure 9. Package outline SOT353-1 (TSSOP5)

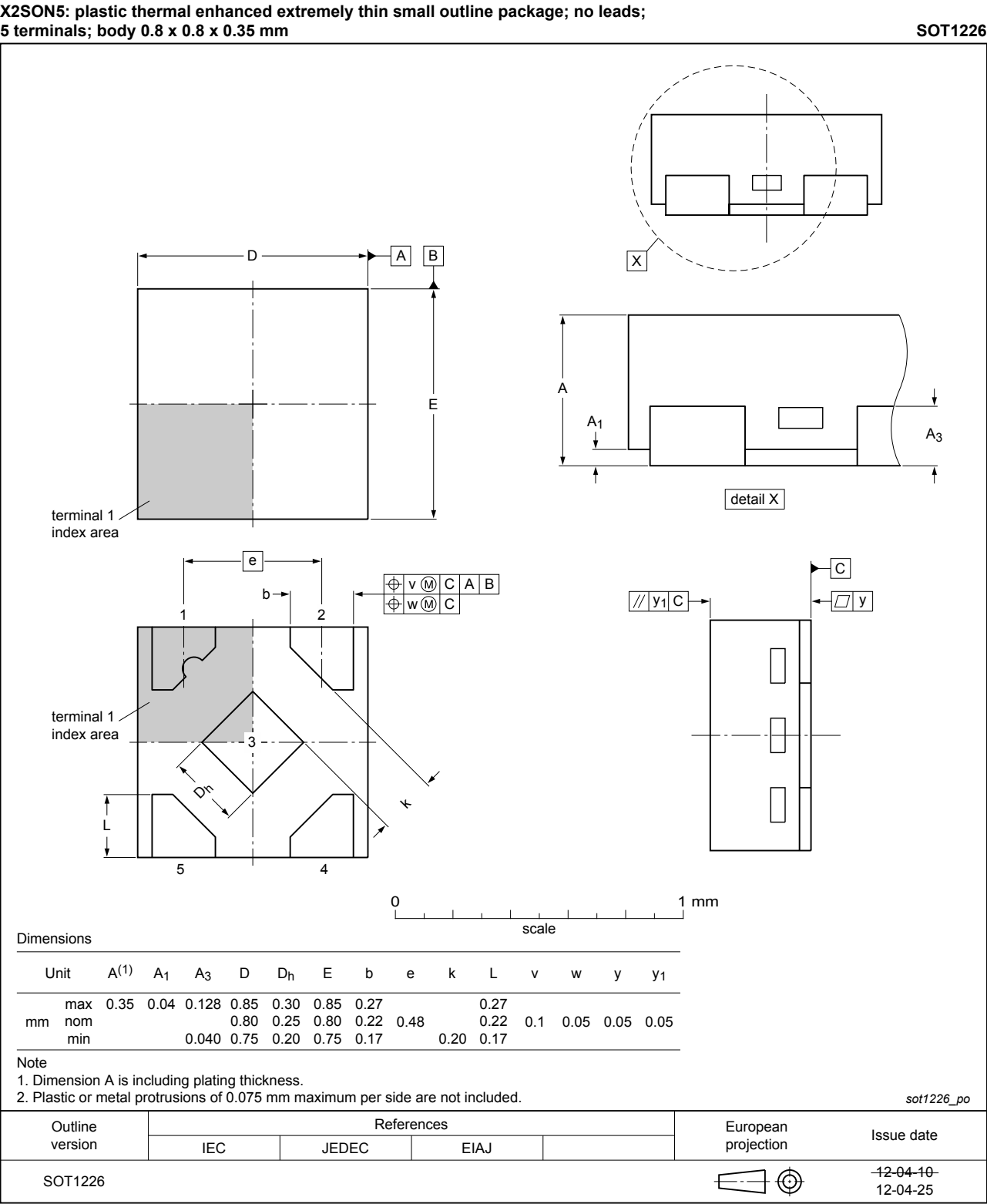


Figure 10. Package outline SOT1226 (X2SON5)

14 Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV1T125 v.1	20171122	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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Single supply translating buffer/line driver; 3-state

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Contents

1 General description 1

2 Features and benefits1

3 Applications1

4 Ordering information 2

5 Marking2

6 Functional diagram2

7 Pinning information 3

7.1 Pinning 3

7.2 Pin description 3

8 Functional description3

9 Limiting values4

10 Recommended operating conditions4

11 Static characteristics5

12 Dynamic characteristics7

12.1 Waveforms and test circuit 8

13 Package outline11

14 Abbreviations 13

15 Revision history 13

16 Legal information 14

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