# 74AVCH1T45

## Dual-supply voltage level translator/transceiver; 3-state

Rev. 5 — 6 January 2016 **Product data sheet**

## 1. General description

The 74AVCH1T45 is a single bit, dual supply transceiver that enables bidirectional level translation. It features two 1-bit input-output ports (A and B), a direction control input (DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins A and DIR are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The device is fully specified for partial power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A and B are in the high-impedance OFF-state.

The 74AVCH1T45 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## 2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 0.8 V to 3.6 V
  - $V_{CC(B)}$: 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E Class 3B exceeds 8000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
  - 500 Mbit/s (1.8 V to 3.3 V translation)
  - 320 Mbit/s (< 1.8 V to 3.3 V translation)
  - 320 Mbit/s (translate to 2.5 V or 1.8 V)
  - 280 Mbit/s (translate to 1.5 V)

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- 240 Mbit/s (translate to 1.2 V)
- Suspend mode
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of $V_{CC}$
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74AVCH1T45GW | –40 °C to +125 °C | SC-88 | plastic surface-mounted package; 6 leads | SOT363 |
| 74AVCH1T45GM | –40 °C to +125 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm | SOT886 |
| 74AVCH1T45GN | –40 °C to +125 °C | XSON6 | extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm | SOT1115 |
| 74AVCH1T45GS | –40 °C to +125 °C | XSON6 | extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm | SOT1202 |

## 4. Marking

**Table 2. Marking**

| Type number | Marking code[1] |
|---|---|
| 74AVCH1T45GW | K5 |
| 74AVCH1T45GM | K5 |
| 74AVCH1T45GN | K5 |
| 74AVCH1T45GS | K5 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

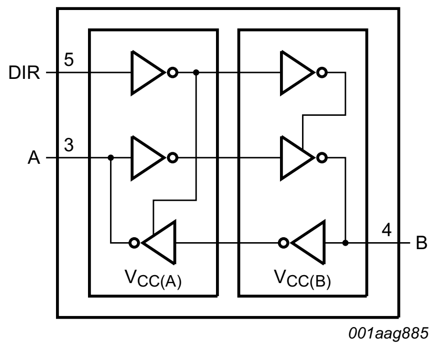



**Fig 1. Logic symbol**

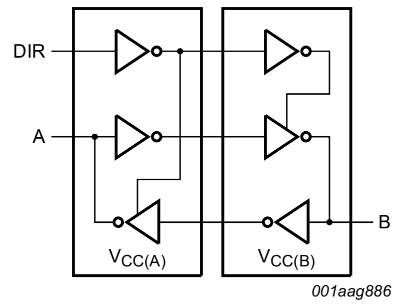



**Fig 2. Logic diagram**

## 6. Pinning information

### 6.1 Pinning

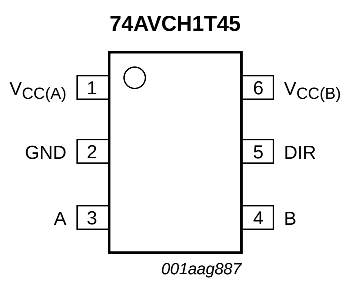



**Fig 3. Pin configuration SOT363**

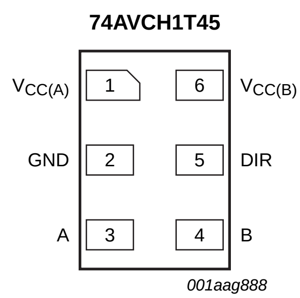



**Fig 4. Pin configuration SOT886**

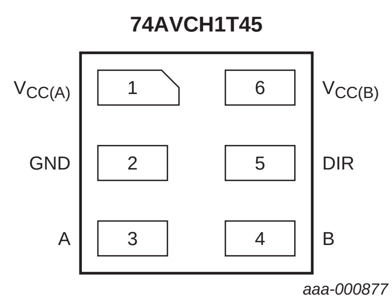



**Fig 5. Pin configuration SOT1115 and SOT1202**

### 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{CC(A)}$ | 1 | supply voltage port A and DIR |
| GND | 2 | ground (0 V) |
| A | 3 | data input or output |
| B | 4 | data input or output |
| DIR | 5 | direction control |
| $V_{CC(B)}$ | 6 | supply voltage port B |

## 7. Functional description

### Table 4. Function table[1]

| Supply voltage | Input | Input/output[2] | |
|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | DIR[3] | A | B |
| 0.8 V to 3.6 V | L | A = B | input |
| 0.8 V to 3.6 V | H | input | B = A |
| GND[4] | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The input circuit of the data I/O is always active.

[3] The DIR input circuit is referenced to $V_{CC(A)}$.

[4] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into Suspend mode.

## 8. Limiting values

### Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC(A)}$ | supply voltage A | | –0.5 | +4.6 | V |
| $V_{CC(B)}$ | supply voltage B | | –0.5 | +4.6 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | –50 | - | mA |
| $V_I$ | input voltage | [1] | –0.5 | +4.6 | V |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | –50 | - | mA |
| $V_O$ | output voltage | Active mode [1][2][3] | –0.5 | $V_{CCO}$ + 0.5 | V |
| | | Suspend or 3-state mode [1] | –0.5 | +4.6 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CCO}$ | - | ±50 | mA |
| $I_{CC}$ | supply current | $I_{CC(A)}$ or $I_{CC(B)}$ | - | 100 | mA |
| $I_{GND}$ | ground current | | –100 | - | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +125 °C [4] | - | 250 | mW |

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] $V_{CCO}$ is the supply voltage associated with the output port.

[3] $V_{CCO}$ + 0.5 V should not exceed 4.6 V.

[4] For SC-88 packages: above 87.5 °C the value of $P_{tot}$ derates linearly with 4.0 mW/K.
For XSON6 packages: above 118 °C the value of $P_{tot}$ derates linearly with 7.8 mW/K.

## 9. Recommended operating conditions

### Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC(A)}$ | supply voltage A | | 0.8 | 3.6 | V |
| $V_{CC(B)}$ | supply voltage B | | 0.8 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 3.6 | V |

**Table 6. Recommended operating conditions** *...continued*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_O$ | output voltage | Active mode [1] | 0 | $V_{CCO}$ | V |
| | | Suspend or 3-state mode | 0 | 3.6 | V |
| $T_{amb}$ | ambient temperature | | –40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CCI}$ = 0.8 V to 3.6 V [2] | - | 5 | ns/V |

[1] $V_{CCO}$ is the supply voltage associated with the output port.

[2] $V_{CCI}$ is the supply voltage associated with the input port.

## 10. Static characteristics

**Table 7. Typical static characteristics at $T_{amb}$ = 25 °C[1][2]**
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = –1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V | - | 0.69 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = 1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V | - | 0.07 | - | V |
| $I_I$ | input leakage current | DIR input; $V_I$ = 0 V or 3.6 V; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V | - | ±0.025 | ±0.25 | μA |
| $I_{BHL}$ | bus hold LOW current | $V_I$ = 0.42 V; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V [3] | - | 26 | - | μA |
| $I_{BHH}$ | bus hold HIGH current | $V_I$ = 0.78 V; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V [4] | - | –24 | - | μA |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_I$ = GND to $V_{CCI}$; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V [5] | - | 28 | - | μA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_I$ = GND to $V_{CCI}$; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V [6] | - | –26 | - | μA |
| $I_{OZ}$ | OFF-state output current | A or B port; $V_O$ = 0 V or $V_{CCO}$; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V [7] | - | ±0.5 | ±2.5 | μA |
| $I_{OFF}$ | power-off leakage current | A port; $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V | - | ±0.1 | ±1 | μA |
| | | B port; $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V | - | ±0.1 | ±1 | μA |
| $C_I$ | input capacitance | DIR input; $V_I$ = 0 V or 3.3 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V | - | 1.0 | - | pF |
| $C_{I/O}$ | input/output capacitance | A and B port; Suspend mode; $V_O = V_{CCO}$ or GND; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V | - | 4.0 | - | pF |

[1] $V_{CCO}$ is the supply voltage associated with the output port.

[2] $V_{CCI}$ is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_I$ to GND and then raising it to $V_{IL}$ max.

[4] The bus hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_I$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.

[5] An external driver must source at least $I_{BHLO}$ to switch this node from LOW to HIGH.

[6] An external driver must sink at least $I_{BHHO}$ to switch this node from HIGH to LOW.

[7] For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

**Table 8. Static characteristics [1][2]**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | data input | | | | | |
| | | $V_{CCI}$ = 0.8 V | $0.70V_{CCI}$ | - | $0.70V_{CCI}$ | - | V |
| | | $V_{CCI}$ = 1.1 V to 1.95 V | $0.65V_{CCI}$ | - | $0.65V_{CCI}$ | - | V |
| | | $V_{CCI}$ = 2.3 V to 2.7 V | 1.6 | - | 1.6 | - | V |
| | | $V_{CCI}$ = 3.0 V to 3.6 V | 2 | - | 2 | - | V |
| | | DIR input | | | | | |
| | | $V_{CC(A)}$ = 0.8 V | $0.70V_{CC(A)}$ | - | $0.70V_{CC(A)}$ | - | V |
| | | $V_{CC(A)}$ = 1.1 V to 1.95 V | $0.65V_{CC(A)}$ | - | $0.65V_{CC(A)}$ | - | V |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V | 1.6 | - | 1.6 | - | V |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V | 2 | - | 2 | - | V |
| $V_{IL}$ | LOW-level input voltage | data input | | | | | |
| | | $V_{CCI}$ = 0.8 V | - | $0.30V_{CCI}$ | - | $0.30V_{CCI}$ | V |
| | | $V_{CCI}$ = 1.1 V to 1.95 V | - | $0.35V_{CCI}$ | - | $0.35V_{CCI}$ | V |
| | | $V_{CCI}$ = 2.3 V to 2.7 V | - | 0.7 | - | 0.7 | V |
| | | $V_{CCI}$ = 3.0 V to 3.6 V | - | 0.9 | - | 0.9 | V |
| | | DIR input | | | | | |
| | | $V_{CC(A)}$ = 0.8 V | - | $0.30V_{CC(A)}$ | - | $0.30V_{CC(A)}$ | V |
| | | $V_{CC(A)}$ = 1.1 V to 1.95 V | - | $0.35V_{CC(A)}$ | - | $0.35V_{CC(A)}$ | V |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V | - | 0.7 | - | 0.7 | V |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V | - | 0.9 | - | 0.9 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –100 μA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V | $V_{CCO} - 0.1$ | - | $V_{CCO} - 0.1$ | - | V |
| | | $I_O$ = –3 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.1 V | 0.85 | - | 0.85 | - | V |
| | | $I_O$ = –6 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.4 V | 1.05 | - | 1.05 | - | V |
| | | $I_O$ = –8 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.65 V | 1.2 | - | 1.2 | - | V |
| | | $I_O$ = –9 mA; $V_{CC(A)} = V_{CC(B)}$ = 2.3 V | 1.75 | - | 1.75 | - | V |
| | | $I_O$ = –12 mA; $V_{CC(A)} = V_{CC(B)}$ = 3.0 V | 2.3 | - | 2.3 | - | V |

**Table 8. Static characteristics** *...continued*[1][2]
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = 100\ \mu A$; $V_{CC(A)} = V_{CC(B)} = 0.8$ V to 3.6 V | - | 0.1 | - | 0.1 | V |
| | | $I_O = 3$ mA; $V_{CC(A)} = V_{CC(B)} = 1.1$ V | - | 0.25 | - | 0.25 | V |
| | | $I_O = 6$ mA; $V_{CC(A)} = V_{CC(B)} = 1.4$ V | - | 0.35 | - | 0.35 | V |
| | | $I_O = 8$ mA; $V_{CC(A)} = V_{CC(B)} = 1.65$ V | - | 0.45 | - | 0.45 | V |
| | | $I_O = 9$ mA; $V_{CC(A)} = V_{CC(B)} = 2.3$ V | - | 0.55 | - | 0.55 | V |
| | | $I_O = 12$ mA; $V_{CC(A)} = V_{CC(B)} = 3.0$ V | - | 0.7 | - | 0.7 | V |
| $I_I$ | input leakage current | DIR input; $V_I = 0$ V or 3.6 V; $V_{CC(A)} = V_{CC(B)} = 0.8$ V to 3.6 V | - | ±1 | - | ±1.5 | μA |
| $I_{BHL}$ | bus hold LOW current | A or B port [3] | | | | | |
| | | $V_I = 0.49$ V; $V_{CC(A)} = V_{CC(B)} = 1.4$ V | 15 | - | 15 | - | μA |
| | | $V_I = 0.58$ V; $V_{CC(A)} = V_{CC(B)} = 1.65$ V | 25 | - | 25 | - | μA |
| | | $V_I = 0.70$ V; $V_{CC(A)} = V_{CC(B)} = 2.3$ V | 45 | - | 45 | - | μA |
| | | $V_I = 0.80$ V; $V_{CC(A)} = V_{CC(B)} = 3.0$ V | 100 | - | 90 | - | μA |
| $I_{BHH}$ | bus hold HIGH current | A or B port [4] | | | | | |
| | | $V_I = 0.91$ V; $V_{CC(A)} = V_{CC(B)} = 1.4$ V | –15 | - | –15 | - | μA |
| | | $V_I = 1.07$ V; $V_{CC(A)} = V_{CC(B)} = 1.65$ V | –25 | - | –25 | - | μA |
| | | $V_I = 1.60$ V; $V_{CC(A)} = V_{CC(B)} = 2.3$ V | –45 | - | –45 | - | μA |
| | | $V_I = 2.00$ V; $V_{CC(A)} = V_{CC(B)} = 3.0$ V | –100 | - | –100 | - | μA |
| $I_{BHLO}$ | bus hold LOW overdrive current | A or B port [5] | | | | | |
| | | $V_{CC(A)} = V_{CC(B)} = 1.6$ V | 125 | - | 125 | - | μA |
| | | $V_{CC(A)} = V_{CC(B)} = 1.95$ V | 200 | - | 200 | - | μA |
| | | $V_{CC(A)} = V_{CC(B)} = 2.7$ V | 300 | - | 300 | - | μA |
| | | $V_{CC(A)} = V_{CC(B)} = 3.6$ V | 500 | - | 500 | - | μA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | A or B port [6] | | | | | |
| | | $V_{CC(A)} = V_{CC(B)} = 1.6$ V | –125 | - | –125 | - | μA |
| | | $V_{CC(A)} = V_{CC(B)} = 1.95$ V | –200 | - | –200 | - | μA |
| | | $V_{CC(A)} = V_{CC(B)} = 2.7$ V | –300 | - | –300 | - | μA |
| | | $V_{CC(A)} = V_{CC(B)} = 3.6$ V | –500 | - | –500 | - | μA |
| $I_{OZ}$ | OFF-state output current | A or B port; $V_O = 0$ V or $V_{CCO}$; $V_{CC(A)} = V_{CC(B)} = 0.8$ V to 3.6 V [7] | - | ±5 | - | ±7.5 | μA |

**Table 8. Static characteristics** *...continued*[1][2]

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $I_{OFF}$ | power-off leakage current | A port; $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V | - | ±5 | - | ±35 | μA |
| | | B port; $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V | - | ±5 | - | ±35 | μA |
| $I_{CC}$ | supply current | A port; $V_I$ = 0 V or $V_{CCI}$; $I_O$ = 0 A | | | | | |
| | | $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V | - | 8 | - | 12 | μA |
| | | $V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V | - | 8 | - | 12 | μA |
| | | $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V | –2 | - | –8 | - | μA |
| | | B port; $V_I$ = 0 V or $V_{CCI}$; $I_O$ = 0 A | | | | | |
| | | $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V | - | 8 | - | 12 | μA |
| | | $V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V | –2 | - | –8 | - | μA |
| | | $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V | - | 8 | - | 12 | μA |
| | | A plus B port ($I_{CC(A)} + I_{CC(B)}$); $I_O$ = 0 A; $V_I$ = 0 V or $V_{CCI}$; $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V | - | 16 | - | 24 | μA |

[1] $V_{CCO}$ is the supply voltage associated with the output port.

[2] $V_{CCI}$ is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_I$ to GND and then raising it to $V_{IL}$ max.

[4] The bus hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_I$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.

[5] An external driver must source at least $I_{BHLO}$ to switch this node from LOW to HIGH.

[6] An external driver must sink at least $I_{BHHO}$ to switch this node from HIGH to LOW.

[7] For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## 11. Dynamic characteristics

**Table 9. Typical dynamic characteristics at $V_{CC(A)}$ = 0.8 V and $T_{amb}$ = 25 °C [1]**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7*

| Symbol | Parameter | Conditions | $V_{CC(B)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 0.8 V | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | |
| $t_{pd}$ | propagation delay | A to B | 15.8 | 8.4 | 8.0 | 8.0 | 8.7 | 9.5 | ns |
| | | B to A | 15.8 | 12.7 | 12.4 | 12.2 | 12.0 | 11.8 | ns |
| $t_{dis}$ | disable time | DIR to A | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | ns |
| | | DIR to B | 11.7 | 7.9 | 7.6 | 8.2 | 8.7 | 10.2 | ns |
| $t_{en}$ | enable time | DIR to A | 27.5 | 20.6 | 20.0 | 20.4 | 20.7 | 22.0 | ns |
| | | DIR to B | 28.0 | 20.6 | 20.2 | 20.2 | 20.9 | 21.7 | ns |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{en}$ is a calculated value using the formula shown in Section 13.4 "Enable times"

**Table 10. Typical dynamic characteristics at $V_{CC(B)}$ = 0.8 V and $T_{amb}$ = 25 °C [1]**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7*

| Symbol | Parameter | Conditions | $V_{CC(A)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 0.8 V | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | |
| $t_{pd}$ | propagation delay | A to B | 15.8 | 12.7 | 12.4 | 12.2 | 12.0 | 11.8 | ns |
| | | B to A | 15.8 | 8.4 | 8.0 | 8.0 | 8.7 | 9.5 | ns |
| $t_{dis}$ | disable time | DIR to A | 12.2 | 4.9 | 3.8 | 3.7 | 2.8 | 3.4 | ns |
| | | DIR to B | 11.7 | 9.2 | 9.0 | 8.8 | 8.7 | 8.6 | ns |
| $t_{en}$ | enable time | DIR to A | 27.5 | 17.6 | 17.0 | 16.8 | 17.4 | 18.1 | ns |
| | | DIR to B | 28.0 | 17.6 | 16.2 | 15.9 | 14.8 | 15.2 | ns |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{en}$ is a calculated value using the formula shown in Section 13.4 "Enable times"

**Table 11. Typical power dissipation capacitance at $V_{CC(A)}$ = $V_{CC(B)}$ and $T_{amb}$ = 25 °C [1][2]**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $V_{CC(A)}$ and $V_{CC(B)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 0.8 V | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | |
| $C_{PD}$ | power dissipation capacitance | A port: (direction A to B); B port: (direction B to A) | 1 | 2 | 2 | 2 | 2 | 2 | pF |
| | | A port: (direction B to A); B port: (direction A to B) | 9 | 11 | 11 | 12 | 14 | 17 | pF |

[1] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i$ = 10 MHz; $V_I$ = GND to $V_{CC}$; $t_r = t_f$ = 1 ns; $C_L$ = 0 pF; $R_L = \infty\ \Omega$.

**Table 12. Dynamic characteristics for temperature range –40 °C to +85 °C [1]**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.*

| Symbol | Parameter | Conditions | $V_{CC(B)}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V ± 0.1 V | | 1.5 V ± 0.1 V | | 1.8 V ± 0.15 V | | 2.5 V ± 0.2 V | | 3.3 V ± 0.3 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| **$V_{CC(A)}$ = 1.1 V to 1.3 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 9.0 | 0.7 | 6.8 | 0.6 | 6.1 | 0.5 | 5.7 | 0.5 | 6.1 | ns |
| | | B to A | 1.0 | 9.0 | 0.8 | 8.0 | 0.7 | 7.7 | 0.6 | 7.2 | 0.5 | 7.1 | ns |
| $t_{dis}$ | disable time | DIR to A | 2.2 | 8.8 | 2.2 | 8.8 | 2.2 | 8.8 | 2.2 | 8.8 | 2.2 | 8.8 | ns |
| | | DIR to B | 2.2 | 8.4 | 1.8 | 6.7 | 2.0 | 6.9 | 1.7 | 6.2 | 2.4 | 7.2 | ns |
| $t_{en}$ | enable time | DIR to A | - | 17.4 | - | 14.7 | - | 14.6 | - | 13.4 | - | 14.3 | ns |
| | | DIR to B | - | 17.8 | - | 15.6 | - | 14.9 | - | 14.5 | - | 14.9 | ns |
| **$V_{CC(A)}$ = 1.4 V to 1.6 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 8.0 | 0.7 | 5.4 | 0.6 | 4.6 | 0.5 | 3.7 | 0.5 | 3.5 | ns |
| | | B to A | 1.0 | 6.8 | 0.8 | 5.4 | 0.7 | 5.1 | 0.6 | 4.7 | 0.5 | 4.5 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.6 | 6.3 | 1.6 | 6.3 | 1.6 | 6.3 | 1.6 | 6.3 | 1.6 | 6.3 | ns |
| | | DIR to B | 2.0 | 7.6 | 1.8 | 5.9 | 1.6 | 6.0 | 1.2 | 4.8 | 1.7 | 5.5 | ns |
| $t_{en}$ | enable time | DIR to A | - | 14.4 | - | 11.3 | - | 11.1 | - | 9.5 | - | 10.0 | ns |
| | | DIR to B | - | 14.3 | - | 11.7 | - | 10.9 | - | 10.0 | - | 9.8 | ns |
| **$V_{CC(A)}$ = 1.65 V to 1.95 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 7.7 | 0.6 | 5.1 | 0.5 | 4.3 | 0.5 | 3.4 | 0.5 | 3.1 | ns |
| | | B to A | 1.0 | 6.1 | 0.7 | 4.6 | 0.5 | 4.4 | 0.5 | 3.9 | 0.5 | 3.7 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.6 | 5.5 | 1.6 | 5.5 | 1.6 | 5.5 | 1.6 | 5.5 | 1.6 | 5.5 | ns |
| | | DIR to B | 1.8 | 7.8 | 1.8 | 5.7 | 1.4 | 5.8 | 1.0 | 4.5 | 1.5 | 5.2 | ns |
| $t_{en}$ | enable time | DIR to A | - | 13.9 | - | 10.3 | - | 10.2 | - | 8.4 | - | 8.9 | ns |
| | | DIR to B | - | 13.2 | - | 10.6 | - | 9.8 | - | 8.9 | - | 8.6 | ns |
| **$V_{CC(A)}$ = 2.3 V to 2.7 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 7.2 | 0.5 | 4.7 | 0.5 | 3.9 | 0.5 | 3.0 | 0.5 | 2.6 | ns |
| | | B to A | 1.0 | 5.7 | 0.6 | 3.8 | 0.5 | 3.4 | 0.5 | 3.0 | 0.5 | 2.8 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.5 | 4.2 | 1.5 | 4.2 | 1.5 | 4.2 | 1.5 | 4.2 | 1.5 | 4.2 | ns |
| | | DIR to B | 1.7 | 7.3 | 2.0 | 5.2 | 1.5 | 5.1 | 0.6 | 4.2 | 1.1 | 4.8 | ns |
| $t_{en}$ | enable time | DIR to A | - | 13.0 | - | 9.0 | - | 8.5 | - | 7.2 | - | 7.6 | ns |
| | | DIR to B | - | 11.4 | - | 8.9 | - | 8.1 | - | 7.2 | - | 6.8 | ns |
| **$V_{CC(A)}$ = 3.0 V to 3.6 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 7.1 | 0.5 | 4.5 | 0.5 | 3.7 | 0.5 | 2.8 | 0.5 | 2.4 | ns |
| | | B to A | 1.0 | 6.1 | 0.6 | 3.6 | 0.5 | 3.1 | 0.5 | 2.6 | 0.5 | 2.4 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | ns |
| | | DIR to B | 1.7 | 7.2 | 0.7 | 5.5 | 0.6 | 5.5 | 0.7 | 4.1 | 1.7 | 4.7 | ns |
| $t_{en}$ | enable time | DIR to A | - | 13.3 | - | 9.1 | - | 8.6 | - | 6.7 | - | 7.1 | ns |
| | | DIR to B | - | 11.8 | - | 9.2 | - | 8.4 | - | 7.5 | - | 7.1 | ns |

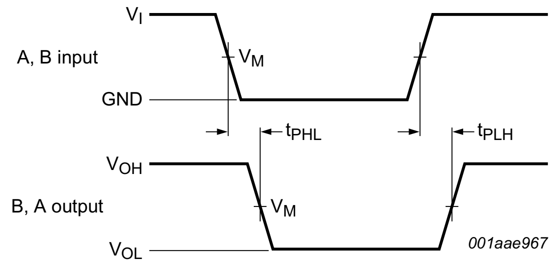
[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{en}$ is a calculated value using the formula shown in Section 13.4 "Enable times"

**Table 13. Dynamic characteristics for temperature range –40 °C to +125 °C [1]**
*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7*

| Symbol | Parameter | Conditions | $V_{CC(B)}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V ± 0.1 V | | 1.5 V ± 0.1 V | | 1.8 V ± 0.15 V | | 2.5 V ± 0.2 V | | 3.3 V ± 0.3 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| **$V_{CC(A)}$ = 1.1 V to 1.3 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 9.9 | 0.7 | 7.5 | 0.6 | 6.8 | 0.5 | 6.3 | 0.5 | 6.8 | ns |
| | | B to A | 1.0 | 9.9 | 0.8 | 8.8 | 0.7 | 8.5 | 0.6 | 8.0 | 0.5 | 7.9 | ns |
| $t_{dis}$ | disable time | DIR to A | 2.2 | 9.7 | 2.2 | 9.7 | 2.2 | 9.7 | 2.2 | 9.7 | 2.2 | 9.7 | ns |
| | | DIR to B | 2.2 | 9.2 | 1.8 | 7.4 | 2.0 | 7.6 | 1.7 | 6.9 | 2.4 | 8.0 | ns |
| $t_{en}$ | enable time | DIR to A | - | 19.1 | - | 16.2 | - | 16.1 | - | 14.9 | - | 15.9 | ns |
| | | DIR to B | - | 19.6 | - | 17.2 | - | 16.5 | - | 16.0 | - | 16.5 | ns |
| **$V_{CC(A)}$ = 1.4 V to 1.6 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 8.8 | 0.7 | 6.0 | 0.6 | 5.1 | 0.5 | 4.1 | 0.5 | 3.9 | ns |
| | | B to A | 1.0 | 7.5 | 0.8 | 6.0 | 0.7 | 5.7 | 0.6 | 5.2 | 0.5 | 5.0 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.6 | 7.0 | 1.6 | 7.0 | 1.6 | 7.0 | 1.6 | 7.0 | 1.6 | 7.0 | ns |
| | | DIR to B | 2.0 | 8.3 | 1.8 | 6.5 | 1.6 | 6.6 | 1.2 | 5.3 | 1.7 | 6.1 | ns |
| $t_{en}$ | enable time | DIR to A | - | 15.8 | - | 12.5 | - | 12.3 | - | 10.5 | - | 11.1 | ns |
| | | DIR to B | - | 15.8 | - | 13.0 | - | 12.7 | - | 11.1 | - | 10.9 | ns |
| **$V_{CC(A)}$ = 1.65 V to 1.95 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 8.5 | 0.6 | 5.7 | 0.5 | 4.8 | 0.5 | 3.8 | 0.5 | 3.5 | ns |
| | | B to A | 1.0 | 6.8 | 0.7 | 5.1 | 0.5 | 4.9 | 0.5 | 4.3 | 0.5 | 4.1 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.6 | 6.1 | 1.6 | 6.1 | 1.6 | 6.1 | 1.6 | 6.1 | 1.6 | 6.1 | ns |
| | | DIR to B | 1.8 | 8.6 | 1.8 | 6.3 | 1.4 | 6.4 | 1.0 | 5.0 | 1.5 | 5.8 | ns |
| $t_{en}$ | enable time | DIR to A | - | 15.4 | - | 11.4 | - | 11.3 | - | 9.3 | - | 9.9 | ns |
| | | DIR to B | - | 14.6 | - | 11.8 | - | 10.9 | - | 9.9 | - | 9.6 | ns |
| **$V_{CC(A)}$ = 2.3 V to 2.7 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 8.0 | 0.5 | 5.2 | 0.5 | 4.3 | 0.5 | 3.3 | 0.5 | 2.9 | ns |
| | | B to A | 1.0 | 6.3 | 0.6 | 4.2 | 0.5 | 3.8 | 0.5 | 3.3 | 0.5 | 3.1 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | ns |
| | | DIR to B | 1.7 | 8.0 | 2.0 | 5.8 | 1.5 | 5.7 | 0.6 | 4.7 | 1.1 | 5.3 | ns |
| $t_{en}$ | enable time | DIR to A | - | 14.3 | - | 10.0 | - | 9.5 | - | 8.0 | - | 8.4 | ns |
| | | DIR to B | - | 12.7 | - | 9.9 | - | 9.0 | - | 8.0 | - | 7.6 | ns |
| **$V_{CC(A)}$ = 3.0 V to 3.6 V** | | | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | A to B | 1.0 | 7.9 | 0.5 | 5.0 | 0.5 | 4.1 | 0.5 | 3.1 | 0.5 | 2.7 | ns |
| | | B to A | 1.0 | 6.8 | 0.6 | 4.0 | 0.5 | 3.5 | 0.5 | 2.9 | 0.5 | 2.7 | ns |
| $t_{dis}$ | disable time | DIR to A | 1.5 | 5.2 | 1.5 | 5.2 | 1.5 | 5.2 | 1.5 | 5.2 | 1.5 | 5.2 | ns |
| | | DIR to B | 1.7 | 7.9 | 0.7 | 6.0 | 0.6 | 6.1 | 0.7 | 4.6 | 1.7 | 5.2 | ns |
| $t_{en}$ | enable time | DIR to A | - | 14.7 | - | 10.1 | - | 9.6 | - | 7.5 | - | 7.9 | ns |
| | | DIR to B | - | 13.1 | - | 10.2 | - | 9.3 | - | 8.3 | - | 7.9 | ns |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{en}$ is a calculated value using the formula shown in Section 13.4 "Enable times"

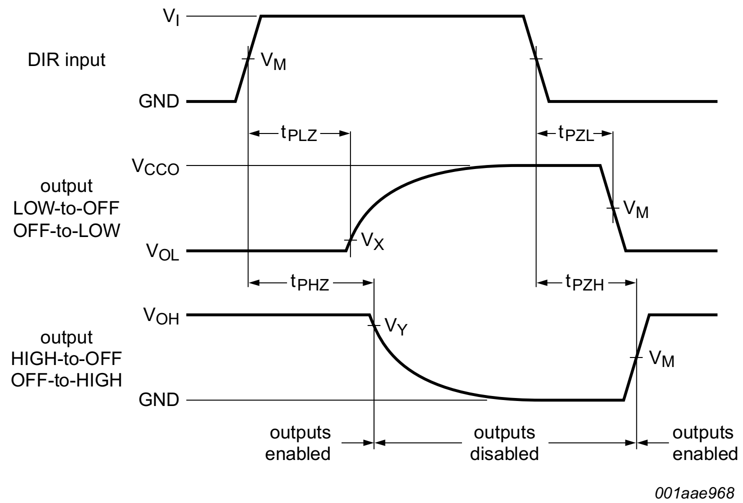
## 12. Waveforms




Measurement points are given in Table 14.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 6. The data input (A, B) to output (B, A) propagation delay times**




Measurement points are given in Table 14.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

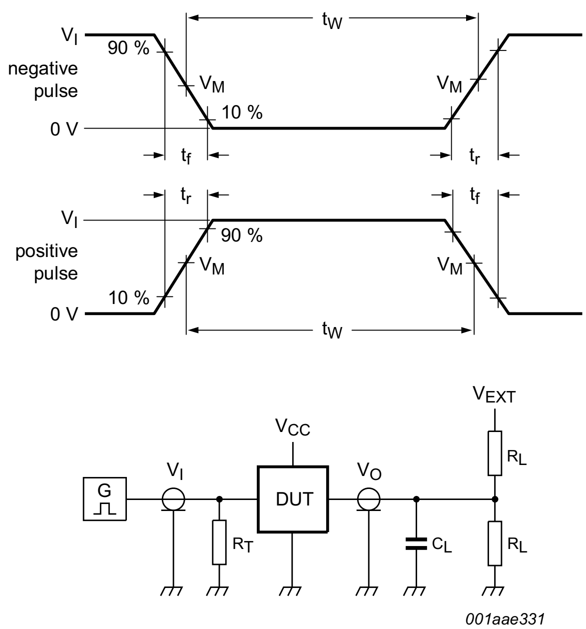
**Fig 7. Enable and disable times**

**Table 14. Measurement points**

| Supply voltage | Input[1] | Output[2] | | |
|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.1 V to 1.6 V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$ + 0.1 V | $V_{OH}$ − 0.1 V |
| 1.65 V to 2.7 V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ − 0.15 V |
| 3.0 V to 3.6 V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |

[1] $V_{CCI}$ is the supply voltage associated with the data input port.

[2] $V_{CCO}$ is the supply voltage associated with the output port.




Test data is given in Table 15.

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance.

$V_{EXT}$ = External voltage for measuring switching times.

**Fig 8. Test circuit for measuring switching times**

**Table 15. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $V_I$[1] | $\Delta t/\Delta V$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$[2] |
| 1.1 V to 1.6 V | $V_{CCI}$ | ≤ 1.0 ns/V | 15 pF | 2 kΩ | open | GND | $2V_{CCO}$ |
| 1.65 V to 2.7 V | $V_{CCI}$ | ≤ 1.0 ns/V | 15 pF | 2 kΩ | open | GND | $2V_{CCO}$ |
| 3.0 V to 3.6 V | $V_{CCI}$ | ≤ 1.0 ns/V | 15 pF | 2 kΩ | open | GND | $2V_{CCO}$ |

[1] $V_{CCI}$ is the supply voltage associated with the data input port.

[2] $V_{CCO}$ is the supply voltage associated with the output port.

# 13. Application information

## 13.1 Unidirectional logic level-shifting application

The circuit given in Figure 9 is an example of the 74AVCH1T45 being used in a unidirectional logic level-shifting application.

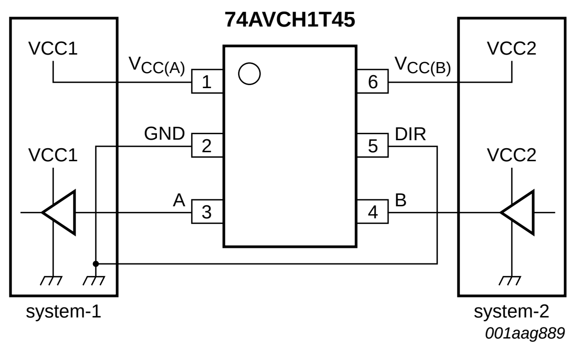



**Fig 9. Unidirectional logic level-shifting application**

**Table 16. Description unidirectional logic level-shifting application**

| Pin | Name | Function | Description |
|---|---|---|---|
| 1 | $V_{CC(A)}$ | $V_{CC1}$ | supply voltage of system-1 (0.8 V to 3.6 V) |
| 2 | GND | GND | device GND |
| 3 | A | OUT | output level depends on $V_{CC1}$ voltage |
| 4 | B | IN | input threshold value depends on $V_{CC2}$ voltage |
| 5 | DIR | DIR | the GND (LOW level) determines B port to A port direction |
| 6 | $V_{CC(B)}$ | $V_{CC2}$ | supply voltage of system-2 (0.8 V to 3.6 V) |

## 13.2 Bidirectional logic level-shifting application

Figure 10 shows the 74AVCH1T45 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.

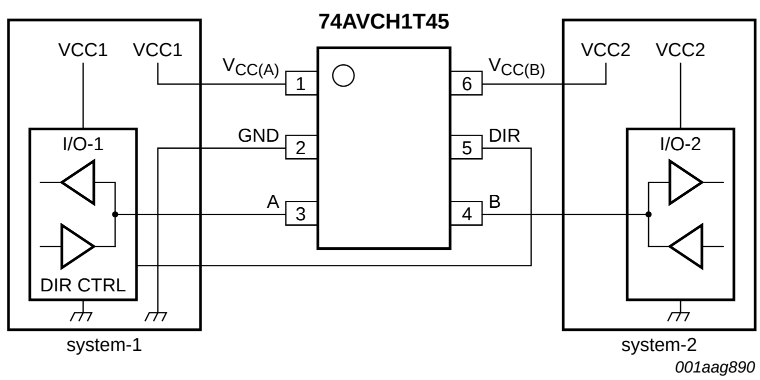



**Fig 10. Bidirectional logic level-shifting application**

Table 17 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

**Table 17. Description bidirectional logic level-shifting application[1]**

| State | DIR CTRL | I/O-1 | I/O-2 | Description |
|---|---|---|---|---|
| 1 | H | output | input | system-1 data to system-2 |
| 2 | H | Z | Z | system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold. |
| 3 | L | Z | Z | DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold. |
| 4 | L | input | output | system-2 data to system-1 |

[1] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

## 13.3 Power-up considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

**Table 18. Typical total supply current ($I_{CC(A)} + I_{CC(B)}$)**

| $V_{CC(A)}$ | $V_{CC(B)}$ | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 0 V | 0.8 V | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | |
| 0 V | 0 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | μA |
| 0.8 V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.7 | 2.3 | μA |
| 1.2 V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.3 | 1.4 | μA |
| 1.5 V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.9 | μA |
| 1.8 V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.5 | μA |
| 2.5 V | 0.1 | 0.7 | 0.3 | 0.1 | 0.1 | 0.1 | 0.1 | μA |
| 3.3 V | 0.1 | 2.3 | 1.4 | 0.9 | 0.5 | 0.1 | 0.1 | μA |

## 13.4 Enable times

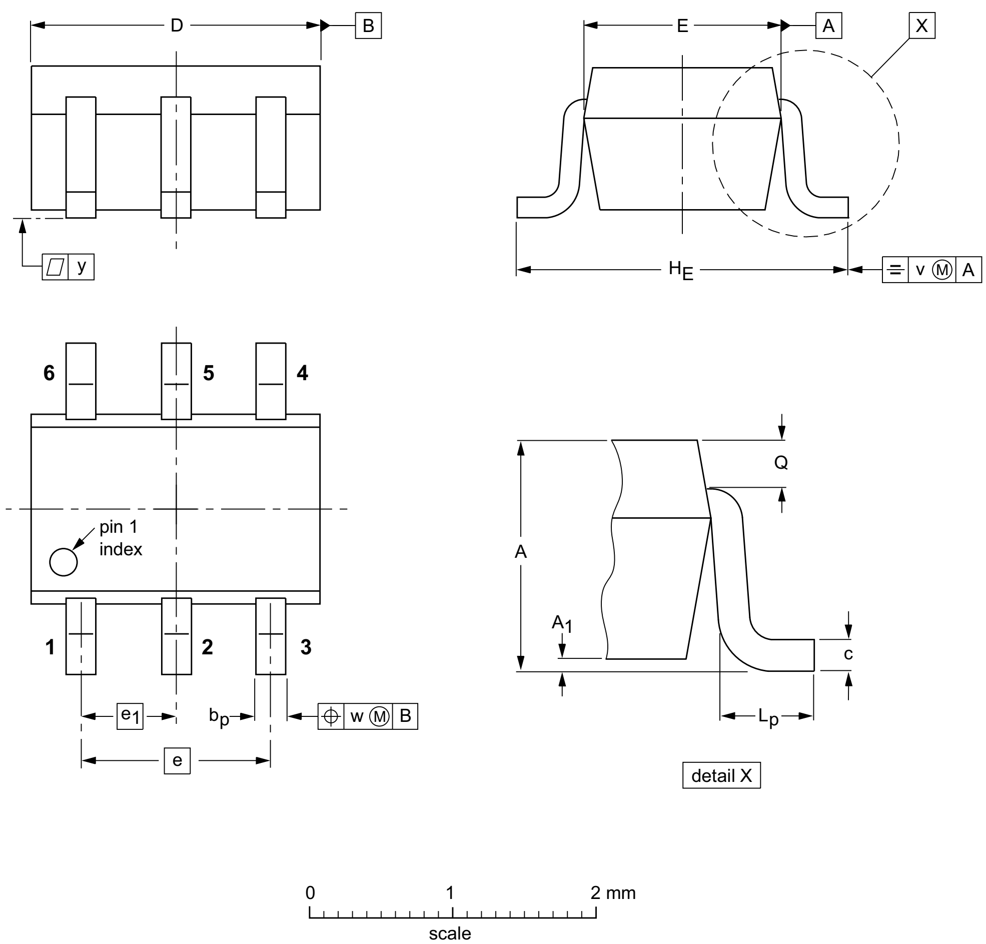
The enable times for the 74AVCH1T45 are calculate from the following formulas:

- $t_{en}$ (DIR to A) = $t_{dis}$ (DIR to B) + $t_{pd}$ (B to A)
- $t_{en}$ (DIR to B) = $t_{dis}$ (DIR to A) + $t_{pd}$ (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the 74AVCH1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

## 14. Package outline

**Plastic surface-mounted package; 6 leads** **SOT363**



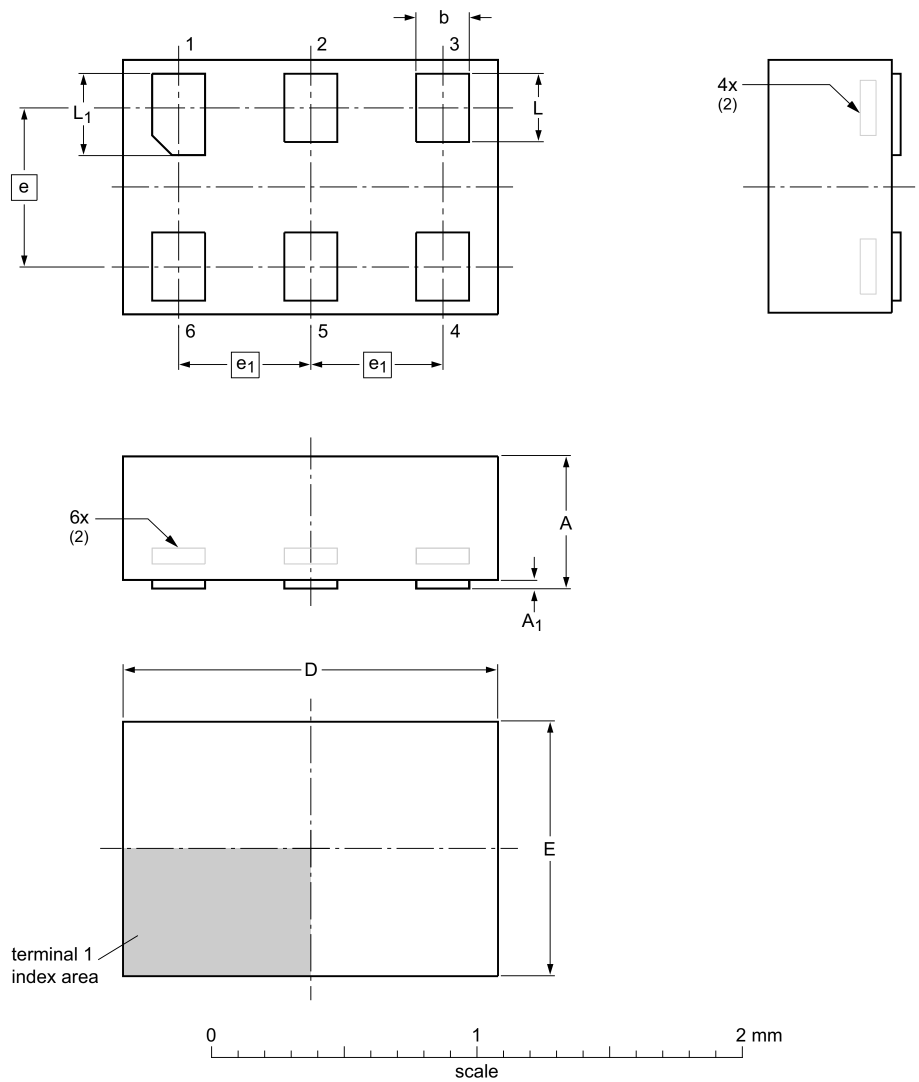

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ max | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.8 | 0.1 | 0.30<br>0.20 | 0.25<br>0.10 | 2.2<br>1.8 | 1.35<br>1.15 | 1.3 | 0.65 | 2.2<br>2.0 | 0.45<br>0.15 | 0.25<br>0.15 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT363 | | | SC-88 | | | ~~04-11-08~~<br>06-03-16 |

**Fig 11. Package outline SOT363 (SC-88)**

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886




Dimensions (mm are the original dimensions)

| Unit | | $A^{(1)}$ | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.5 | 0.04 | 0.25 | 1.50 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.20 | 1.45 | 1.00 | 0.6 | 0.5 | 0.30 | 0.35 |
| | min | | | 0.17 | 1.40 | 0.95 | | | 0.27 | 0.32 |

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

*sot886_po*

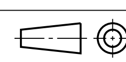
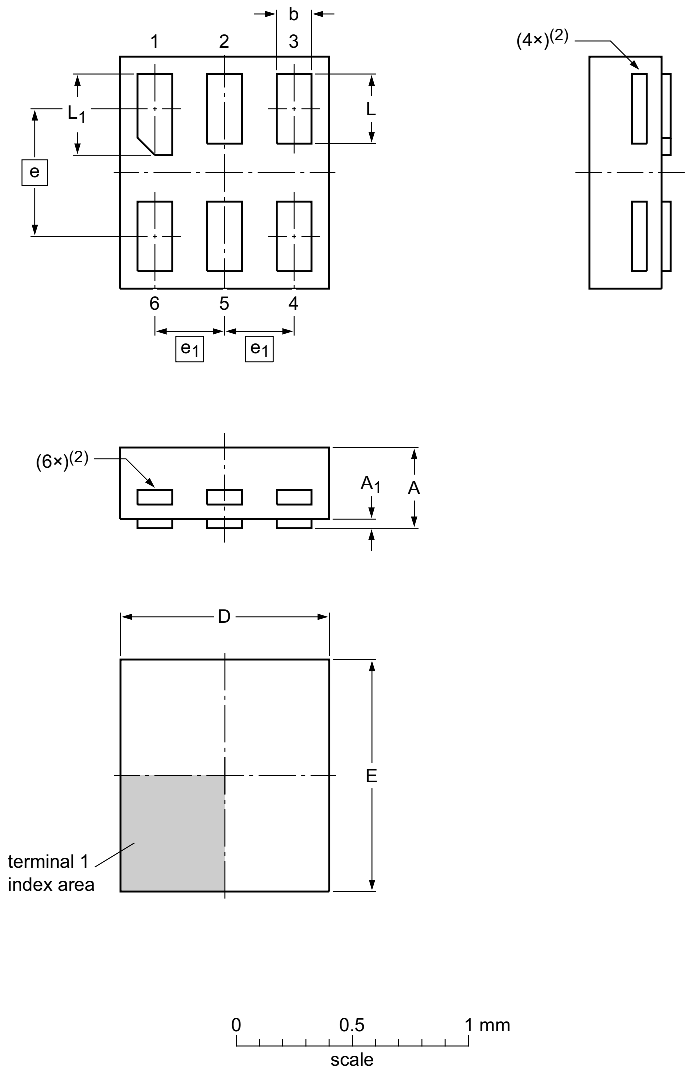
| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT886 | | MO-252 | | |  | ~~04-07-22~~ 12-01-05 |

**Fig 12. Package outline SOT886 (XSON6)**

**XSON6: extremely thin small outline package; no leads;**
**6 terminals; body 0.9 x 1.0 x 0.35 mm** **SOT1115**




Dimensions

| Unit | | $A^{(1)}$ | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | max | 0.35 | 0.04 | 0.20 | 0.95 | 1.05 | | | 0.35 | 0.40 |
| mm | nom | | | 0.15 | 0.90 | 1.00 | 0.55 | 0.3 | 0.30 | 0.35 |
| | min | | | 0.12 | 0.85 | 0.95 | | | 0.27 | 0.32 |

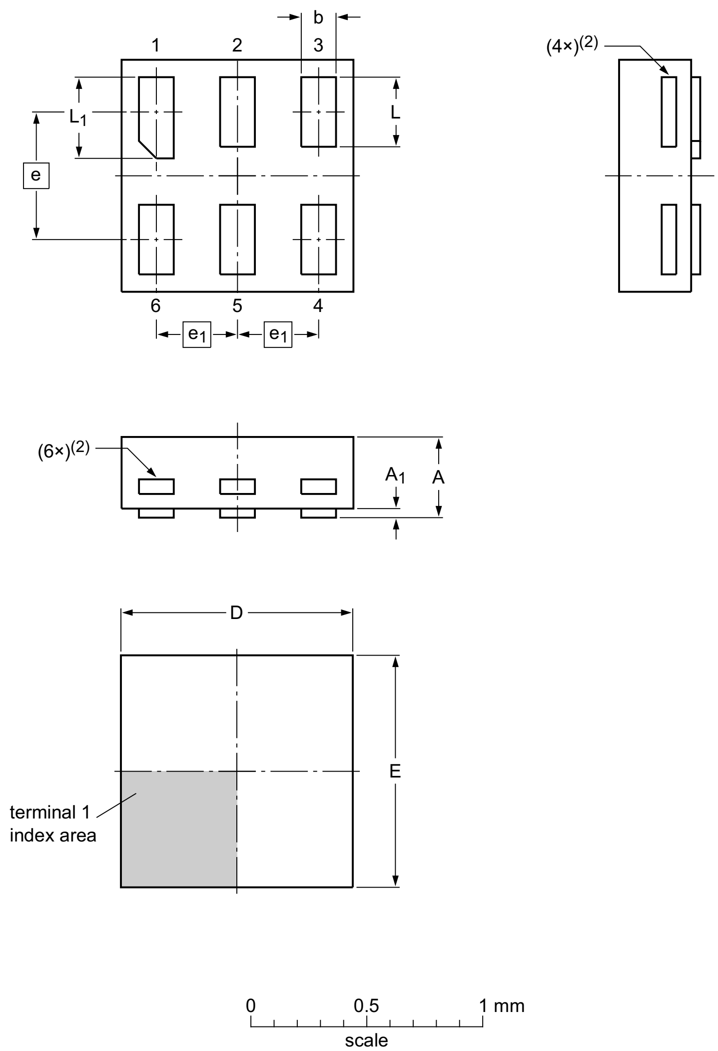
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1115 | | | | | | ~~10-04-02~~<br>10-04-07 |

**Fig 13. Package outline SOT1115 (XSON6)**

**XSON6: extremely thin small outline package; no leads;**
**6 terminals; body 1.0 x 1.0 x 0.35 mm** **SOT1202**




Dimensions

| Unit | | A(1) | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.35 | 0.04 | 0.20 | 1.05 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.15 | 1.00 | 1.00 | 0.55 | 0.35 | 0.30 | 0.35 |
| | min | | | 0.12 | 0.95 | 0.95 | | | 0.27 | 0.32 |

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

*sot1202_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1202 | | | | | | ~~10-04-02~~<br>10-04-06 |

**Fig 14. Package outline SOT1202 (XSON6)**

## 15. Abbreviations

**Table 19. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

## 16. Revision history

**Table 20. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AVCH1T45 v.5 | 20160106 | Product data sheet | - | 74AVCH1T45 v.4 |
| Modifications: | • Table 16: Labels for pins 4 and 5 corrected. | | | |
| 74AVCH1T45 v.4 | 20120803 | Product data sheet | - | 74AVCH1T45 v.3 |
| Modifications: | • Package outline drawing of SOT886 (Figure 12) modified. | | | |
| 74AVCH1T45 v.3 | 20111027 | Product data sheet | - | 74AVCH1T45 v.2 |
| Modifications: | • Added type number 74AVCH1T45GN (SOT1115/XSON6 package).<br>• Added type number 74AVCH1T45GS (SOT1202/XSON6 package). | | | |
| 74AVCH1T45 v.2 | 20090505 | Product data sheet | - | 74AVCH1T45 v.1 |
| 74AVCH1T45 v.1 | 20071025 | Product data sheet | - | - |

# 17. Legal information

## 17.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 19. Contents





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**Date of release: 06 January 2016**