



MP1917A

100V, 4A, High-Frequency Half-Bridge Gate Driver

DESCRIPTION

The MP1917A is a high-frequency, half-bridge, N-channel power MOSFET driver. Its low-side and high-side driver channels are controlled independently and matched with less than 5ns of time delay. Under-voltage lockout (UVLO) on both the high-side and low-side supplies forces the outputs low in the event that the supply is insufficient. The integrated bootstrap diode reduces the external component count.

The MP1917A is available in a QFN-10 (4mmx4mm) package.

FEATURES

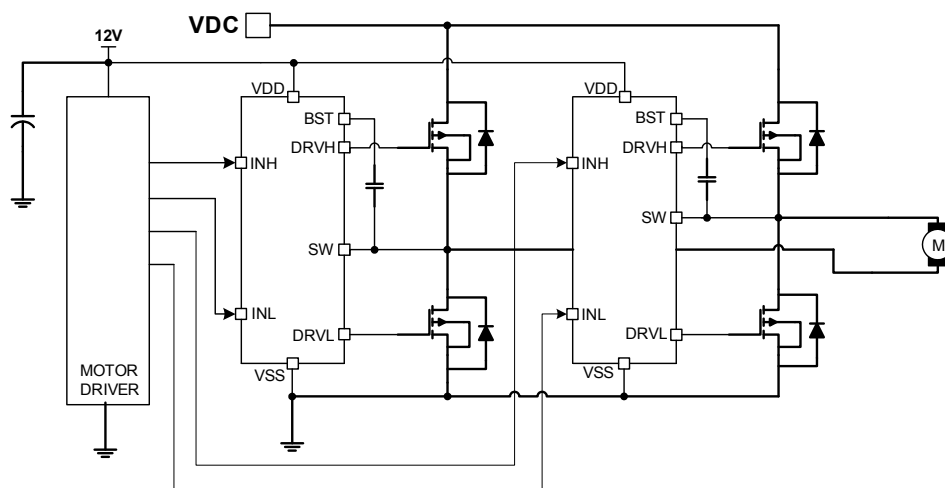
- Drives an N-Channel MOSFET Half-Bridge
- 115V Bootstrap Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Driver Matching of Less than 5ns
- Drives a 2.2nF Load with 15ns of Rise Time and 12ns of Fall Time at 12V VDD
- TTL-Compatible Input
- Quiescent Current of Less than 150μA
- UVLO for Both High-Side and Low-Side Gate Drivers
- QFN-10 (4mmx4mm) Package

APPLICATIONS

- Isolated Brick Power
- Telecom Half-Bridge Power Supplies
- Avionics DC/DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MP1917AGR*	QFN-10 (4mmx4mm)	See Below

* For Tape & Reel, add suffix –Z (e.g. MP1917AGR–Z).

TOP MARKING

MPSYWW

M1917A

LLLLLL

MPS: MPS prefix

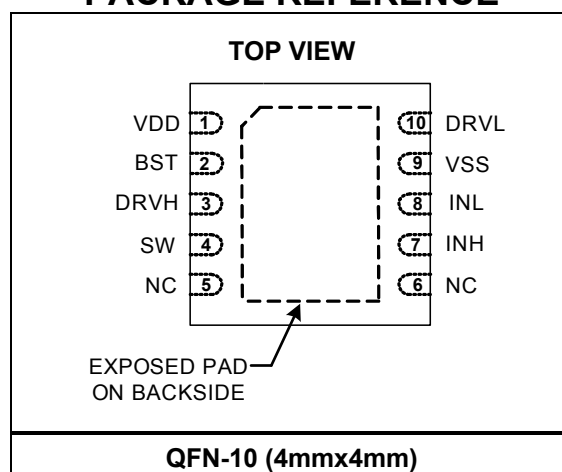
Y: Year code

WW: Week code

M1917A: First six digits of the part number

LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{DD})	-0.3V to 18V
SW voltage (V_{SW})	-1V (-18V for < 100nS) to 105V
BST voltage (V_{BST})	-0.3V to 115V
BST to SW	-0.3V to 18V
DRVH to SW	-0.3V (-2V for < 100nS) to (BST - SW) + 0.3V
DRVL to VSS	-0.3V (-2V for < 100nS) to (V_{DD} + 0.3V)
All other pins	-0.3V to (V_{DD} + 0.3V)
Continuous power dissipation ($T_A = 25^\circ\text{C}$) ⁽²⁾	
QFN-10 (4mmx4mm)	2.66W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 150°C

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{DD})	8.0V to 15.0V
SW voltage (V_{SW})	-1.0V to 98V
SW slew rate	<50V/ns
Operating junction temp (T_J)	-40°C to 125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-10 (4mmx4mm)	47	7

NOTES:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, no load at DRVH and DRVL, $T_A = +25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Currents						
VDD quiescent current	I _{DDQ}	INL = INH = 0		100	150	μA
VDD operating current	I _{DDO}	fsw = 500kHz		9		mA
Floating driver quiescent current	I _{BSTQ}	INL = INH = 0		60	90	μA
Floating driver operating current	I _{BSTO}	fsw = 500kHz		7.5		mA
Leakage current	I _{LK}	BST = SW = 100V		0.05	1	μA
Inputs						
INL/INH high				2	2.4	V
INL/INH low			1	1.4		V
INL/INH internal pull-down resistance	R _{IN}			185		kΩ
Under-Voltage Protection						
VDD rising threshold	V _{DDR}		6.4	6.8	7.2	V
VDD hysteresis	V _{DDH}			0.5		V
BST-SW rising threshold	V _{BSTR}		6.1	6.5	6.9	V
BST-SW hysteresis	V _{BSTH}			0.5		V
Bootstrap Diode						
Bootstrap diode VF at 100μA	V _{F1}			0.5		V
Bootstrap diode VF at 100mA	V _{F2}			0.95		V
Bootstrap diode dynamic R	R _D	At 100mA		2.5		Ω
Low-Side Gate Driver						
Low-level output voltage	V _{OLL}	I _O = 100mA		0.1		V
High-level output voltage to rail	V _{OHL}	I _O = -100mA		0.36		V
Source current ⁽⁵⁾	I _{OHL}	V _{DRVL} = 0V, V _{DD} = 12V		3		A
		V _{DRVL} = 0V, V _{DD} = 16V		4.7		A
Sink current ⁽⁵⁾	I _{OLL}	V _{DRVL} = V _{DD} = 12V		4.5		A
		V _{DRVL} = V _{DD} = 16V		6		A
Floating Gate Driver						
Low-level output voltage	V _{OLH}	I _O = 100mA		0.1		V
High-level output voltage to rail	V _{OHH}	I _O = -100mA		0.32		V
Source current ⁽⁵⁾	I _{OHH}	V _{DRVH} = 0V, V _{DD} = 12V		2.6		A
		V _{DRVH} = 0V, V _{DD} = 16V		4		A
Sink current ⁽⁵⁾	I _{OLH}	V _{DRVH} = V _{DD} = 12V		4.5		A
		V _{DRVH} = V _{DD} = 16V		5.9		A

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, no load at DRVH and DRVL, $T_A = +25^{\circ}C$, unless otherwise noted.

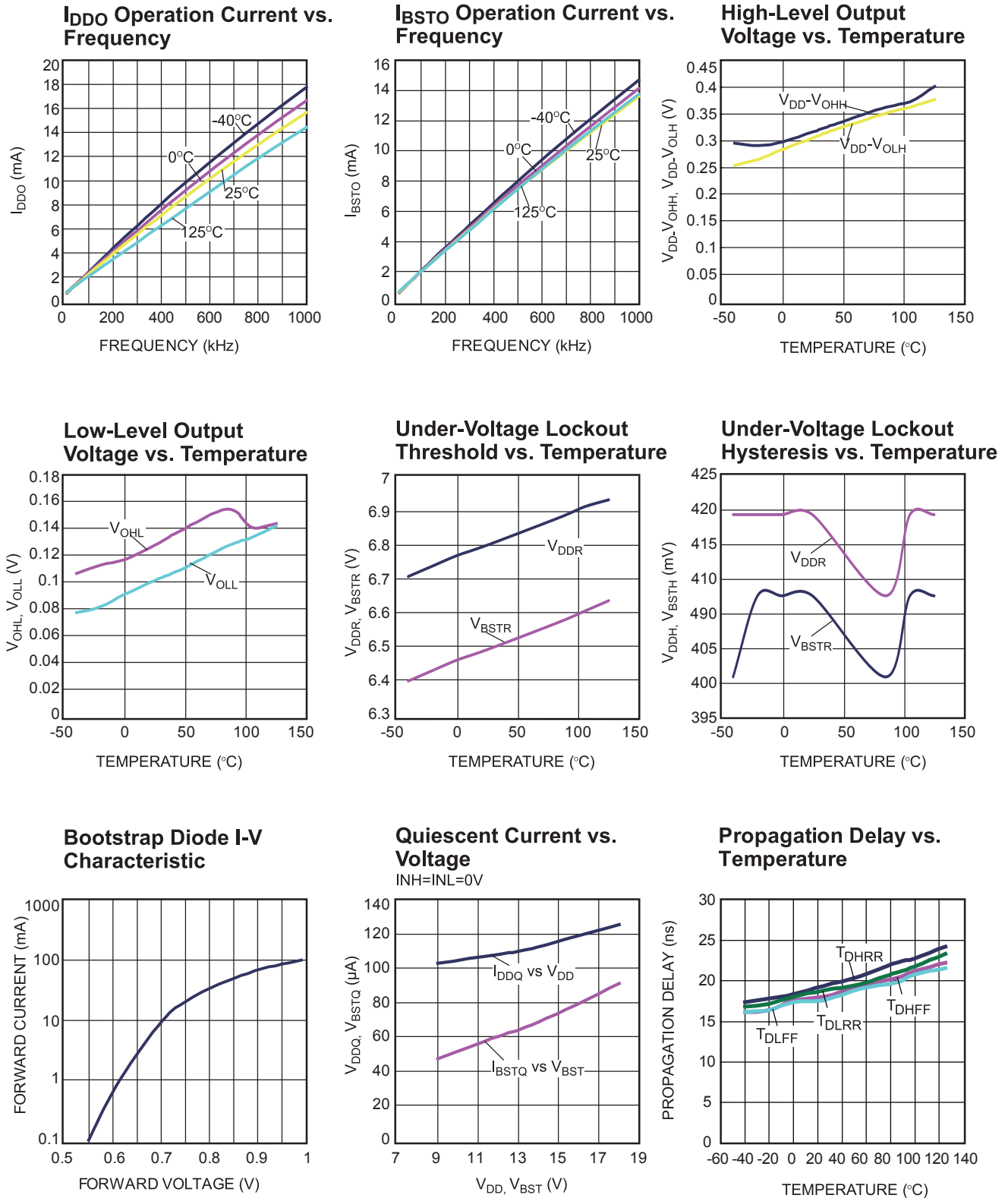
Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Specification – Low-Side Gate Driver						
Turn-off propagation delay INL falling to DRVL falling	T_{DLFF}			20		ns
Turn-on propagation delay INL rising to DRVL rising	T_{DLRR}			20		
DRVL rise time		$C_L = 2.2nF$		15		ns
DRVL fall time		$C_L = 2.2nF$		15		ns
Switching Specification – Floating Gate Driver						
Turn-off propagation delay INH falling to DRVH falling	T_{DHFF}			20		ns
Turn-on propagation delay INH rising to DRVH rising	T_{DHRR}			20		ns
DRVH rise time		$C_L = 2.2nF$		15		ns
DRVH fall time		$C_L = 2.2nF$		15		ns
Switching Specification – Matching						
Floating driver turn-off to low-side driver turn-on ⁽⁵⁾	T_{MON}			1	5	ns
Low-side driver turn-off to floating driver turn-on ⁽⁵⁾	T_{MOFF}			1	5	ns
Minimum input pulse width that changes the output ⁽⁵⁾	T_{PW}				50	ns
Bootstrap diode turn-on or turn- off time ⁽⁵⁾	T_{BS}			10		ns
Thermal shutdown				150		$^{\circ}C$
Thermal shutdown hysteresis				25		$^{\circ}C$

NOTE:

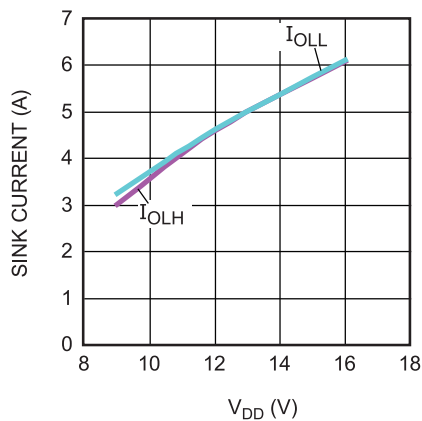
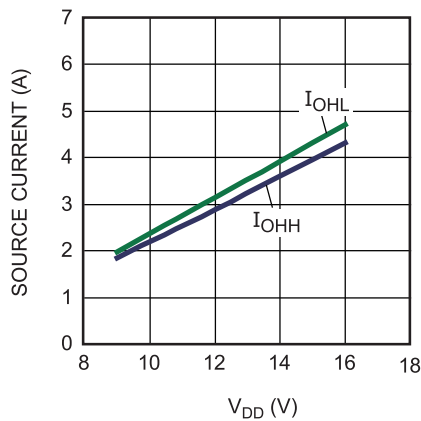
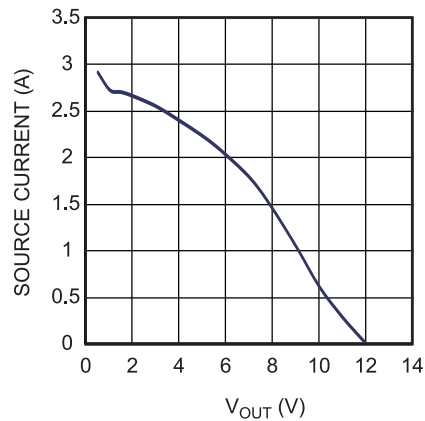
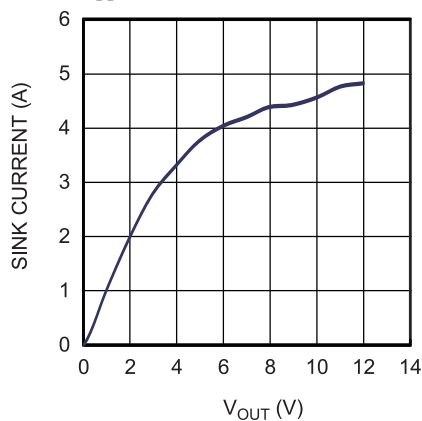
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.



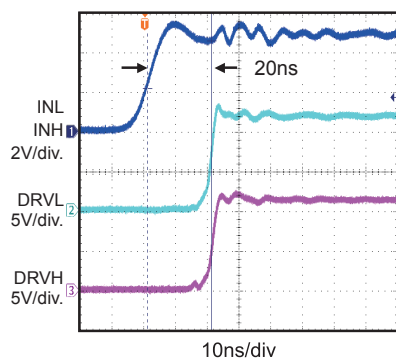
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

**Sink Current vs.
 V_{DD} Voltage**

**Source Current vs.
 V_{DD} Voltage**

**Source Current vs.
Output Voltage**
 $V_{DD} = 12V$

**Sink Current vs.
Output Voltage**
 $V_{DD} = 12V$


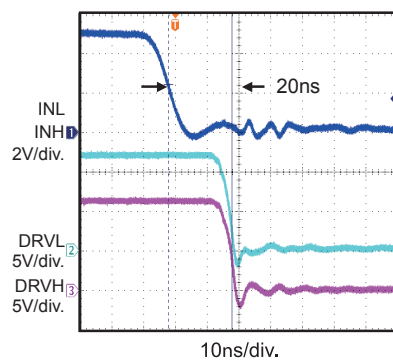
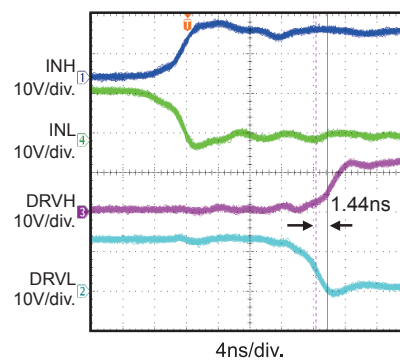
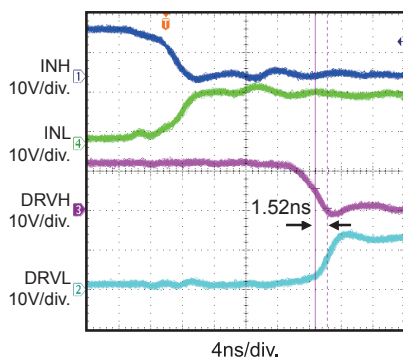
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^{\circ}C$, unless otherwise noted.

Turn-On Propagation Delay

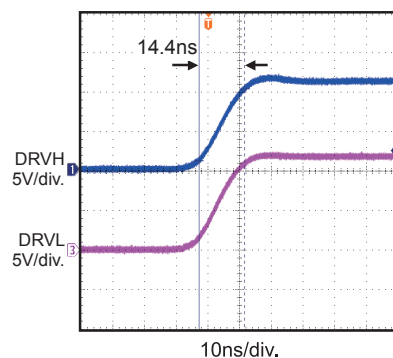


Turn-Off Propagation Delay


Gate Drive Matching T_{MOFF}

Gate Drive Matching T_{MON}


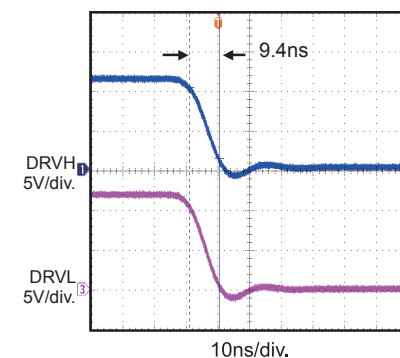
Drive Rise Time

2.2nF Load



Drive Fall Time

2.2nF Load



PIN FUNCTIONS

Pin #	Name	Description
1	VDD	Supply input. VDD supplies power to the internal circuitry. Place a decoupling capacitor on ground close to VDD to ensure a stable and clean supply.
2	BST	Bootstrap. Positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
3	DRVH	Floating driver output.
4	SW	Switching node.
5, 6	NC	No connection.
7	INH	Control signal input for the floating driver.
8	INL	Control signal input for the low-side driver.
9	VSS, exposed pad	Chip ground. Connect the exposed pad to VSS for proper thermal operation.
10	DRVL	Low-side driver output.

TIMING DIAGRAM

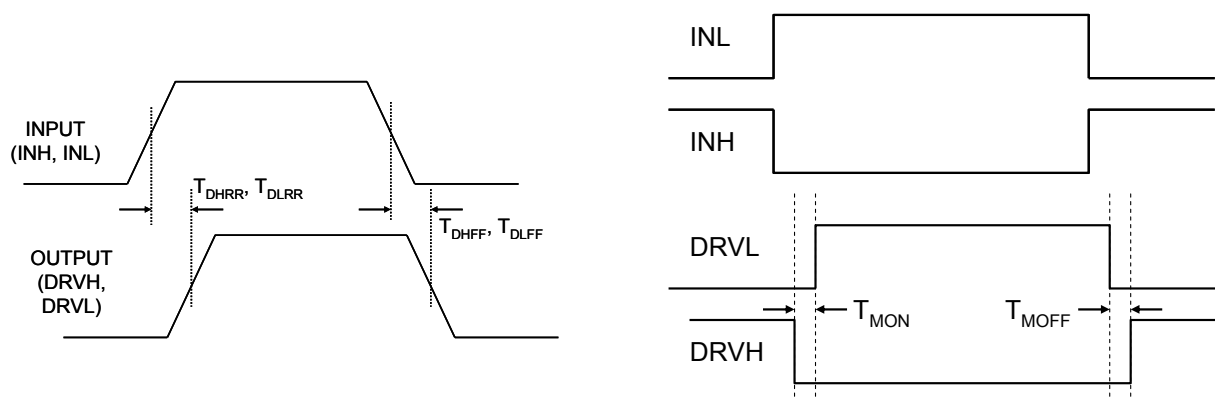


Figure 1: Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

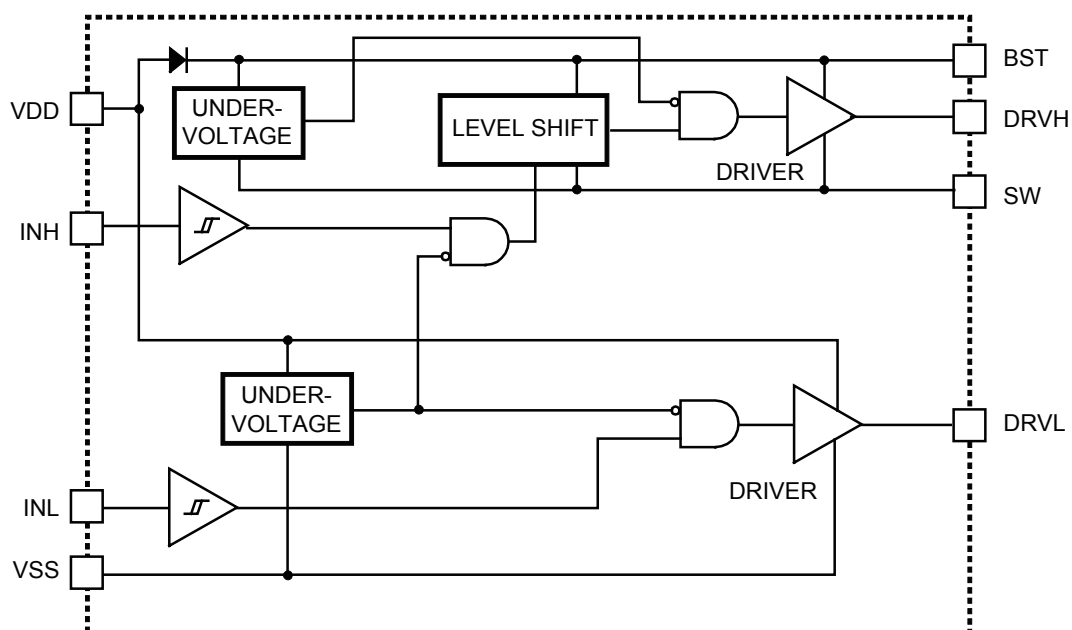


Figure 2: Functional Block Diagram

APPLICATION INFORMATION

The INH and INL input signals can be controlled independently. If both INH and INL control the high-side and low-side MOSFETs of the same bridge, set a sufficient dead time between INH

and INL low, and vice versa, to avoid shoot-through (see Figure 3). Dead time is defined as the time interval between INH low and INL low.

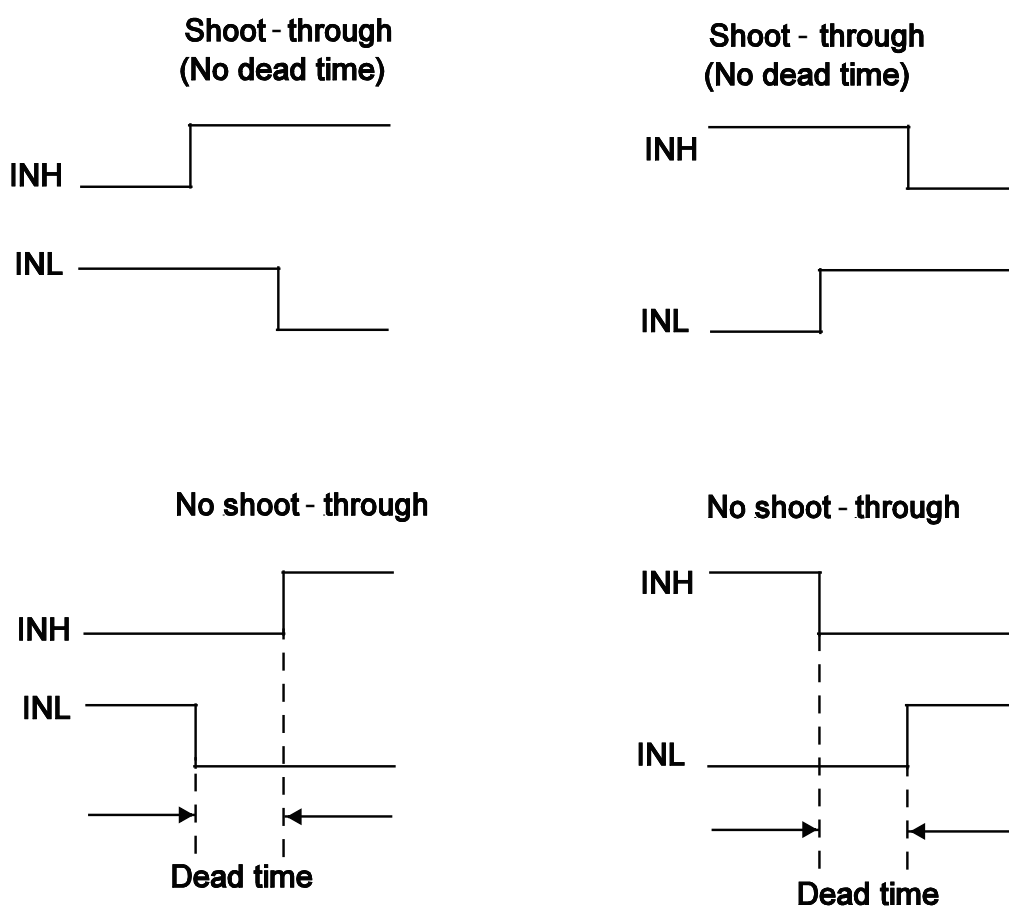


Figure 3: Shoot-Through Timing Diagram

Active Clamp Forward Converter

In active clamp forward converter topology, the MP1917A drives the MOSFETs with alternating signals. The high-side MOSFET, in conjunction with C_{reset} , is used to reset the power transformer with minimal power loss.

This topology is optimal for running at duty cycles exceeding 50%. The device may not be able to run at 100V under this topology (see Figure 6).

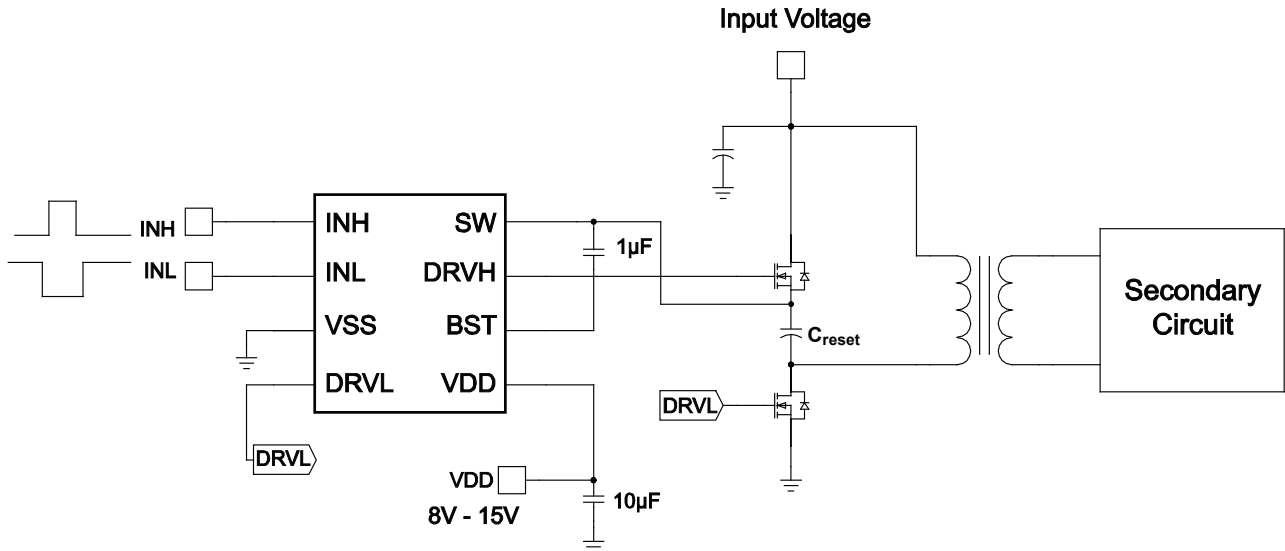
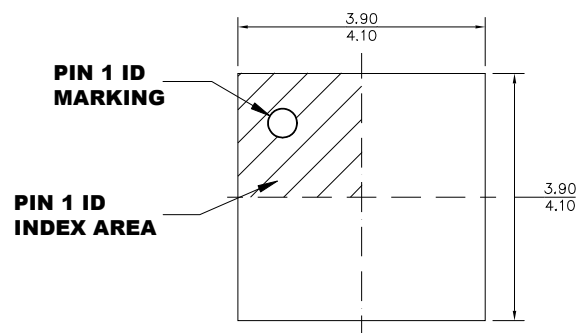


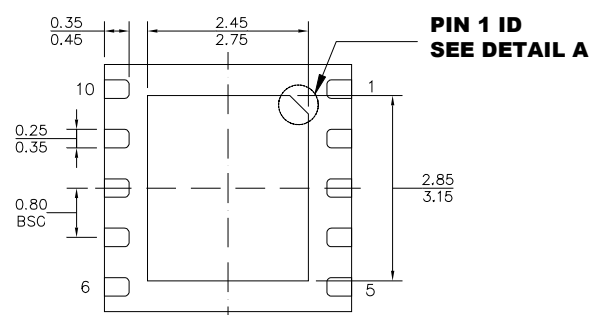
Figure 6: Active Clamp Forward Converter

PACKAGE INFORMATION

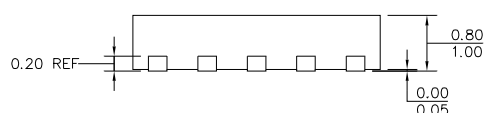
QFN-10 (4mmx4mm)



TOP VIEW

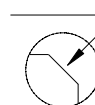


BOTTOM VIEW

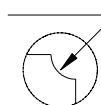


SIDE VIEW

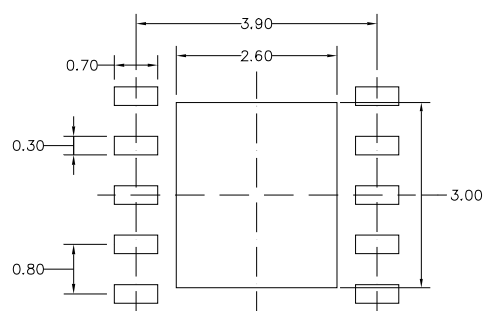
PIN 1 ID OPTION A
0.30x45° TYP.



PIN 1 ID OPTION B
R0.25 TYP.



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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