DDR4 SDRAM SODIMM Addendum

MTA18ASF2G72HBZ – 16GB

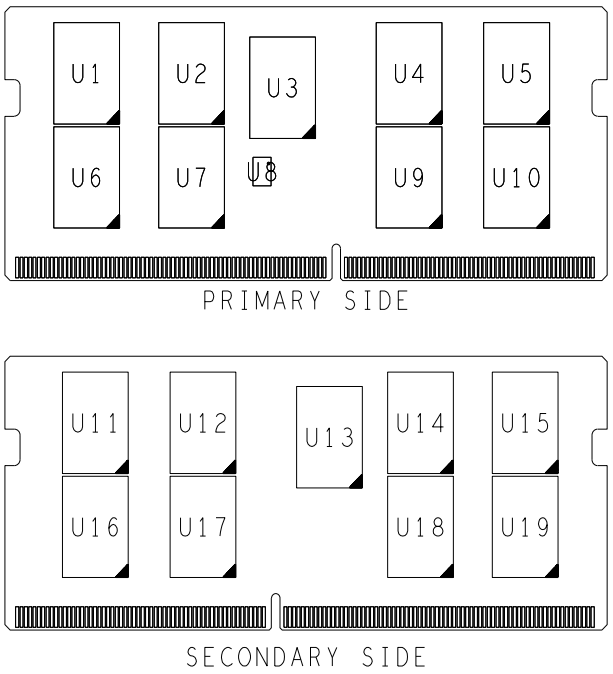
Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 SODIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 SODIMM Core data sheet
- 260-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rate: PC4-3200
- 16GB (2 Gig x 72)
- Data bus inversion (DBI) for data bus
- Supports ECC error detection and correction
- Dual-rank
- Onboard I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 260-Pin SODIMM



Options	Marking
• Operating temperature	
– Extended ($-40°C \le T_{OPER} \le 105°C$)	B
• Package	
– 260-pin DIMM (Green)	Z
• Frequency/CAS latency	
– 0.625ns @ CL = 22 (DDR4-3200)	-3G2

Table 1: Addressing

Parameter	16GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig x 8), 16 banks
Module rank address	CS_n[1:0]

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT40A1G8,[1] 8Gb DDR4 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)
MTA18ASF2G72HBZ-3G2__	16GB	2 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22

Notes:
1. The data sheet for the base device can be found on Micron's web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA18ASF2G72HBZ-3G2E1.

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DQ Maps

Table 3: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	11	42	U2	0	27	84
	1	8	28		1	25	71
	2	10	41		2	26	83
	3	9	29		3	24	70
	4	14	38		4	31	80
	5	12	24		5	29	67
	6	15	37		6	30	79
	7	13	25		7	28	66
U3	0	CB3	105	U4	0	34	187
	1	CB0	92		1	33	173
	2	CB2	101		2	35	186
	3	CB1	91		3	32	174
	4	CB6	100		4	39	182
	5	CB4	88		5	36	170
	6	CB7	104		6	38	183
	7	CB5	87		7	37	169
U5	0	51	229	U6	0	2	20
	1	49	215		1	0	8
	2	50	228		2	3	21
	3	48	216		3	1	7
	4	55	225		4	6	16
	5	53	212		5	4	4
	6	54	224		6	7	17
	7	52	211		7	5	3
U7	0	22	58	U9	0	42	207
	1	20	46		1	40	195
	2	23	59		2	43	208
	3	21	45		3	41	194
	4	18	62		4	46	203
	5	16	50		5	45	190
	6	19	63		6	47	204
	7	17	49		7	44	191

Table 3: Component-to-Module DQ Map, Front (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	59	250				
	1	57	236				
	2	58	249				
	3	56	237				
	4	63	246				
	5	61	233				
	6	62	245				
	7	60	232				

Table 4: Component-to-Module DQ Map, Back

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	49	215	U12	0	33	173
	1	51	229		1	34	187
	2	48	216		2	32	174
	3	50	228		3	35	186
	4	53	212		4	36	170
	5	55	225		5	39	182
	6	52	211		6	37	169
	7	54	224		7	38	183
U13	0	CB0	92	U14	0	25	71
	1	CB3	105		1	27	84
	2	CB1	91		2	24	70
	3	CB2	101		3	26	83
	4	CB4	88		4	29	67
	5	CB6	100		5	31	80
	6	CB5	87		6	28	66
	7	CB7	104		7	30	79

Table 4: Component-to-Module DQ Map, Back (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U15	0	8	28	U16	0	57	236
	1	11	42		1	59	250
	2	9	29		2	56	237
	3	10	41		3	58	249
	4	12	24		4	61	233
	5	14	38		5	63	246
	6	13	25		6	60	232
	7	15	37		7	62	245
U17	0	40	195	U18	0	20	46
	1	42	207		1	22	58
	2	41	194		2	21	45
	3	43	208		3	23	59
	4	45	190		4	16	50
	5	46	203		5	18	62
	6	44	191		6	17	49
	7	47	204		7	19	63
U19	0	0	8				
	1	2	20				
	2	1	7				
	3	3	21				
	4	4	4				
	5	6	16				
	6	5	3				
	7	7	17				

I_{DD} Specifications

Table 5: DDR4I_{DD} Specifications and Conditions – 16GB (Die Revision E)

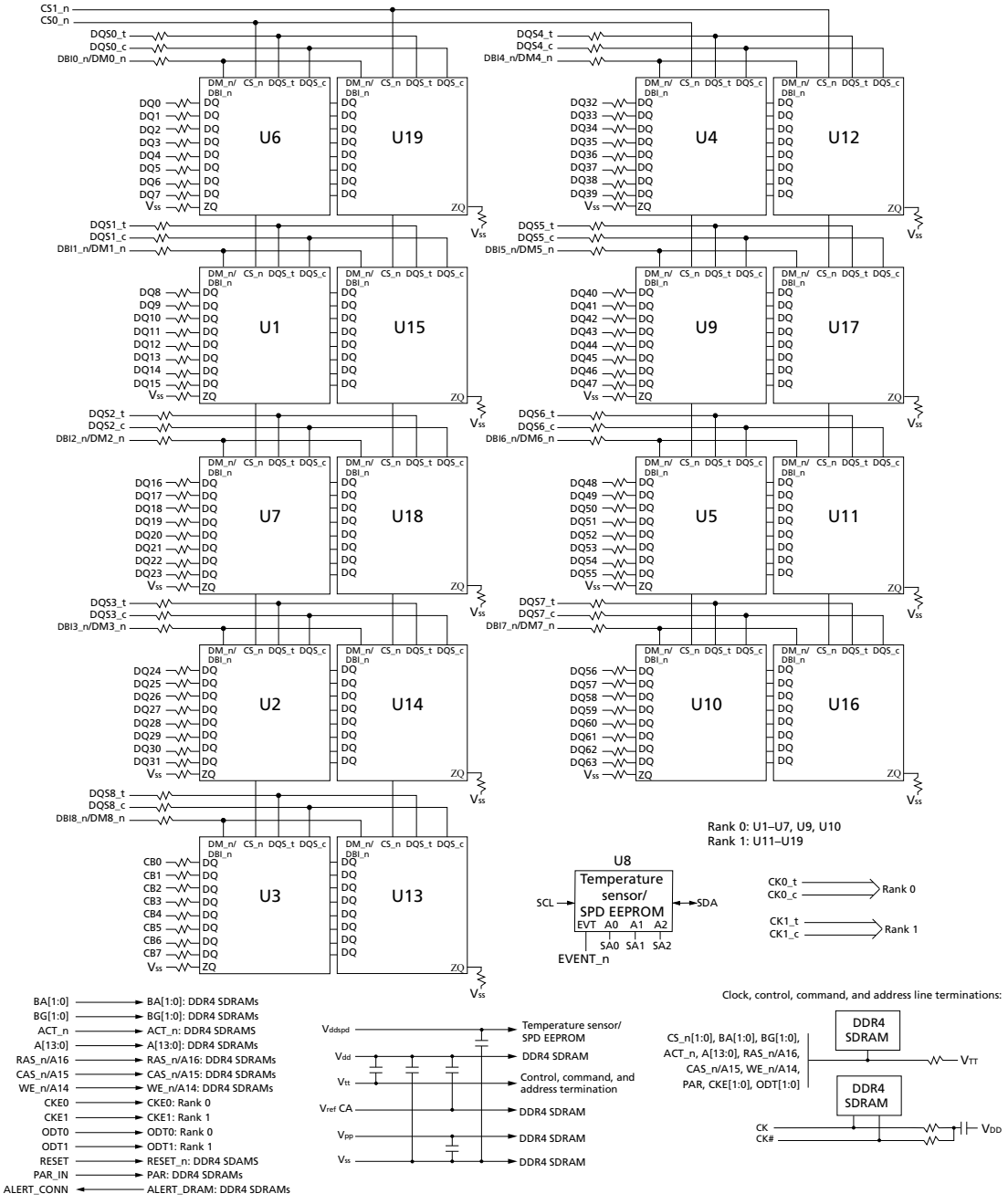
Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	693	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, IPP current	I_{PP0}[1]	54	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}[1]	837	mA
Precharge standby current	I_{DD2N}[2]	648	mA
Precharge standby ODT current	I_{DD2NT}[1]	666	mA
Precharge power-down current	I_{DD2P}[2]	468	mA
Precharge quite standby current	I_{DD2Q}[2]	522	mA
Active standby current	I_{DD3N}[2]	846	mA
Active standby I_{PP} current	I_{PP3N}[2]	54	mA
Active power-down current	I_{DD3P}[2]	666	mA
Burst read current	I_{DD4R}[1]	1935	mA
Burst write current	I_{DD4W}[1]	1674	mA
Burst refresh current (1x REF)	I_{DD5R}[1]	1134	mA
Burst refresh I_{PP} current (1x REF)	I_{PP5R}[1]	72	mA
Self refresh current: Normal temp range (0–85°C)	$I_{DD6N\ (0–85°C)}$[2]	612	mA
Self refresh current: Extended temp range (0–95°C)	$I_{DD6E\ (0–95°C)}$[2]	1710	mA
Self refresh current: Reduced temp range (0–45°C)	$I_{DD6R\ (0–45°C)}$[2]	378	mA
Auto self refresh current (25°C)	$I_{DD6A\ (25°C)}$[2]	155	mA
Auto self refresh current (45°C)	$I_{DD6A\ (45°C)}$[2]	378	mA
Auto self refresh current (75°C)	$I_{DD6A\ (75°C)}$[2]	558	mA
Auto self refresh current (95°C)	$I_{DD6A\ (95°C)}$[2]	1710	mA
Auto self refresh I_{PP} current	I_{PP6X}[2]	108	mA
Bank interleave read current	I_{DD7}[1]	1989	mA
Bank interleave read IPP current	I_{PP7}[1]	144	mA
Maximum Power Down Current	I_{DD8}[2]	360	mA

Notes:
1. One module rank in the active $I_{DD/PP}$, the other rank in $I_{DD2P/PP3N}$.
2. All ranks in this $I_{DD/PP}$ condition.

Functional Block Diagrams

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.