



5-BIT 2:1 MUX-LATCH

SY10E154
SY100E154

FEATURES

- 750ps max. LEN to output
- Extended 100E VEE range of -4.2V to -5.5V
- 700ps max. D to output
- Differential outputs
- Asynchronous Master Reset
- Dual latch-enables
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E154
- Available in 28-pin PLCC package

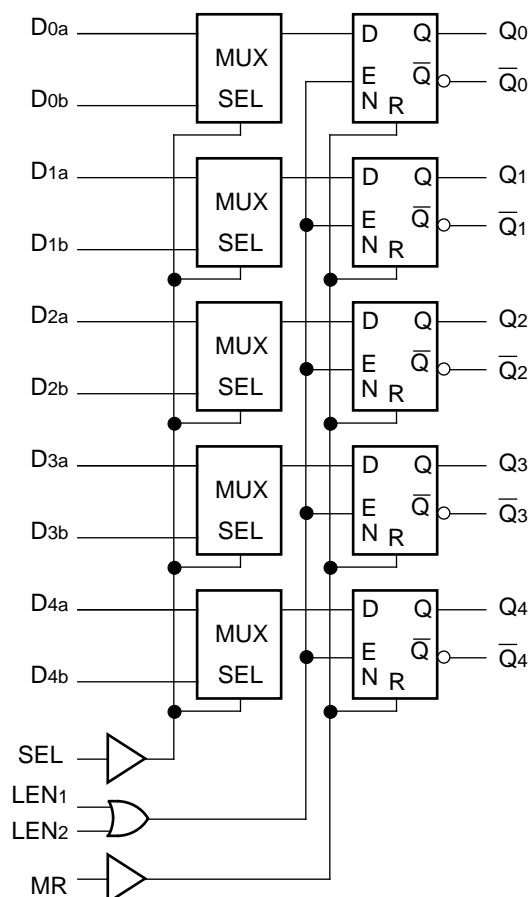
DESCRIPTION

The SY10/100E154 offer five 2:1 multiplexers followed by latches with differential outputs, designed for use in new, high-performance ECL systems. The two external Latch-Enable signals (LEN1, LEN2) are gated through a logical OR operation before use as control for the five latches. When both LEN1 and LEN2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN1 or LEN2 (or both) are at a logic HIGH, the outputs are latched.

The multiplexer operation is controlled by the SEL(Select) signal which selects one of the two bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to make all Q outputs go to a logic LOW.

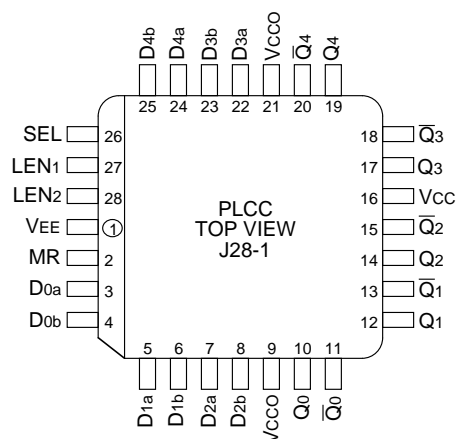
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0a-D4a	Input Data a
D0b-D4b	Input Data b
SEL	Data Select Input
LEN1, LEN2	Latch Enables
MR	Master Reset
Q0-Q4	True Outputs
Q0-Q4	Inverted Outputs
VCC0	VCC to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E154JC	J28-1	Commercial	SY10E154JC	Sn-Pb
SY10E154JCTR ⁽²⁾	J28-1	Commercial	SY10E154JC	Sn-Pb
SY100E154JC	J28-1	Commercial	SY100E154JC	Sn-Pb
SY100E154JCTR ⁽²⁾	J28-1	Commercial	SY100E154JC	Sn-Pb
SY10E154JZ ⁽³⁾	J28-1	Commercial	SY10E154JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E154JZTR ^(2, 3)	J28-1	Commercial	SY10E154JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E154JZ ⁽³⁾	J28-1	Commercial	SY100E154JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E154JZTR ^(2, 3)	J28-1	Commercial	SY100E154JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLES

SEL	Data
H	a
L	b

LEN ₁	LEN ₂	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	76	91	—	76	91	—	76	91		
	100E	—	76	91	—	76	91	—	87	105		

AC ELECTRICAL CHARACTERISTICS

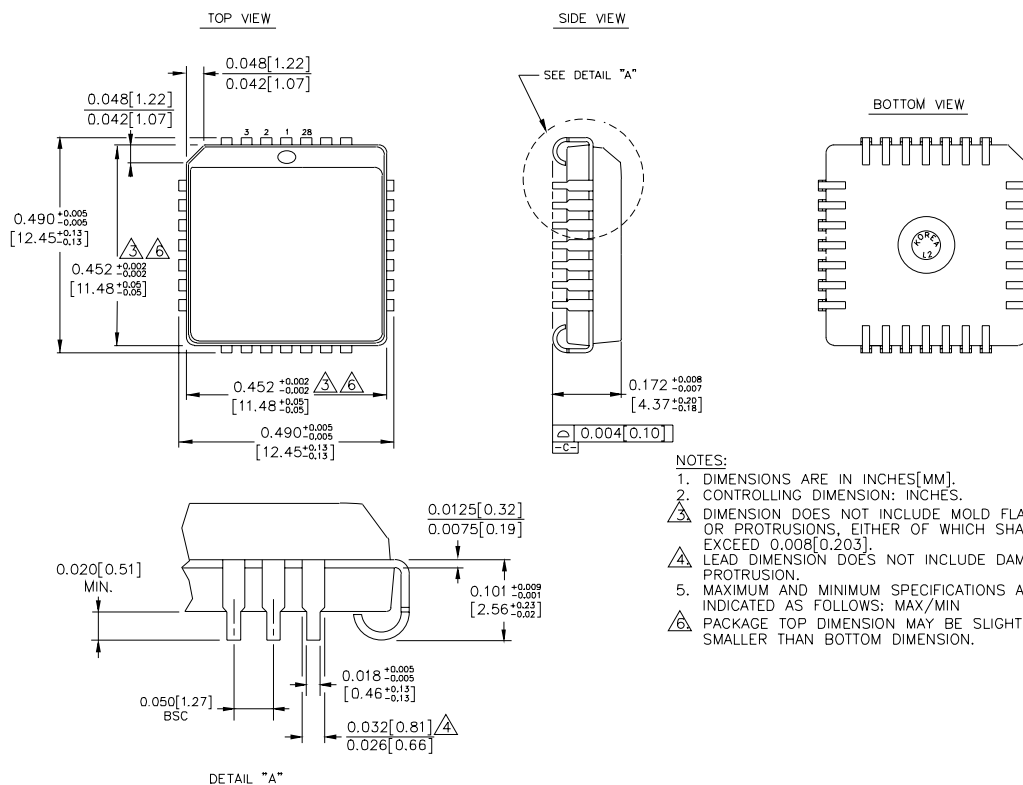
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PD}	Propagation Delay to Output D SEL LEN MR	325 475 350 450	500 650 500 600	700 925 750 800	325 475 350 450	500 650 500 600	700 925 750 800	325 475 350 450	500 650 500 600	700 925 750 800	ps	—
t _s	Set-up Time D SEL	300 500	100 250	— —	300 500	100 250	— —	300 500	100 250	— —	ps	—
t _H	Hold Time D SEL	300 200	–100 –250	— —	300 200	–100 –250	— —	300 200	–100 –250	— —	ps	—
t _{RR}	Reset Recovery Time	800	600	—	800	600	—	800	600	—	ps	—
t _{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	475	800	300	475	800	300	475	800	ps	—

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

28-PIN PLCC (J28-1)



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