Features

- Highly Integrated DAB Front-end Solution Covering Band III and L-band Reception
- Convenient Internal Clock Generation, Single Reference Clock
- Fractional PLL for VHF
- Fully Integrated VCOs
- High-precision Digitally Tunable Reference Oscillator
- Integrated High-performance LNAs
- Very Flexible Programming of the AGC
- Automatically Aligned External Filter Tuning
- Simple Three-wire Digital Control Interface for Easy Handling
- Single Low Voltage (3.3V) Supply Operation
- Low Current Consumption Due to Several Power-down Options
- Small SMD Package (QFN 9 mm × 9 mm)

Applications

- Commercial DAB Receivers
- DAB Receiver Solutions for Car Radio Applications
- Portable DAB Solutions

1. Description

The ATR2732N3 is a front-end monolithic integrated circuit, manufactured using Atmel®'s silicon-germanium BiCMOS process (SiGMOS).

The ATR2732N3 carries out all functions of RF and IF processing, as well as the clock-signal generation for these functions. Therefore, there is an integrated fractional PLL, which, equivalent to most of the other functions, can be controlled via an external digital bus. The RF functions include LNA, down-conversion mixing, amplifying, detection, and gain control. An external SAW filter is required in the signal path after the RF functions. Additional amplifiers with detection and control functions are integrated IF functions.

The device offers several tuning support functions, and was created to simplify the design and manufacturing process. To this end, the number of external components are minimal.

The part fits perfectly to Atmel's DAB baseband processor ATR2740.

Integrated DAB One-chip Front End

ATR2732N3

Summary

NOTE: This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

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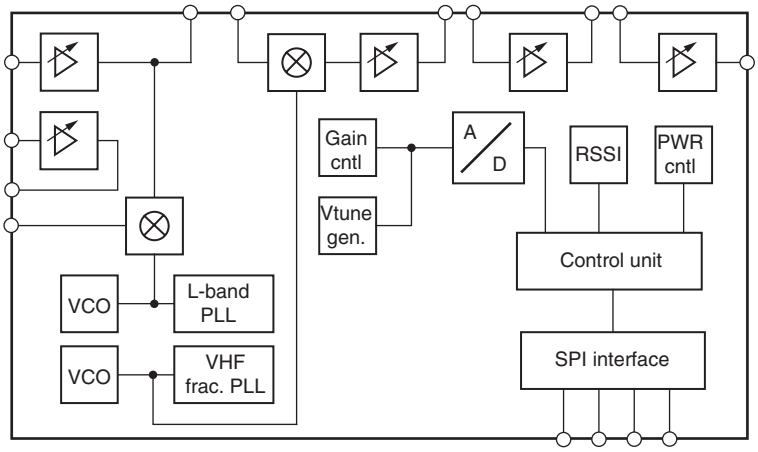
Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN64

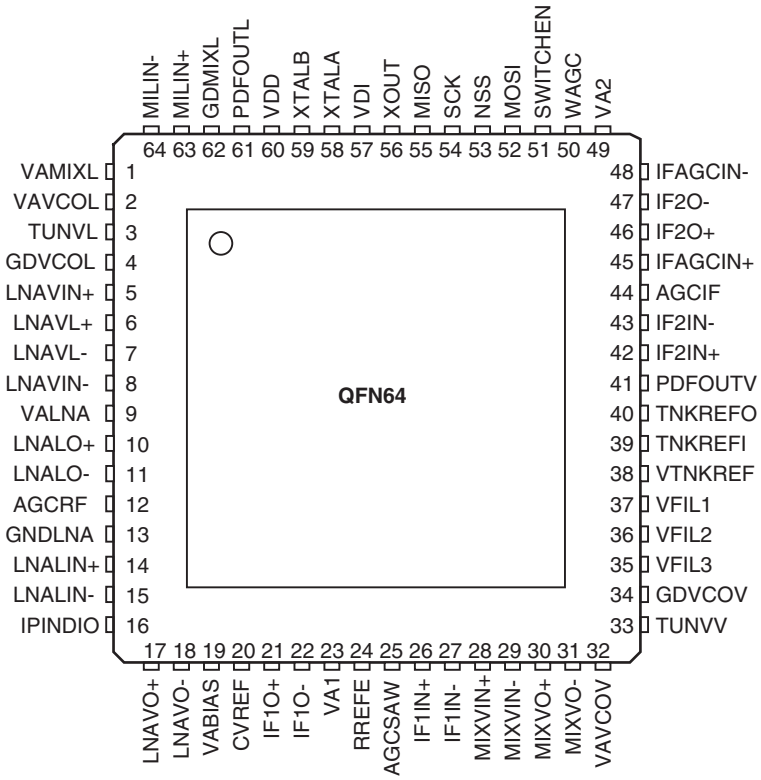


Table 2-1. Pin Description

Pin	Symbol	Function
1	VAMIXL	Supply voltage (mixer for L-band)
2	VAVCOL	Supply voltage (VCO for L-band)
3	TUNVL	Tuning voltage for integrated L-band VCO (connected to PLL loop filter)
4	GDVCOL	Ground (L-band VCO)
5	LNAVIN+	Input for VHF LNVGA (differential with pin 8)
6	LNAVL+	Connection for degeneration coil (inductance) to GNDLNA for VHF LNVGA
7	LNAVL–	Connection for degeneration coil (inductance) to GNDLNA for VHF LNVGA
8	LNAVIN–	Input for VHF LNVGA (differential with pin 5)
9	VALNA	Supply voltage for LNVGAs
10	LNALO+	(Differential) output for L-band LNVGA
11	LNALO–	(Differential) output for L-band LNVGA
12	AGCRF	Connection for time-constant capacitor of RF AGC (LNVGAs, external PIN diode)
13	GNDLNA	Ground for LNVGAs
14	LNALIN+	(Differential) input for L-band LNVGA
15	LNALIN–	(Differential) input for L-band LNVGA
16	IPINDIO	Current output to external PIN diode for additional attenuation of incoming signal (optional)
17	LNAVO+	(Differential) output of VHF LNVGA and/or mixer for L-band
18	LNAVO–	(Differential) output of VHF LNVGA and/or mixer for L-band
19	VABIAS	Supply voltage for (internal) voltage and current bias reference circuits
20	CVREF	Connection for capacitor for filtering internal voltage/current reference circuits (capacitor to VABIAS)
21	IF1O+	(Differential) Output of IFVGA1
22	IF1O–	(Differential) Output of IFVGA1
23	VA1	Supply voltage
24	RREFE	Connection for current reference resistor (resistor to ground)
25	AGCSAW	Connection for AGC time-constant capacitor of the VHF mixer
26	IF1IN+	(Differential) Input of 1st IFVGA
27	IF1IN–	(Differential) Input of 1st IFVGA
28	MIXVIN+	(Differential) Input of VHF mixer
29	MIXVIN–	(Differential) Input of VHF mixer
30	MIXVO+	(Differential) Output of VHF mixer
31	MIXVO–	(Differential) Output of VHF mixer
32	VAVCOV	Supply voltage (VHF VCO)
33	TUNVV	Tuning voltage for integrated VHF VCO (connected to PLL loop filter)
34	GDVCOV	Ground (VHF VCO)
35	VFIL3	Voltage outputs for frequency tuning of VHF filters: antenna filter, preselection filter
36	VFIL2	Voltage outputs for frequency tuning of VHF filters: antenna filter, preselection filter
37	VFIL1	Voltage outputs for frequency tuning of VHF filters: antenna filter, preselection filter
38	VTNKREF	Output voltage for tuning the reference tank (-varactor)
39	TNKREFI	Reference-tank connection for to generate the tuning voltages for the external VHF filters (varactors)
40	TNKREFO	Reference-tank connection for to generate the tuning voltages for the external VHF filters (varactors)

Table 2-1. Pin Description (Continued)

Pin	Symbol	Function
41	PFDOUTV	Output-of-phase comparator for VHF VCO (connected to PLL loop filter)
42	IF2IN+	(Differential) Input of 2nd IFVGA
43	IF2IN–	(Differential) Input of 2nd IFVGA
44	AGCIF	Connection for time-constant capacitor of IFVGAs' AGC
45	IFAGCIN+	Input of IFAGC detector (differential with pin 48)
46	IF2O+	(Differential) Output of 2nd IFVGA
47	IF2O–	(Differential) Output of 2nd IFVGA
48	IFAGCIN–	Input of IFAGC detector (differential with pin 45)
49	VA2	Supply voltage
50	WAGC	Window AGC input: All AGCs frozen and currents to capacitors switched off (necessary during Null Symbol or when unused symbols are left out and the part is powered down using the SWITCHEN input)
51	SWITCHEN	Input for selection between the two enable registers, allowing a fast change between reduced, low-current, and normal-reception mode, and offering current-saving capability
52	MOSI	Input of SPI bus (data, refer to SPI bus protocol)
53	NSS	Input of SPI bus (chip select, refer to SPI bus protocol)
54	SCK	Input of SPI bus (clock, refer to SPI bus protocol)
55	MISO	Output of SPI bus (data, refer to SPI bus protocol)
56	XOUT	Crystal oscillator clock output to baseband If used: AC-couple to baseband (single VCXO concept) If not used: short-circuit to GND
57	VDI	Supply voltage from baseband (1.65V to 3.6V) to adaptation interface to baseband
58	XTALA	Connection for reference clock crystal
59	XTALB	Connection for reference clock crystal
60	VDD	Supply for digital circuits
61	PFDOUTL	Output of phase comparator for VCO for L-band (connected to PLL loop filter)
62	GDMIXL	Ground (L-band mixer)
63	MILIN+	(Differential) Input of L-band mixer
64	MILIN–	(Differential) Input of L-band mixer
Paddle	GND	Ground

3. Functional Description

The ATR2732N3 front-end IC was developed as a tuner IC for DAB reception. It was designed for operation in L-band (1452 MHz to 1492 MHz) and VHF BIII (167 MHz to 240 MHz). The front end contains gain-controlled LNAs, an L-band mixer with a corresponding PLL, and a VHF-band mixer with a fractional PLL. The IF path contains three gain-controlled amplifiers. The front-end IC allows the use of automatic tuning, which contains an adjustable input filter for VHF BIII and an adjustable preselection filter for L-band and VHF reception.

The high dynamic range of the RF inputs, the use of gain-controlled amplifiers and gain-controlled mixers in the RF and IF path, and an integrated driver for an external PIN diode attenuator (VHF band) offer the possibility of handling even strong RF input signals.

The RF and IF parts include AGC functional blocks, which are needed for proper operation. The thresholds are programmable via a simple serial bus.

The SPI bus is used to adjust and control all functional blocks.

The following sections briefly describe the major functions and features.

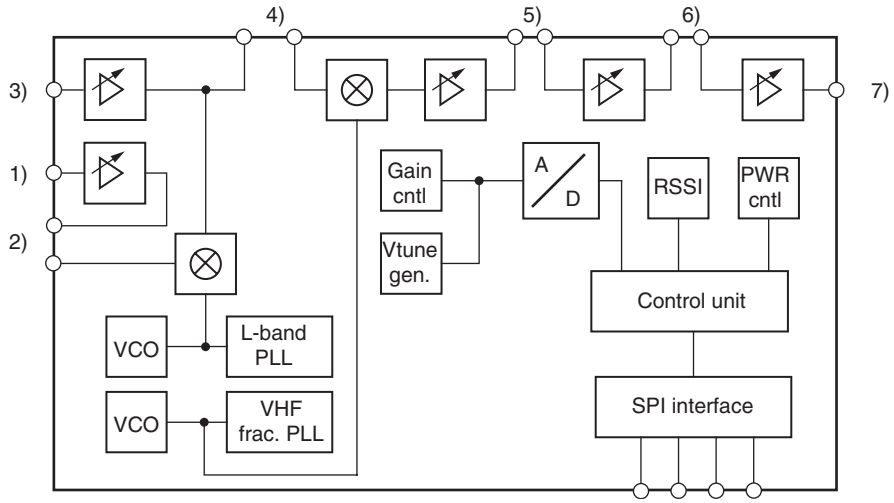
3.1 Main Functions

The following description gives a short overview of the general signal flow using the ATR2732N3 front-end IC for reception of DAB signals. Numbers in the text refer to the numbers in Figure 3-1 on page 6.

A DAB signal in the L-band frequency range (1452 MHz to 1492 MHz) is received by the L-band antenna; a separate LNA with a separate input is available for the VHF Band III signals. In both cases, the signal is band-pass filtered using a filter with low insertion loss. The internal variable gain LNA (for L-band (1), for Band III (3)) amplifies the signal. For the L-band reception, a second band-pass filter is placed between the LNA output and mixer input at (2). This mixer converts the L-band signal to the VHF BIII frequency range (167 MHz to 240 MHz). The signal leaves the IC at point (4), followed by an external preselection filter.

This filter has an automatic tuner adjustment; that is, the tuning-voltage-generation block adjusts the pass band of this filter to the desired frequency. After passing this filter, the RF signal is down-mixed to a fixed IF frequency of 38.912 MHz. The IF signal is amplified and passed to a SAW filter (5). The first IF variable-gain amplifier is followed by an IF filter at position (6). This filter is used as an anti-alias-filter. Finally, the DAB signal is amplified using the 2nd IF amplifier. The signal leaves the front-end IC at (7), giving the signal to the DAB baseband IC.

Figure 3-1. Functional Block Diagram with Labelled Inputs and Outputs



3.2 AGC in General

There are three AGCs in the ATR2732N3, one for the RF signals (around the LNAs) (1) and (3), one for the very beginning of the IF path (mainly VHF mixer), and one for the IF amplifiers (5) down to the output to baseband (7).

In these AGCs, the output signals of the relevant blocks are amplified, weakly band-pass filtered, rectified, and, finally, low-pass filtered. The voltage derived in this power-measurement process is compared to a voltage threshold which can be digitally controlled by several bits, independently of each other. The setting is done via the control bus. Depending on the result of this comparison, charge pumps feed a positive or negative current in order to charge or discharge external capacitors. The voltage of these external capacitors is used to control the gains of practically all blocks in the signal path.

By means of the control bus, the current of the AGC charge pump can be selected as specified in the following table:

Table 3-1. Selection of Time Constant Factor

MSB		LSB	Time Constant Factor
0	0	0	Infinite
0	0	1	32
0	1	0	16
0	1	1	8
1	0	0	4
1	0	1	2
1	1	0	1
1	1	1	0.2

The input pin WAGC, set to logical 1, always sets all AGCs to time constant *Infinite* (meaning there is practically no current to the AGC capacitors), regardless of the actual status of the bus settings.

3.3 Device Support Functions

The ATR2732N3 has incorporated some very useful additional functions for handling the device and optimizing the performance. First of all, a very precise clocking engine is incorporated. To optimize the performance of this front end, a tuning support for alignment of the filters is featured by this part too, similar to Atmel's other radio front ends.

3.4 Tuning Support Functions

The ATR2732N3 includes three operational amplifiers, and three programmable digital-analog converters (DACs). These outputs are used for automatic filter alignment of the tunable VHF antenna filter and the preselection filter. DACs are incorporated in the ATR2732N3 for this tuning-support function.

For more details about the usage of the filter-tuning function contact your local Atmel sales office and ask for the application note covering this feature.

3.5 DAC Usage

There are two DAC modes: pure DAC and Loop/Offset mode. In the pure DAC mode the DAC sets a definite value. In the Loop/Offset mode the filter tuning voltage is derived from a reference tank circuit (inductor plus varicap). An offset value can be added to this voltage. This Loop/Offset mode is the most useful mode and recommended for most applications. Temperature compensation is also included in this mode.

3.6 RSSI Measurement

The ATR2732N3 offers the option of getting information about the field strength. This is not an absolute real-field-strength value, but an indication of in which range the field strength is available. This information can be obtained from the 8 low bits of the status register.

3.7 Clocking Engine in General

The ATR2732N3 incorporates a convenient and flexible clocking engine. This includes VCOs and PLLs for both bands, as well as a reference oscillator which can be precisely tuned using the SPI interface. Together, this results in low external component count, but offers high flexibility and convenience.

3.8 PLL Part

The two PLL parts, the L-band PLL and the Band III PLL, perform phase lock of the LO signal to an on-chip crystal reference oscillator. The Band III PLL incorporates a fractional part. This technique allows operation with an increased bandwidth of the PLL, which results in improved phase noise.

3.9 Fast Fractional PLL

The frequency of the VHF VCO is locked to a reference frequency by an on-chip fractional-N PLL circuit which guarantees superior phase-noise performance. The reference frequencies for the two PLL blocks are generated by an on-chip oscillator.

The VCOs are fully integrated, which simplifies the design of the device and reduces the bill of materials of the application.

The LO signal for the first L-band mixer is derived from a PLL-controlled on-chip VCO. The down-converting to an IF frequency of 38.912 MHz for VHF or converted L-band signal is done by an additional on-chip VCO using an internal fractional-N PLL.

Due to the digital tuning option of the reference frequency, the ATR2732N3 is able to support the single reference clock design if the baseband can support such a feature (as the ATR2740 does).

3.10 Reference Oscillator

An on-chip crystal oscillator generates the reference signal which is fed to the reference divider. By applying a crystal to the pins XTALA and XTALB, this oscillator generates a highly stable reference signal.

Furthermore, the frequency of this reference oscillator can be digitally tuned via the SPI bus bits XOTi (i = 11, ..., 0) with a 12-bit step size.

3.11 Reference Divider

Starting from a minimum value, the scaling factor of the 6-bit reference divider is arbitrarily programmable by means of the SPI bus bits Ri (i = 5, ..., 0).

The output of this first programmable divider typically provides a 2.048 MHz reference frequency for the L-band PLL.

A second programmable divider (dividing by 8 to 128) then outputs 64 kHz, which is a useful reference frequency for the VHF PLL.

Together with the fractional-N PLL, a step size of 16 kHz for the frequency setting of the VHF LO is ensured.

3.12 Main Divider

The main divider consists of a fully programmable 13-bit divider which defines a division ratio N. The applied division ratio is either N or N + 1, as specified by a special control unit. On average, the scaling factors SF = N + k / 4 can be selected where k = 0, 1, 2, or 3.

3.13 Phase Comparator and Charge Pump

The tri-state phase detectors cause the charge pumps to source or sink currents at the output pins PFDOUTV (for VHF) and PFDOUTL (for L-band) depending on the phase relation of its input signals, which are provided by the reference and the main dividers, respectively.

3.14 SPI Bus

The bus interface can be adapted to the signal voltage as a result of the supply voltage of the external baseband processing unit connected to the bus. This is done with the help of a sensing pin, VDI, which checks the supply voltage of the processor. The interface adapts itself to any voltage between 1.65V and 3.5V.

3.14.1 Programming via SPI

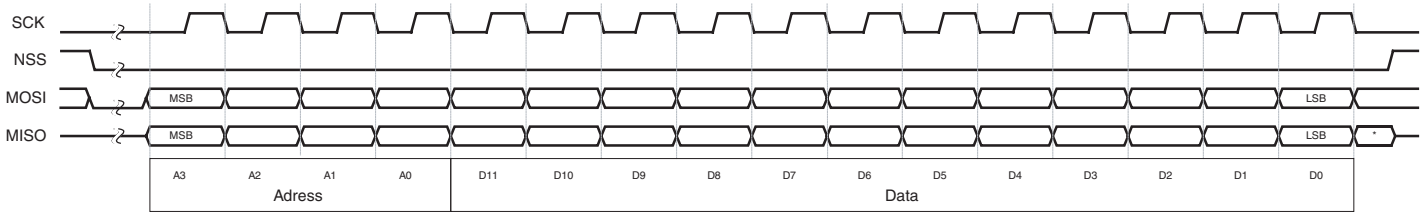
Some things need to be taken into account when programming the ATR2732N3 via the SPI interface: the data packet needs to be properly configured to write into the 14 different registers.

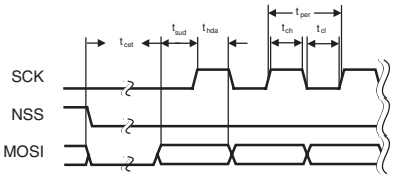
There are 16 registers. Fourteen of them are used to control the ATR2732N3. The two others, registers 15 and 16, are Test Mode Registers. All these registers need to be reset by writing “0” to every bit of each register one time, before starting the configuration of the ATR2732N3.

There are 4 address bits (bit 12 is address bit 0; bit 15 is address bit 3) which are used to select the correct register. These are followed by 12 data bits (LSB is bit 0; MSB is bit 11). There is a definite transmit order which needs to be considered: the MSB must be transmitted first (bit 15, address bit 3), and LSB (data bit 0) last.

Unused and test mode register bits may not be documented in the datasheet and have to be set to “0” in customer applications. Information about the status of the device is available by reading one word (16 bits) out of the part.

Figure 3-2. Timing Diagram of the SPI Interface (16 Bits per Transfer)





t_{cet}: Clock enable time
t_{sud}: Data setup time
t_{hda}: Hold time of MOSI
t_{per}: Clock period
t_{ch}: Clock high time
t_{cl}: Clock low time

Note: It is absolutely necessary to set the NSS signal back to high after every SPI access.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	V_{CC}	4.0	V
Operating case temperature	T_c	–40 to +100	°C
Storage temperature	T_{stg}	–40 to +150	°C
Maximum RF input power VHF		25	dBm
Maximum RF input power L-band		20	dBm

Notes: 1. The part may not survive all maximums applied simultaneously!

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction, case	R_{thJC}	15	K/W

6. Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V_{CC}	3.0 to 3.5	V
Ambient temperature	T_{amb}	–40 to +85	°C

7. Electrical Characteristics

Test conditions (if not otherwise specified): V_{CC} = +3.3V, T_{amb} = +25°C, 50Ω input match

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply**								
1.1	Supply voltage of front end ATR2732N3			V_{CC}	3.0		3.5	V	A
1.2	Supply voltage of baseband processor			V_{Di}	1.65		V_{CC}	V	A
1.3	Leakage current, all off			I_{leak}		3	25	µA	A
2	**Power Control**								
2.1	Power on/off delay					1		µs	C
2.2	Power off/on delay					5		ms	C
2.3	Supply current L-band off	Reception only VHF				150		mA	A
2.4	Supply current L-band					185		mA	A
2.5	Power-off tuning voltage generation	Tuning generation not active				140		mA	B
2.6	Average current consumption					80		mA	B
3	**SPI Bus Interface**								
3.1	BUS voltage high			V_{BUSH}	V_{Di} – 0.36		V_{Di} + 0.3	V	A
3.2	BUS voltage low			V_{BUSL}	–0.3		+0.25	V	A
3.3	Clock frequency			$1 / t_{per}$			2	MHz	A
3.4	Clock high time (SCK)			t_{ch}	$0.4 \times t_{per}$				
3.5	Clock low time (SCK)			t_{cl}	$0.4 \times t_{per}$				
3.6	Clock enable time			t_{cet}	5			µs	
3.7	Data set-up time			t_{sud}	$0.4 \times t_{per}$				
3.8	Hold time MOSI			t_{hda}	$0.4 \times t_{per}$				
4	**Reference Crystal Oscillator**								
4.1	Operating frequency				16	24.576	32	MHz	C
4.2	Tuning range				120	210		ppm	A
4.3	Reference clock output voltage	Sine wave output				0.5		V_{pp}	A
5	**VHF Fractional PLL**								
5.1	LO frequency				200		290	MHz	A
6	**L-band PLL**								
6.1	LO frequency				1.26		1.27	GHz	A
7	**IF Interface**								
7.1	IF frequency range				30	38.91	50	MHz	D
7.2	Output impedance (differential)		46, 47			56	100	Ω	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

Test conditions (if not otherwise specified): V_{CC} = +3.3V, T_{amb} = +25°C, 50Ω input match

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.3	Driving capability/ max. load capacitance (differential)	IFAGCIN+, IFAGCIN– (pins 45, 48) directly connected to IF20+, IF20–	46, 47		5.5	7		pF	D
8	**VHF Band Operation**								
8.1	Frequency range			f_{Rfin}	167		240	MHz	C
8.4	Sensitivity	8 dB SNR at IF output to baseband, measured with sample application				–98		dBm	C
8.5	Maximum input power level					–5		dBm	C
9	**L-band Operation**								
9.1	Frequency range			f_{Rfin}	1452		1492	MHz	C
9.4	Sensitivity	8 dB SNR at IF output to baseband, measured with sample application				–96		dBm	C
9.5	Maximum input power level					–15		dBm	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

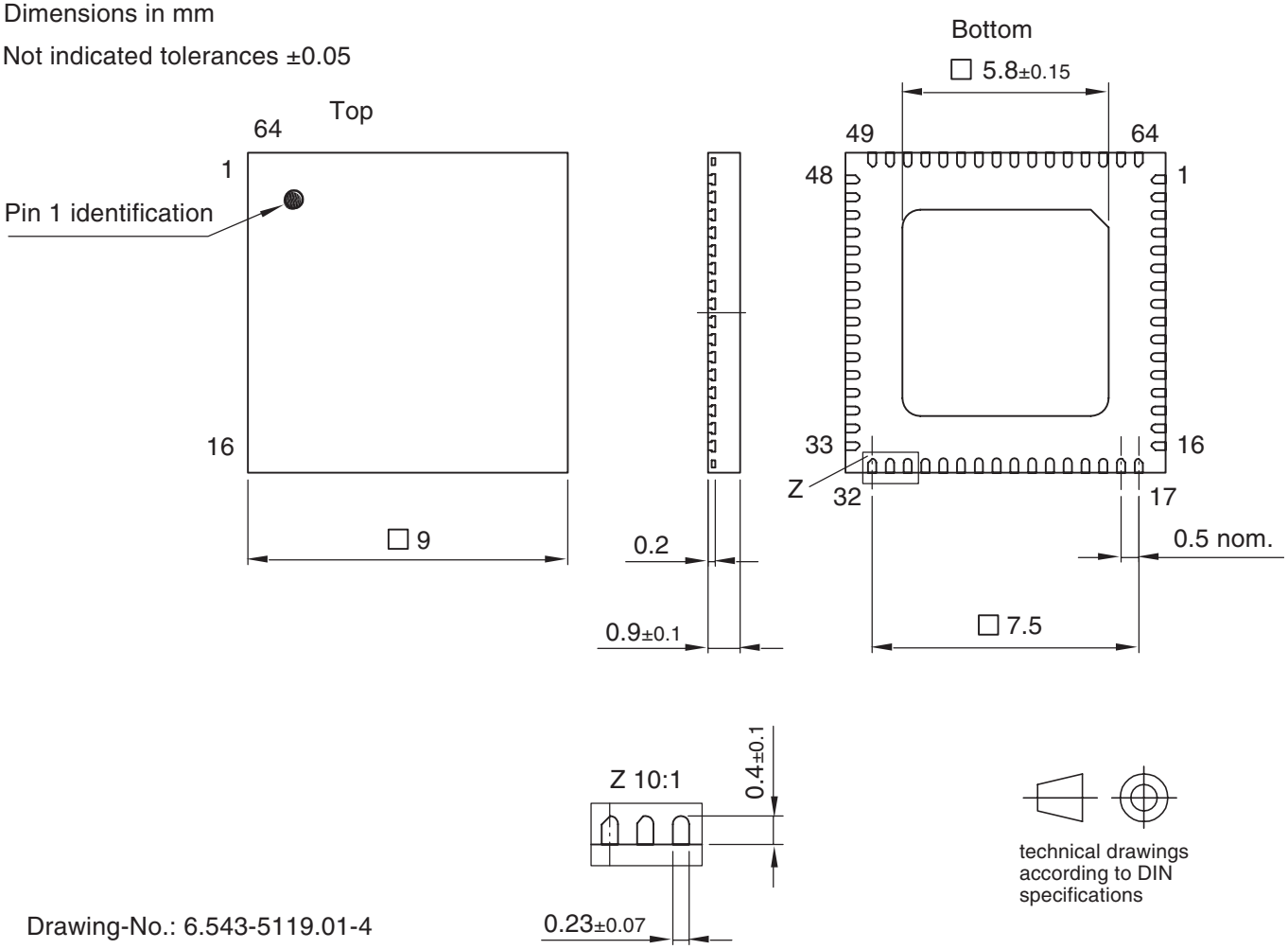
8. Ordering Information

Extended Type Number	Package	Remarks
ATR2732N3-PBQW	QFN64	9 mm × 9 mm, 0.5 mm pitch, lead-free
ATR2732N3-PBPW	QFN64	9 mm × 9 mm, 0.5 mm pitch, lead-free

9. Package Information

Package: VQFN_ 9 x 9_64L
Exposed pad 5.8 x 5.8
Dimensions in mm

Not indicated tolerances ±0.05



Drawing-No.: 6.543-5119.01-4

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