
2.4 GHz WLAN 11b/g/n/ac, High-Efficiency Power Amplifier

Features

- High Gain:
 - Typically 27 dB gain across 2.4–2.5 GHz, <1.5 dB variation over temperature -20°C to +85°C
- Linear output power:
 - >24 dBm P1dB
 - Please refer to [“Absolute Maximum Stress Ratings” on page 5](#)
 - Meets 802.11g OFDM spectrum mask requirement up to 22 dBm
 - Typically 18.5 dBm with <3% EVM, 802.11g, 54 Mbps
 - Typically 18 dBm with <2.5% EVM, 802.11n, MCS7-HT40, 50% duty cycle
 - Meets 802.11b, 1 Mbps, ACPR requirement up to 22 dBm
- High-speed power-up/down
 - Turn on/off time (10%-90%) <100 ns
- 10:1 VSWR survivability (unconditionally stable up to 22 dBm)
- On-chip power detection
 - >20 dB, dB-wise line linear, dynamic range
 - VSWR- and temperature-insensitive
- Simple input/output matching
- Packages available
 - 16-contact UQFN (3mm x 3mm)
 - Pin-to-pin compatible with SST12LP15A
- All non-Pb (lead-free) devices are RoHS compliant

Applications

- WLAN (IEEE 802.11b/g/n)
- WLAN 256 QAM
- AP router
- WiMax (IEEE 802.16e)
- Cordless phones
- 2.4 GHz ISM wireless equipment
- Bluetooth®

1.0 PRODUCT DESCRIPTION

SST12LP25 power amplifier (PA) is based on the highly-reliable InGaP/GaAs HBT technology.

This PA can be easily configured for high-power applications with high power-added efficiency while operating over the 2.4-2.5 GHz frequency band. It typically provides 27 dB gain with greater than 36% power-added efficiency @ $P_{OUT} = 22$ dBm for 802.11g.

SST12LP25 has excellent linearity, typically 18.5 dBm at 3% EVM with 54 Mbps 802.11g operation while meeting 802.11g spectrum mask at 22 dBm. The PA also provides typically 18 dBm at 2.5% EVM with MCS7-HT40 modulation.

The power amplifier IC also features easy board-level usage, high-speed power-up/-down control, and a single-ended power detector which lowers the users' cost for power control.

SST12LP25 is offered in 16-contact UQFN package. See [Figure 3-1](#) for pin assignments and [Table 3-1](#) for pin descriptions.

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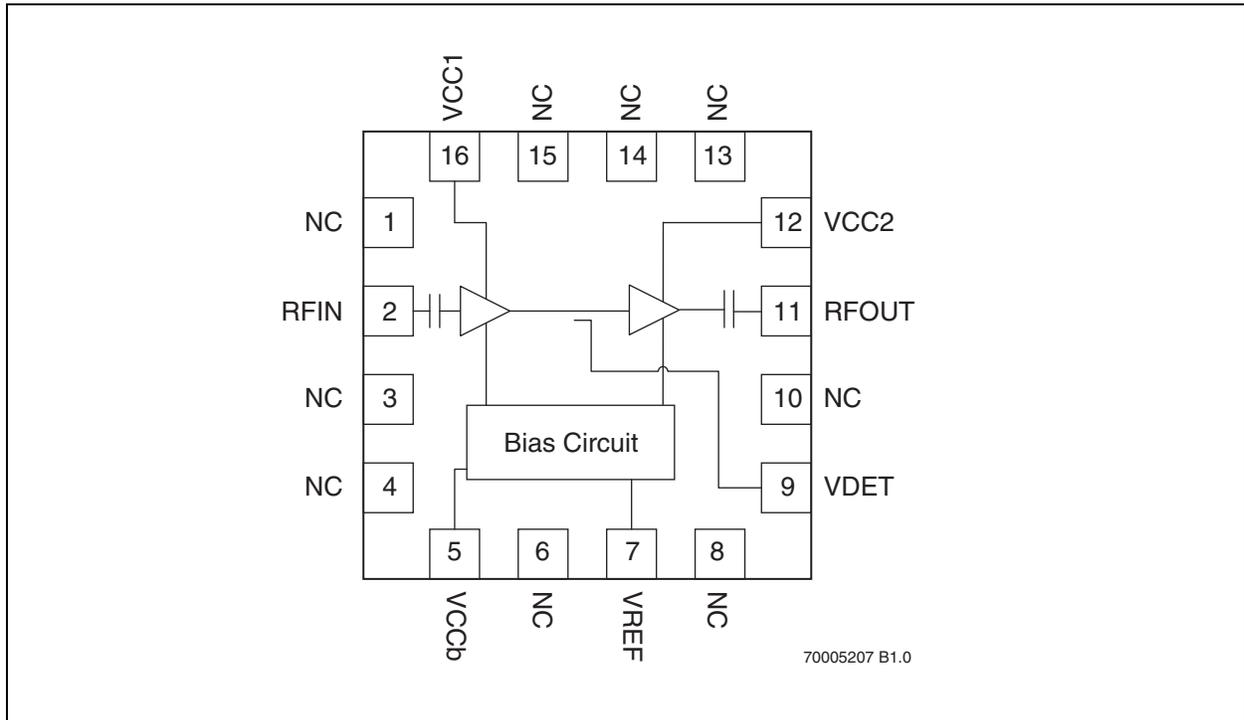
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2.0 FUNCTIONAL BLOCKS

FIGURE 2-1: FUNCTIONAL BLOCK DIAGRAM



SST12LP25

3.0 PIN ASSIGNMENTS

FIGURE 3-1: PIN ASSIGNMENTS FOR 16-CONTACT UQFN

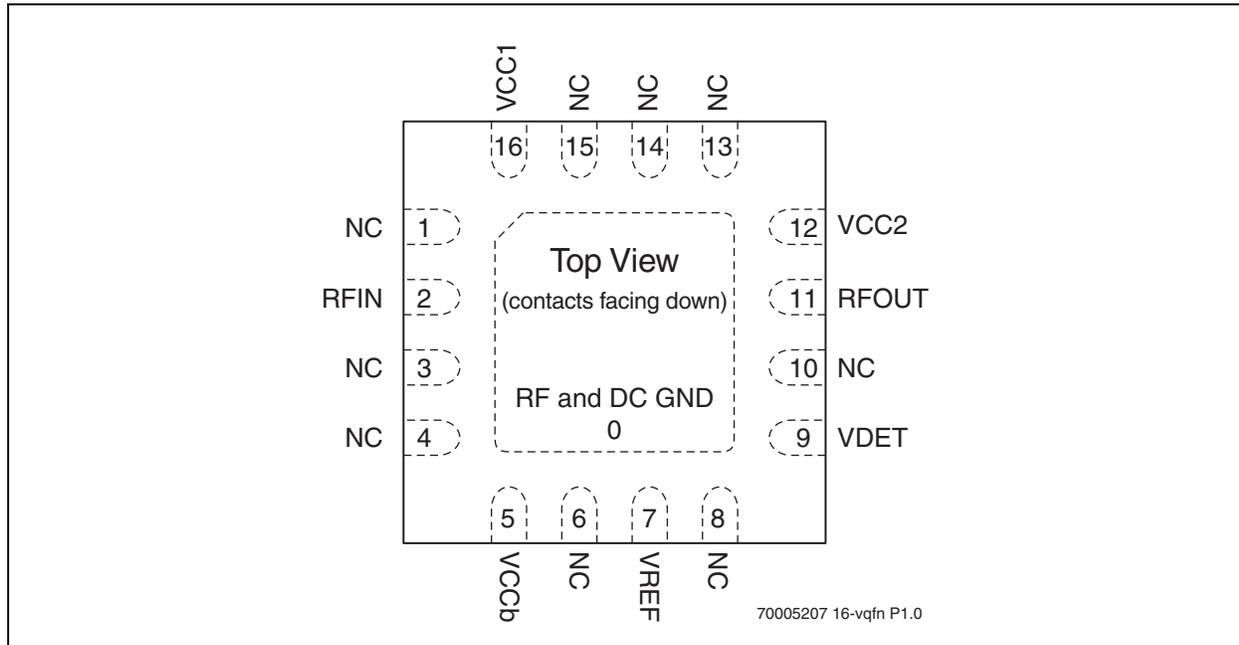


TABLE 3-1: PIN DESCRIPTION

Symbol	Pin No.	Pin Name	Type ¹	Function
GND	0	Ground		The center pad should be connected to RF ground with several low inductance, low resistance vias.
NC	1	No Connection		Unconnected pin
RFIN	2		I	RF input, DC decoupled
NC	3	No Connection		Unconnected pin
NC	4	No Connection		Unconnected pin
VCCb	5	Power Supply	PWR	Supply voltage for bias circuit
NC	6	No Connection		
VREF	7	Power supply	PWR	Idle-current control
NC	8	No Connection		Unconnected pin
VDET	9			On-chip power detector
NC	10	No Connection		Unconnected pin
RFOUT	11		O	RF output
VCC2	12	Power Supply	PWR	Power supply, 2 nd stage
NC	13	No Connection		Unconnected pin
NC	14	No Connection		Unconnected pin
NC	15	No Connection		Unconnected pin
VCC1	16	Power Supply	PWR	Power supply, 1 st stage

1. I=Input, O=Output

4.0 ELECTRICAL SPECIFICATIONS

The DC and RF specifications for the power amplifier are specified below. Refer to [Table 4-2](#) for the DC voltage and current specifications.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pin 2 (P_{IN})	+5 dBm
Supply voltage at pins 5,12,and 16 (V_{CC})	+6 V
Reference voltage to pin 7 (V_{REF})	+3.2 V
DC supply current (I_{CC})	250 mA
Operating Temperature (T_A)	-40°C to +85°C
Storage Temperature (T_{STG})	-40°C to +120°C
Maximum Junction Temperature (T_J)	+150°C
Surface Mount Solder Reflow Temperature	260°C for 10 seconds

TABLE 4-1: OPERATING RANGE

Range	Ambient Temp	V_{CC}
Industrial	-20°C to +85°C	5.0V

TABLE 4-2: DC ELECTRICAL CHARACTERISTICS AT 25°C

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
I_{CC}	DC Current				
	for 802.11g, 22 dBm		125		mA
	for 802.11b, 22 dBm		125		mA
I_{CQ}	Idle Current for 802.11g to meet EVM<3% @18.5 dBm		52		mA
V_{REG}	Reference Voltage see Figure 5-7 on page 10		2.85	3.0	V
I_{REG}	Reference Current		1		mA

SST12LP25

TABLE 4-3: AC ELECTRICAL CHARACTERISTICS FOR CONFIGURATION AT $V_{CC} = 3.3V$, $V_{REF} = 2.85V$, 25°C, 50% DUTY CYCLE

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range in 802.11b/g applications	2400		2500	MHz
P_{OUT}	Output power at 3% EVM with 802.11g OFDM at 54 Mbps		18.5		dBm
	Output power at 2.5% EVM with 802.11n MCS7 HT20		18		dBm
	Output power meeting 802.11g spectral mask		22		dBm
	Output power meeting 802.11n HT40 spectral mask		19.5		dBm
	Output power meeting 802.11b, 1 Mbps spectral mask		22		dBm
G	Power gain for 802.11b/g/n/256 QAM	24.5	27		dB
G_{VAR}	Gain variation over band			± 0.5	dB
2f	Second Harmonic at 22 dBm, 802.11b mask compliance		-25		dBm/MHz
	Second Harmonic at 22 dBm ¹		-50		dBm/MHz
3f	Third Harmonic at 22 dBm, 802.11b mask compliance		-35		dBm/MHz
	Third Harmonic at 22 dBm ¹		-50		dBm/MHz

1. With filter match. [Figure 5-8 on page 11](#)

5.0 TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: $V_{CC} = 3.3V$, $V_{REG} = 2.85V$, $T_A = 25^\circ C$, IEEE 802.11g, 54 Mbps, 50% duty cycle, unless otherwise specified

FIGURE 5-1: S-PARAMETERS

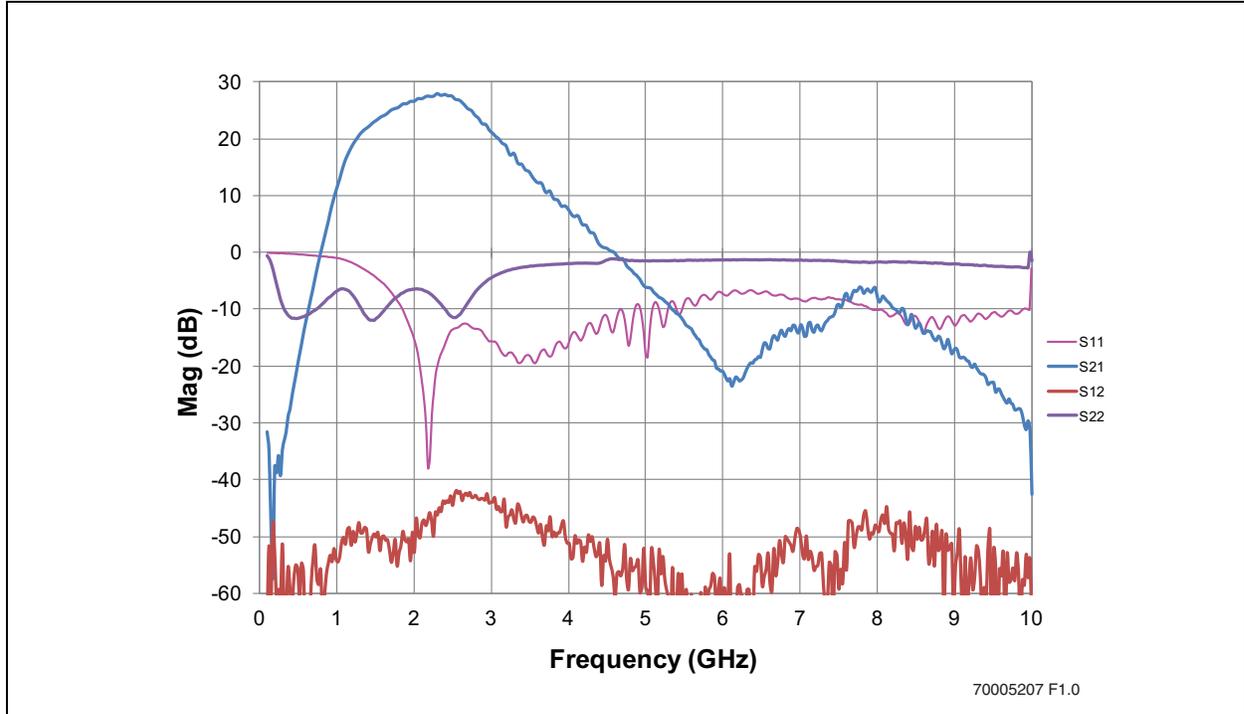
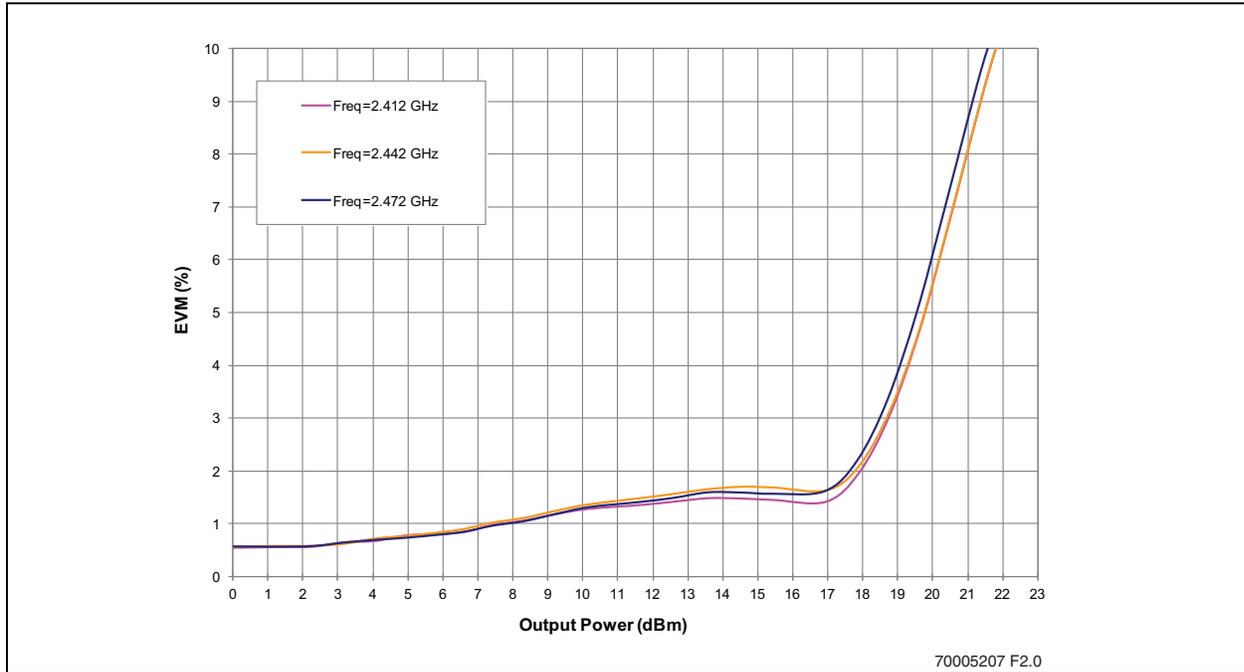


FIGURE 5-2: DYNAMIC EVM VERSUS OUTPUT POWER



SST12LP25

FIGURE 5-3: DYNAMIC EVM VERSUS OUTPUT POWER, WITH MCS7-40 MHz

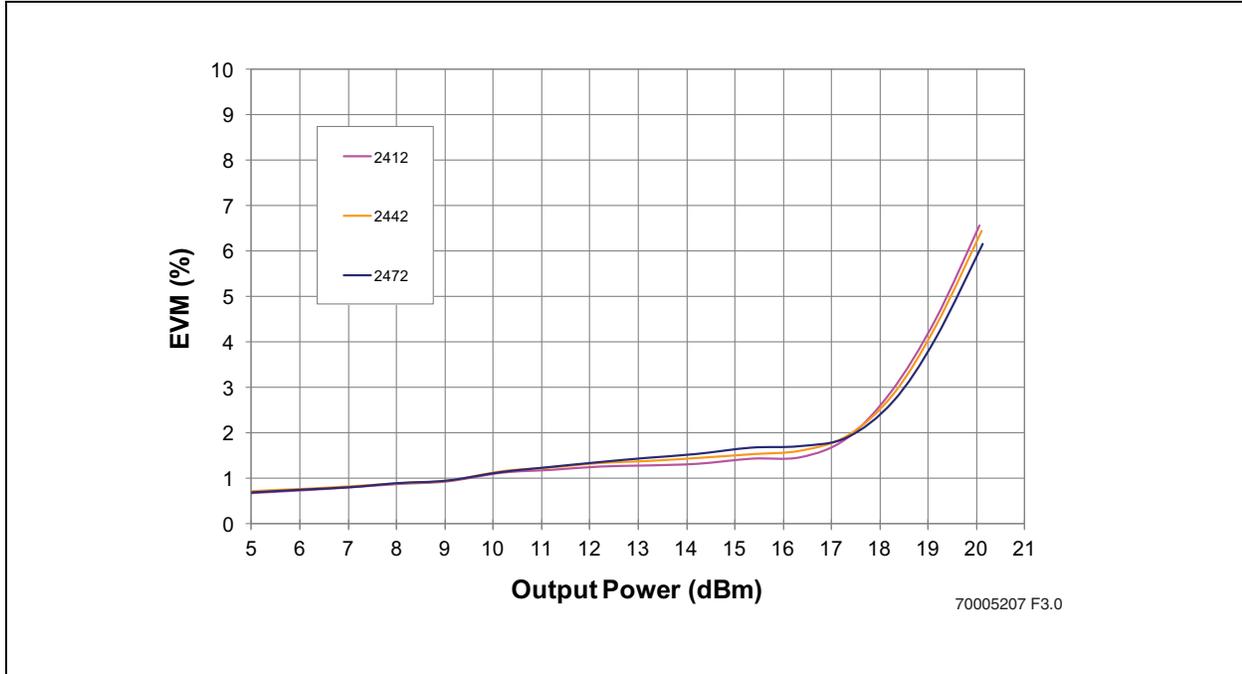


FIGURE 5-4: POWER GAIN VERSUS OUTPUT POWER

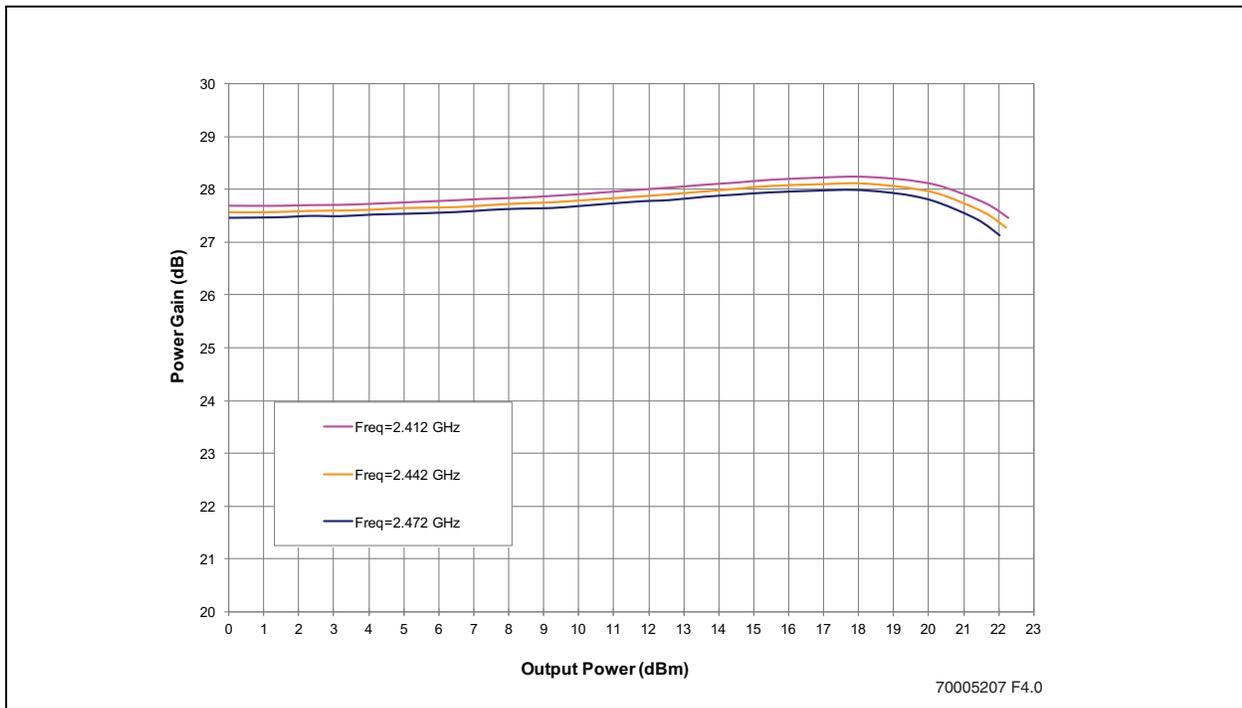


FIGURE 5-5: SUPPLY CURRENT VERSUS OUTPUT POWER

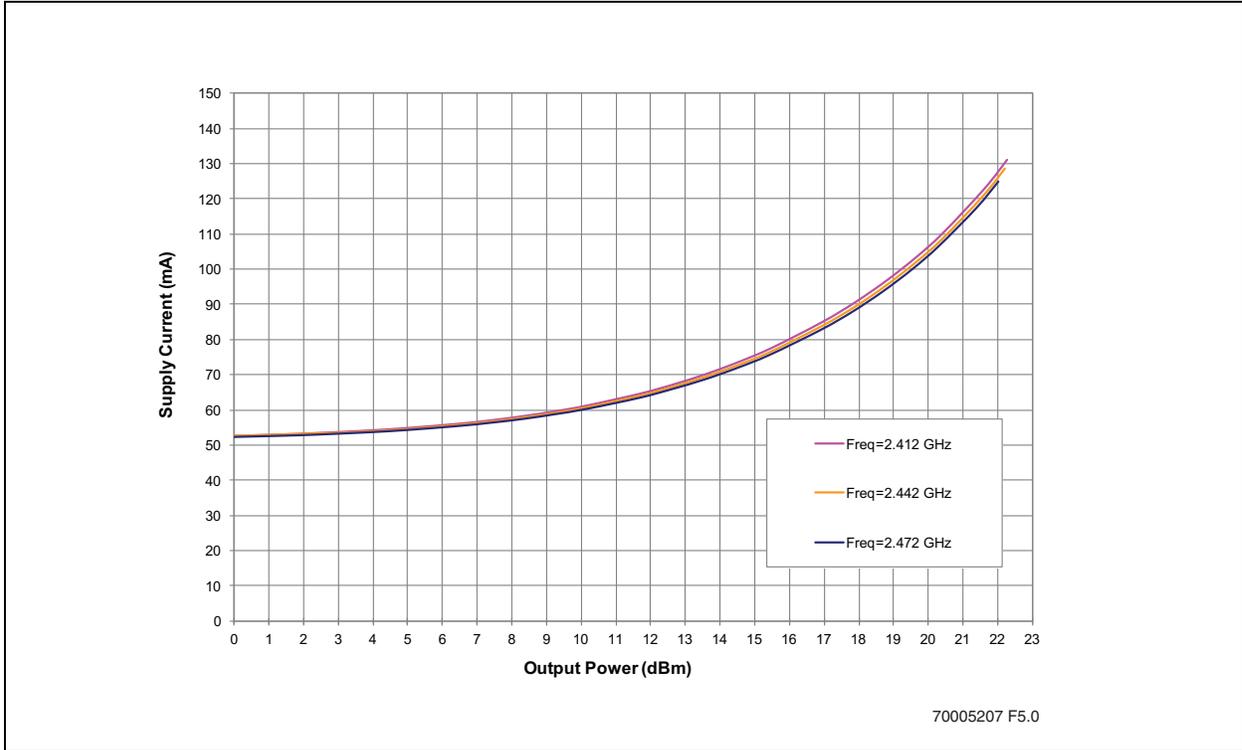
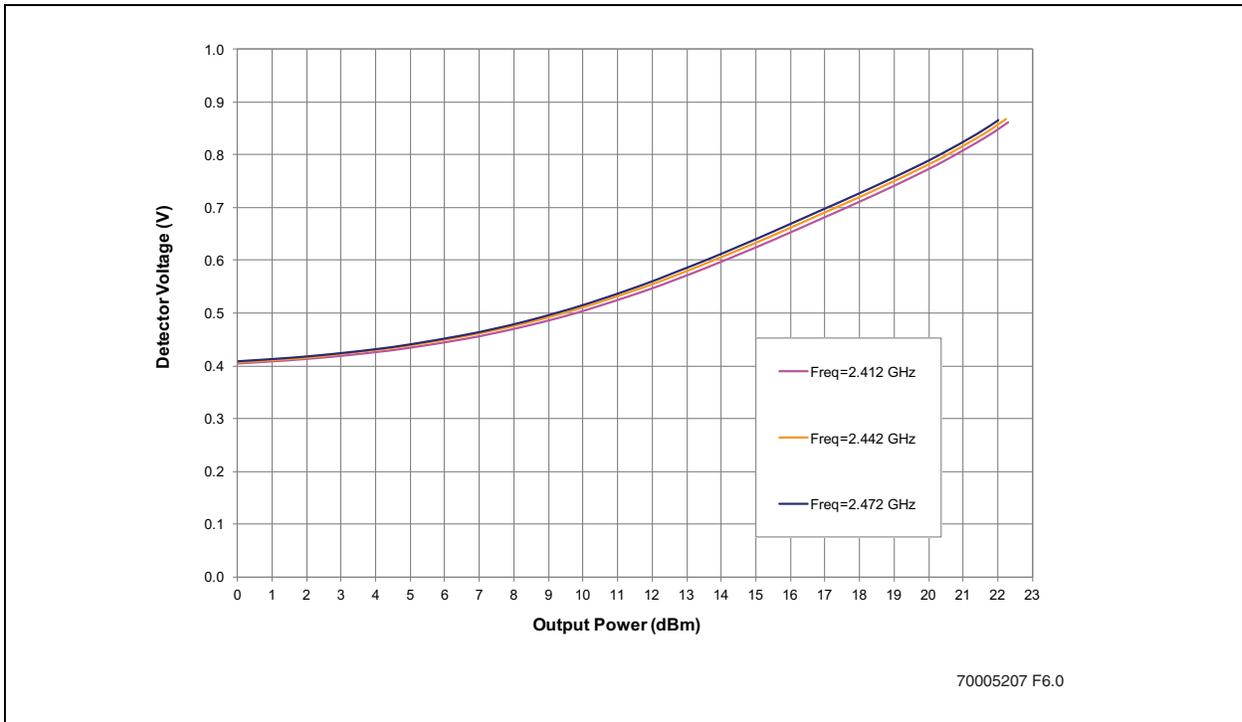


FIGURE 5-6: DETECTOR CHARACTERISTIC VERSUS OUTPUT POWER



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FIGURE 5-7: TYPICAL SCHEMATIC

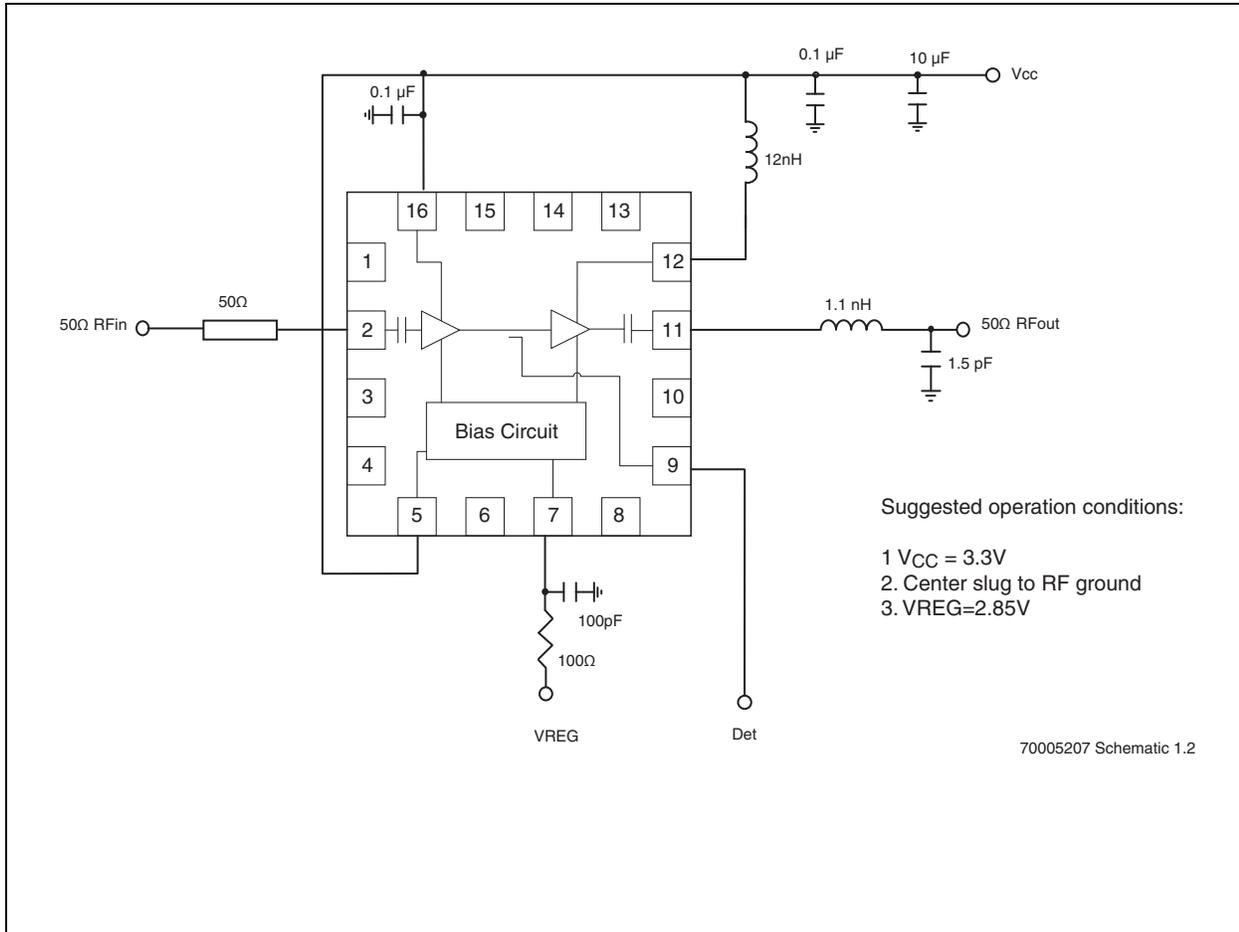
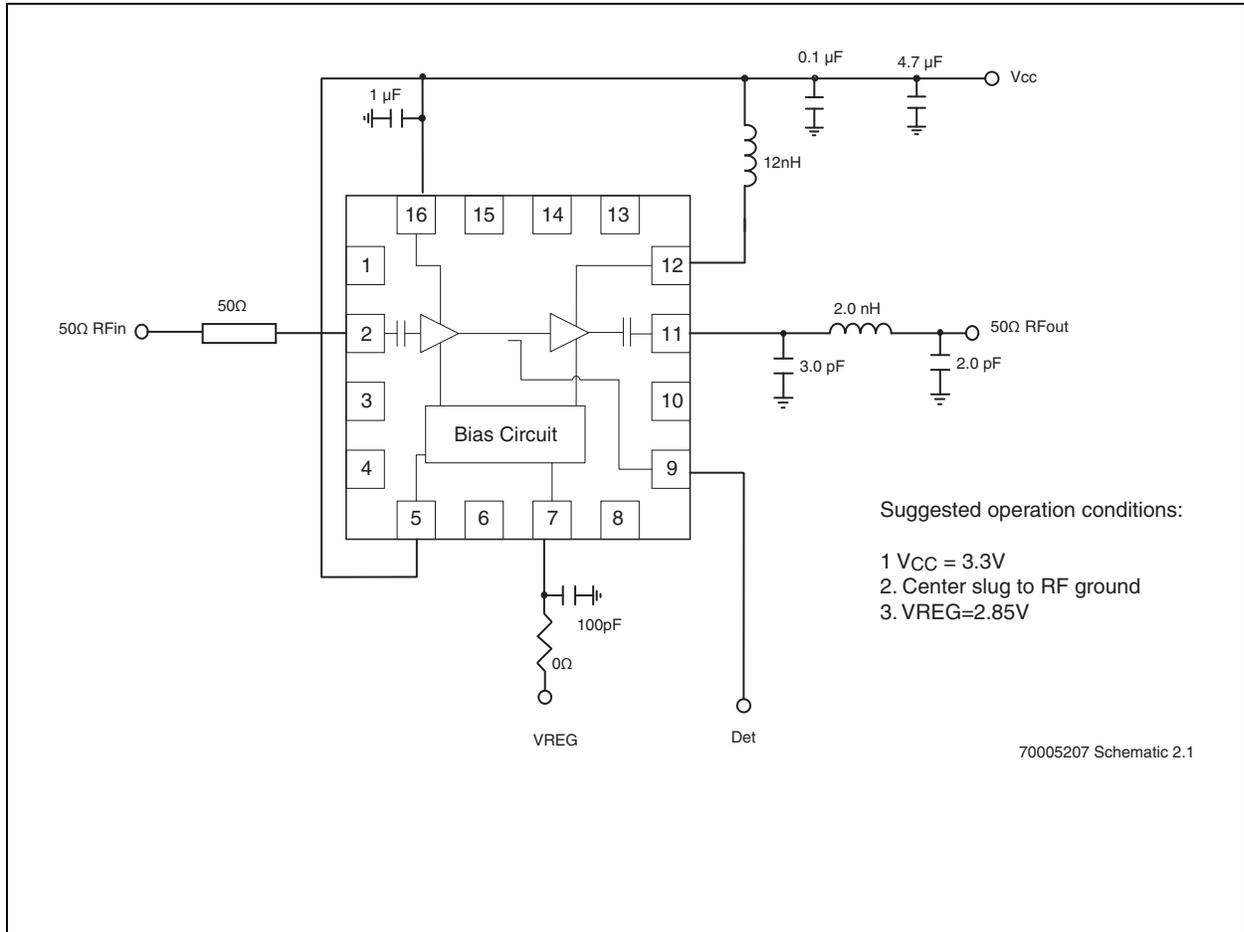


FIGURE 5-8: TYPICAL SCHEMATIC WITH FILTER MATCH

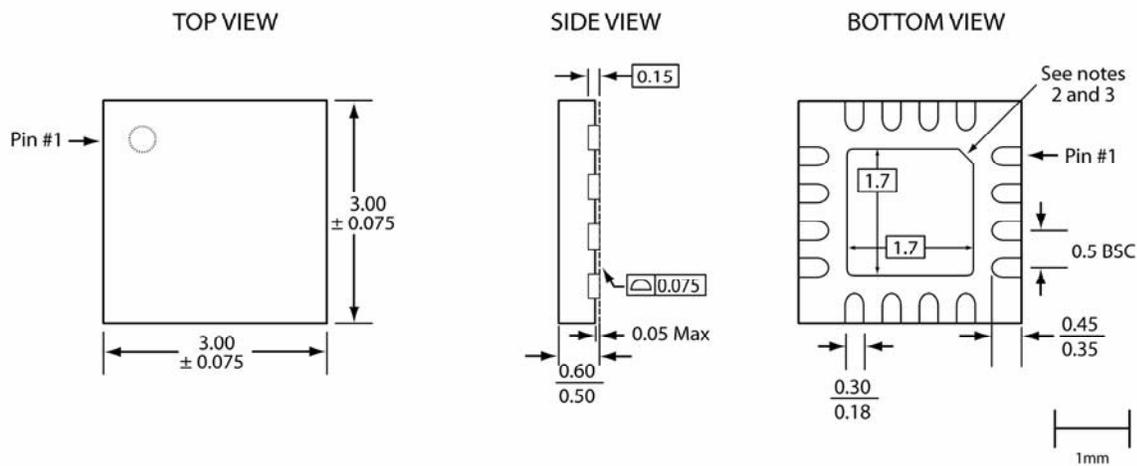


SST12LP25

6.0 PACKAGING DIAGRAMS

16-Lead Ultra Thin Quad Flatpack No-Leads (QUCE/F) - 3x3 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



16-uqfn-3x3-QUC-0.0

Note:

1. Complies with JEDEC JEP95 MO-248D, variant UEED-4 except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

TABLE 6-1: REVISION HISTORY

Revision	Description	Date
A	• Initial release of data sheet	Jan 2015

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7.0 PRODUCT IDENTIFICATION SYSTEM

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PART NO.	XXX	
Device	Package	
Device:	SST12LP25	= 2.4 GHz Power Amplifier
Package:	QUCE	= UQFN (3mm x 3mm), 0.6 max thickness 16-contact
Evaluation Kit Flag	K	= Evaluation Kit

Valid Combinations:
SST12LP25-QUCE
SST12LP25-QUCE-K

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