Atmel ATWINC1500

Single Chip IEEE 802.11 b/g/n Network Controller SOC with Integrated Flash Memory

PRELIMINARY DATASHEET

Description

The Atmel® WINC1500 is a single chip IEEE® 802.11 b/g/n RF, IoT (Internet of Things) Network Controller SoC. The WINC1500 most advanced mode is a single stream 1x1 802.11n mode providing up to 72Mbps PHY throughput. The WINC1500 features fully integrated Power Amplifier, LNA, Switch and Power Management. Implemented in 65nm CMOS technology, the WINC1500 offers very low power consumption while simultaneously providing high performance and optimized bill of material.

The WINC1500 provides internal Flash memory as well as multiple peripheral interfaces including UART, SPI, and I2C. The only external clock source needed for the WINC1500 is a high-speed crystal or oscillator with a wide variety of reference clock frequencies supported (between 12 – 32 MHz). The WINC1500 is available in a QFN package and connects to any AVR or SMART MCU with minimal resources.

Features

- IEEE 802.11 b/g/n RF/PH/MAC SOC
- IEEE 802.11 b/g/n (1x1) for up to 72Mbps
- Single spatial stream in 2.5Ghz RF band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via advanced PHY signal processing
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- On-chip memory management engine to reduce host load
- 4Mbit internal Flash memory for system software
- SPI, UART and I^2C as host interfaces
- Power save modes:
  - 3µA deep sleep mode
  - 600µA standby mode (state is preserved)
  - On-chip low power sleep oscillator
  - Fast host wake-up by chip pin or clock-less transaction
- Fast boot options
  - On-Chip Boot ROM (Firmware instant boot)
  - SPI flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables (next chip revision)

- No SPI flash is needed if firmware patches and state variables can be loaded from MCU at boot time
- Fast AP Re-Association (150ms)

- On-Chip Network Stack to offload MCU
  - Integrated Network IP stack to minimize host CPU requirements
  - Network features TCP, UDP, DHCP, ARP, HTTP, SSL, and DNS
- TCP/IP protocol stack (client/server) sockets applications
- Wi-Fi security WEP, WPA, WPA2 and WPS
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Network protocols (DHCP/DNS)
- WSC (wireless simple configuration WPS)
- No OS small footprint host driver (4KB flash – less than 1KB RAM)

1. Ordering Information

Ordering code	Package[1]	Description
ATWINC1500A-MU-T	5x5 QFN	Single 802.11.b/g/n Chip
ATWINC1500-MR210PA	22 X 15mm	Certified module with ATWINC1500A-Mu chip and PCB antenna
ATWINC1500-MR510A		Certified module withATWINC1500A-Mu chip and crypto security
ATWINC1500-XPRO		An extension card containing ATWINC1500-MR210PA module that is compatible with any XPlained Pro card
ATWINC1500-XSTK		Starter kit including XPlained Pro-D21 and an WINC1500-XPRO wing board

Note: 1. The QFN package is a qualified Green Package.

2. Package Information

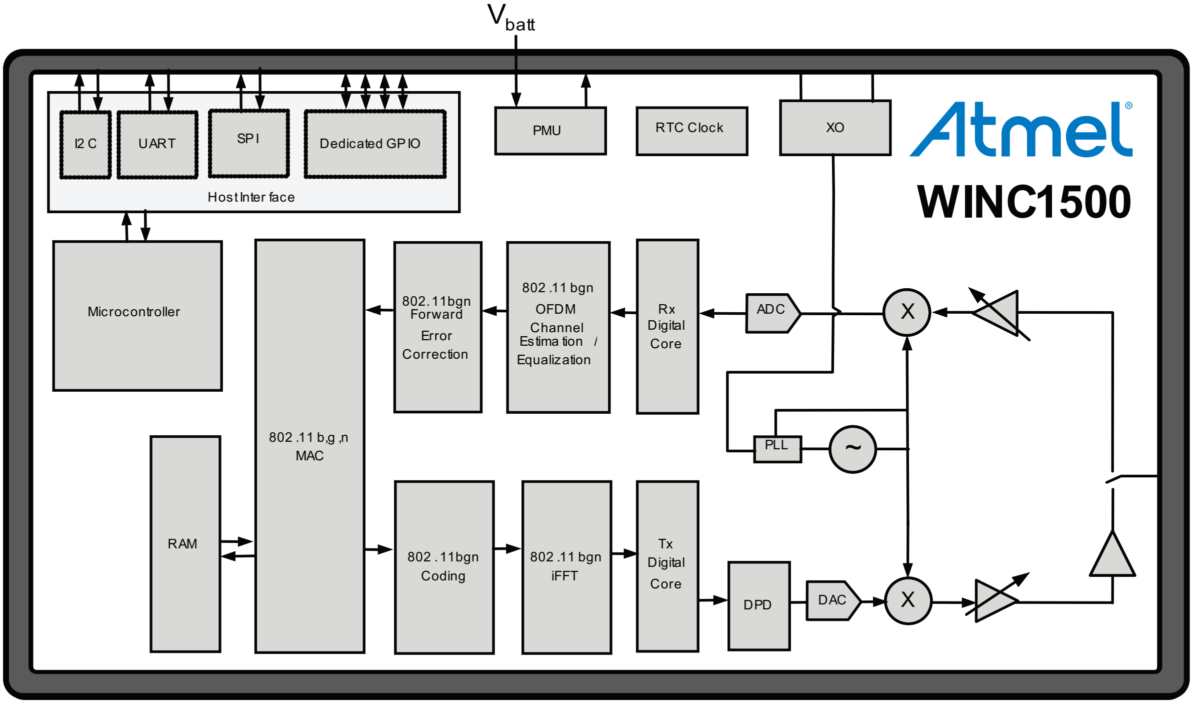
Table 2-1. WINC1500 QFN Package Information[1]

Parameter	Value	Units	Tolerance
Package Size	5 x 5	mm	± 0.1mm
QFN Pad Count	40		
Total Thickness	0.85	mm	± 0.05mm
QFN Pad Pitch	0.4	mm	
Pad Width	0.2	mm	
Exposed Pad Size	3.7 x 3.7	mm	

Note: 1. For the details, see "Package Drawing" on page 22

3. Block Diagram

Figure 3-1. WINC1500 Block Diagram



4. Pinout

The Atmel WINC1500 is offered in an exposed pad 40L, QFN package. The package has an exposed paddle that must be connected to the system board ground.

Table 4-1. WINC1500 QFN Pin Connectivity

Pin #	Pin Name	Pull up/down	Description
1	TP_P	None	Test Pin / Customer No Connect
2	VDD_RF_RX	None	Tuner 1.2V RF Supply
3	VDD_AMS	None	1.2V Analog / Mixed Signal Supply
4	VDD_RF_TX	None	Tuner 1.2V RF supply
5	VBAT_PPA	None	PrePA power supply
6	VBAT_PA	None	Battery Power Supply for PA
7	RFIOP	None	Pos RF Differential I/O
8	RFION	None	Neg RF Differential I/O
9	SPI_CFG	None	Tie to HIGH for SPI
10	GPIO0/HOST_WAKE	Programmable Pull-Up	GPIO0 / SLEEP Mode Control
11	GPIO2/IRQN	Programmable Pull-Up	GPIO2 / Device Interrupt
12	UART_TXD	Programmable Pull-Up	UART_TXD
13	SPI_RXD	Programmable Pull-Up	SPI Data Rx
14	VDD_1V20_1	None	1.2V Core Power Supply
15	VDDIO	None	I/O Power Supply
16	SPI_SSN	Programmable Pull-Up	SPI Slave Select
17	SPI_TXD	Programmable Pull-Up	SPI Data Tx
18	SPI_SCK	Programmable Pull-Up	SPI Clock
19	UART_RXD	Programmable Pull-Up	UART_RXD
20	VBATT_BUCK	None	Battery Supply for DC/DC Converter
21	VSW	None	1.2V Power from DC/DC Converter
22	VREG_BUCK	None	Feeds VSW Back to DC/DC Converter
23	CHIP_EN	None	PMU Enable
24	GPIO1/RTC_CLK	Programmable Pull-Down	GPIO1 / 32 kHz Clock Input
25	TEST_MODE	None	Test Mode – Customer Tie to GND
26	VDDIO	None	I/O Power Supply
27	VDD_1V20_2	None	1.2V Core Power Supply
28	GPIO17	Programmable Pull-Up	GPIO17
29	GPIO18	Programmable Pull-Up	GPIO18

Table 4-1. WINC1500 QFN Pin Connectivity (Continued)

Pin #	Pin Name	Pull up/down	Description
30	GPIO19	Programmable Pull-Up	GPIO19
31	GPIO20	Programmable Pull-Up	GPIO20
32	I2C_SCL	Programmable Pull-Up	I^2C Slave Clock
33	I2C_SDA	Programmable Pull-Up	I^2C Slave Data
34	RESETN	None	Active-Low Hard Reset
35	XO_N	None	Crystal Oscillator N
36	XO_P	None	Crystal Oscillator P
37	VDD_SXDIG	None	1.2V SX Power Supply
38	VDD_VCO	None	1.2V VCO Power Supply
39	VDDIO_A	None	Tuner VDDIO Supply
40	TPN	None	Test Pin / Customer No Connect
41	PADDLE VSS	None	Connect to System Board Ground

5. Power Management

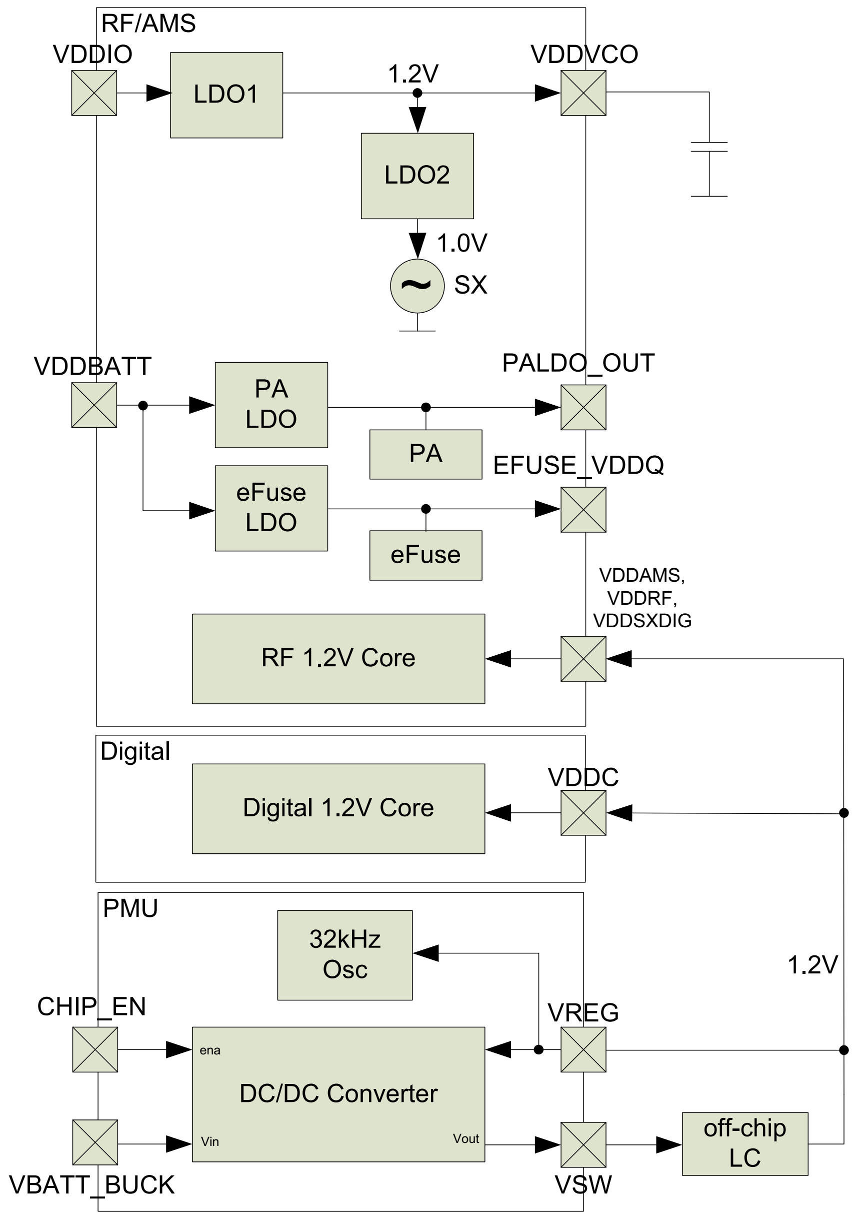
5.1 Power Architecture

The Atmel WINC1500 device uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. The architecture is shown in Figure 5-1.

The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the 1.2V supply used by the digital and RF/AMS blocks. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

The power connections in Figure 5-1 provide a conceptual framework for understanding the WINC1500 power architecture. Reference designs will be provided to demonstrate how to properly connect the supplies, including proper isolation of the supplies used by the digital and RF/AMS blocks.

Figure 5-1. WINC1500 Power Architecture



5.2 Power Consumption

5.2.1 Description of Device States

Atmel WINC1500 device has several Device States:

- **ON_Transmit** – Device is actively transmitting an 802.11 signal
- **ON_Receive** – Device is actively receiving an 802.11 signal
- **ON_Doze** – Device is on but is neither transmitting nor receiving
- **SLEEP** – Device is asleep with 1.2V supply off
- **Power_Off** – Device is powered off; VDD_1P3 and VDDIO are off

5.2.2 Controlling the Device States

Table 5-1 shows how to switch between the device states using the following:

- **CHI_EN** – Device pin (pin #23) used to enable DC/DC Converter
- **VDDIO** – I/O supply voltage from external supply

Table 5-1. WINC1500 Device State Control

Device State	CHIP_EN	VDDIO	Remark	Power Consumption
ON_Transmit	VDDIO	On	Transmitting	172mA @3.3V (18dBm) 149mA @2.5V (14dBm) 117mA @2.0V (10dBm)
ON_Receive	VDDIO	On	Receiving	70mA @3.3V (-90dBm) 65mA @3.3V (-87dBm)
ON_Doze	VDDIO	On	Idle[1]	1mA
SLEEP	GND	On		< 4µA

Note: 1. The device is Idle in ON_Doze state during Passive Scan waiting for the Beacon Signal

5.2.3 Restrictions for Power_Off State

When the Atmel WINC1500 is in the Device State Power_Off, there is no power supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the WINC1500 pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

6. CPU and Memory Subsystem

6.1 Processor

The Atmel WINC1500 device has a Cortus APS3 32-bit processor with a JTAG debug interface. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

6.2 Memory Subsystem

The APS3 core uses a small boot ROM along with a 128KB instruction RAM and a 64KB data RAM. In addition, the device uses a 128KB shared memory which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

6.3 Non-Volatile Memory

The Atmel WINC1500 device has 256 bits of non-volatile memory (NVM) that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as the MAC address, along with calibration information, such as TX power calibration tables.

6.4 Flash Memory

NMC1500 has 4 Mbits of Flash memory that can be wrote to and read by the CPU. This memory can be used to store the Network IP stack (TCP, UDP etc) and Wi-Fi Security such as WEP, WPA(2) and WPS. Enables host driver to operate on very small memory footprint MCUs without an OS (4KB Flash/1KB RAM).

7. Clocking

7.1 Crystal Oscillator

Table 7-1. WINC1500 Crystal Oscillator Parameters

Parameter	Min	Typical	Max	Units
Crystal Resonant Frequency	12		32	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability	-25		25	ppm

The block diagram in Figure 7-1(a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5pF can be applied to the XO_N terminal as shown Figure 7-1(b).

Figure 7-1. WINC1500 XO connections to crystal when (a) the crystal oscillator is used, and (b) the crystal oscillator is bypassed

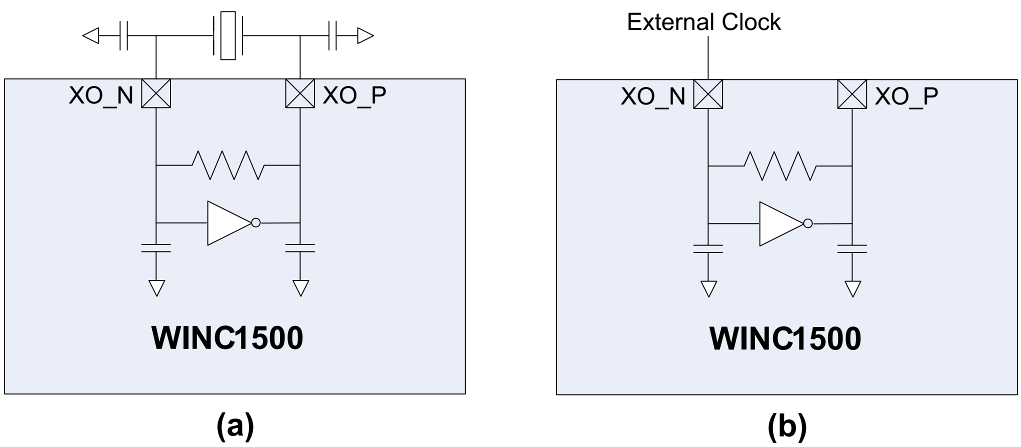


Table 7-2. WINC1500 Bypass Clock Specification

Parameter	Conditions	Min	Max	Units	Comments
Oscillator frequency		12	32	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing		0.5	1.8	Vpp	Must be AC coupled
Stability		-100	+100	ppm	
Phase Noise	@ 1KHz Offset		-130	dBc/Hz	
Jitter (RMS)			<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

7.2 Low Power Oscillator

Atmel WINC1500 device provides an internally-generated 32kHz clock to provide timing information for various sleep functions. In addition, WINC1500 allows for an external 32kHz clock to be provided through Pin 24. Software selects whether the internal clock or external clock is used.

8. WLAN Subsystem

The WLAN subsystem is composed by the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

8.1 MAC

8.1.1 Features

The Atmel WINC1500 IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/HCCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
  - PSMP
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)
- Built-in programmable processor for future enhancement and standards evolution
- Auto-rate control
- MIB management

8.1.2 Description

The Atmel WINC1500 MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block-ack controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

8.2 PHY

8.2.1 Features

The Atmel WINC1500 IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

8.2.2 Description

The Atmel WINC1500 PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

8.3 Radio

8.3.1 Receiver Performance

Table 8-1. WINC1500 Receiver Performance

Parameter	Description	Min	Typical	Max	Unit
Frequency		**2,412**		**2,484**	**MHz**
Sensitivity 802.11b	1Mbps DSS		-97.3		dBm
	2Mbps DSS		-94.0		dBm
	5.5Mbps DSS		-91.7		dBm
	11Mbps DSS		-87.7		dBm
Sensitivity 802.11g	6Mbps OFDM		-89.4		dBm
	9Mbps OFDM		-88.4		dBm
	12Mbps OFDM		-87.2		dBm
	18Mbps OFDM		-85.0		dBm
	24Mbps OFDM		-82.6		dBm
	36Mbps OFDM		-79.1		dBm
	48Mbps OFDM		-75.8		dBm
	54Mbps OFDM		-74.1		dBm
Sensitivity 802.11n (BW = 20MHz)	MCS 0		-89.5		dBm
	MCS 1		-88.9		dBm
	MCS 2		-87.2		dBm
	MCS 3		-85.0		dBm
	MCS 4		-82.6		dBm
	MCS 5		-79.1		dBm
	MCS 6		-75.8		dBm
	MCS 7		-74.1		dBm
Maximum Receive Signal Level	1-11Mbps DSS		0	5	dBm
	6-54Mbps OFDM		0	1	dBm
	MCS 0 - 7		0	0	dBm

Table 8-1. WINC1500 Receiver Performance (Continued)

Parameter	Description	Min	Typical	Max	Unit
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)			48	dB
	11Mbps DSS (30MHz offset)			46	dB
	6Mbps OFDM (25MHz offset)			37	dB
	54Mbps OFDM (25MHz offset)			18	dB
	MCS 0 - 20MHz BW (25MHz offset)			42	dB
	MCS 7 - 20MHz BW (25MHz offset)			26	dB
Cellular Blocker Immunity	776-794MHz CDMA		-10		dBm
	824-849MHz GSM		-6		dBm
	880-915MHz GSM		-6		dBm
	1710-1785MHz GSM		-10		dBm
	1850-1910MHz GSM		-10		dBm
	1850-1910MHz WCDMA		-18		dBm
	1920-1980MHz WCDMA		-18		dBm

8.3.2 Transmitter Performance

Table 8-2. WINC1500 Transmitter Performance

Parameter	Description	Min	Typical	Max	Unit
Frequency		**2,412**		**2,484**	**MHz**
Output Power	802.11b DSSS 1Mbps		19.0[(1)]	19.0[(1)]	dBm
	802.11b DSSS 11Mbps		19.0[(1)]	19.0[(1)]	dBm
	802.11g OFDM 6Mbps		17.5[(1)]	17.5[(1)]	dBm
	802.11g OFDM 54Mbps		17.3[(1)]	17.3[(1)]	dBm
	802.11n HT20 MCS 0		15.8[(1)]	15.8[(1)]	dBm
	802.11n HT20 MCS 7		15.8[(1)]	15.8[(1)]	dBm
Tx Power Accuracy			±1.5		dB
Carrier Suppression			30.0		dBc
Return Loss	S11			-8.0	dB

Table 8-2. WINC1500 Transmitter Performance (Continued)

Parameter	Description	Min	Typical	Max	Unit
Out of Band Transmit Power	76-108		-125		dBm/Hz
	776-794		-125		dBm/Hz
	869-960		-125		dBm/Hz
	925-960		-125		dBm/Hz
	1570-1580		-125		dBm/Hz
	1805-1880		-125		dBm/Hz
	1930-1990		-125		dBm/Hz
	2110-2170		-125		dBm/Hz
Harmonic Output Power	2nd		-33		dBm/MHz
	3rd		-38		dBm/MHz

Note: 1. Measured at 802.11 spec compliant EVM / Spectral Mask

8.3.3 Calibration

Atmel WINC1500 device does not require any external calibration to meet the specifications shown in this document. The WINC1500 does however contain nonvolatile memory for customer's optional use.

- Frequency Compensation - Improve frequency accuracy of main system clock based on external crystal
- Power control - Improve output power tolerance beyond limits specified in this document
- MAC address programming

9. External Interfaces

Atmel WINC1500 external interfaces include I^2C for control, SPI and UART for control and data transfer, and six General Purpose Input / Output (GPIO) pins.

9.1 I^2C Interface

9.1.1 Overview

Atmel WINC1500 provides an I^2C bus slave that allows the host processor to read or write any register in the chip. The WINC1500 supports I^2C bus Version 2.1 - 2000.

The I^2C interface, used primarily for control, is a two-wire serial interface consisting of a serial data line (SDA, Pin 33) and a serial clock (SCL, Pin 32). It responds to the seven bit address value 0x60. The WINC1500 I^2C interface can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I^2C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, please refer to the Philips Specification entitled "The I^2C -Bus Specification, Version 2.1".

9.1.2 I^2C Timing

The I^2C is provided in Figure 9-1 and in Table 9-1 on page 17.

Figure 9-1. WINC1500 I^2C Timing Diagram

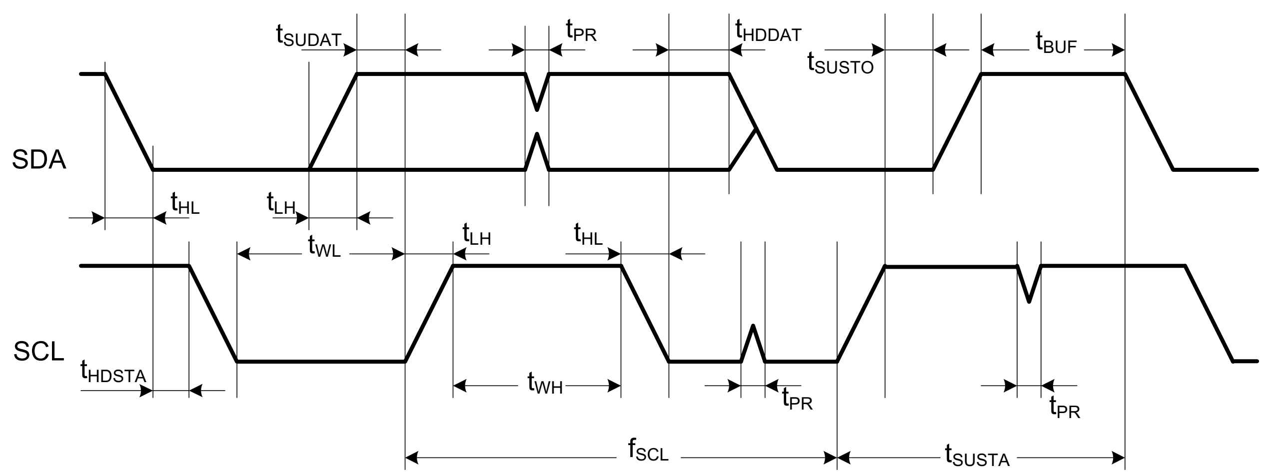


Table 9-1. WINC1500 I^2C Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL clock frequency	f_{SCL}	0	400	kHz	
SCL low pulse width	t_{WL}	1.3		µs	
SCL high pulse width	t_{WH}	0.6		µs	
SCL, SDA fall time	t_{HL}		300	ns	
SCL, SDA rise time	t_{LH}		300	ns	This is dictated by external components
START setup time	t_{SUSTA}	0.6		µs	
START hold time	t_{HDSTA}	0.6		µs	
SDA setup Time	t_{SUDAT}	100		ns	
SDA hold time	t_{HDDAT}	0		ns	Slave and Master default
		40		ns	Master programming option
STOP setup time	t_{SUSTO}	0.6		µs	
Bus free time between STOP and START	t_{BUF}	1.3		µs	
Glitch pulse reject	t_{PR}	0	50	ns	

9.2 SPI Interface

9.2.1 Overview

Atmel WINC1500 device has a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in Table 9-2. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 9-2. WINC1500 SPI Interface Pin Mapping

Pin #	SPI Function
9	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
13	RXD: Serial Data Receive
18	SCK: Serial Clock
17	TXD: Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

9.2.2 SPI Timing

The SPI timing is provided in Figure 9-2 and in Table on page 18

Figure 9-2. WINC1500 SPI Timing Diagram

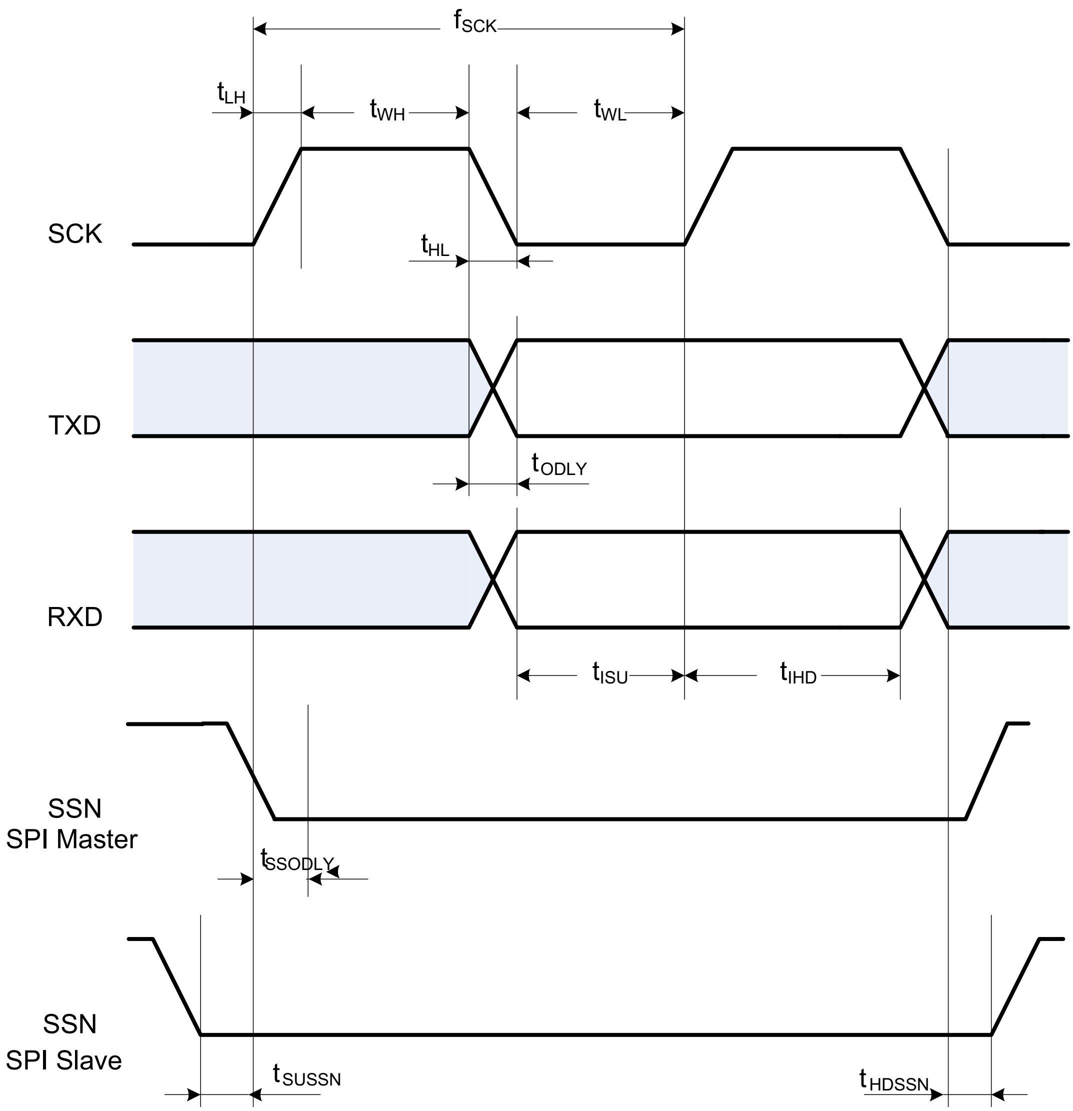


Table 9-3. WINC1500 SPI Slave Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock input frequency	f_{SCK}		48	MHz
Clock low pulse width	t_{WL}	15		ns
Clock high pulse width	t_{WH}	15		ns
Clock rise time	t_{LH}		10	ns
Clock fall time	t_{HL}		10	ns
Input setup time	t_{ISU}	5		ns

Table 9-3. WINC1500 SPI Slave Timing Parameters (Continued)

Parameter	Symbol	Min	Max	Units
Input hold time	t_{IHD}	5		ns
Output Delay	t_{ODLY}	0	20	ns
Slave select setup time	t_{SUSSN}	5		ns
Slave select hold time	t_{HDSSN}	5		ns

9.3 UART

Atmel WINC1500 device has a Universal Asynchronous Receiver / Transmitter (UART) interface. The UART is a standard 2-wire interface (RXD, TXD) with a variety of programmable baud rates for transmission and reception. The software accessible registers allow the programmer to configure the general characteristics of the UART such as the baud rate, clock source and data format. The UART can be configured for 7 or 8 bit operation with or without parity and with one or two stop bits. FIFOs ensure reliable high speed reception and low software overhead transmission. FIFO status can be monitored through transmit and receive status registers.

9.4 GPIOs

Six-General Purpose Input / Output (GPIO) pins are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input.

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Table 10-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD_1P3	1.2V supply voltage	-0.3	1.5	V
VDDIO	I/O supply voltage	-0.3	3.6	V
VBATT	Battery supply voltage	-0.3	6.0	V
V_{IN}	Digital input voltage	-0.3	VDDIO+0.3 (up to 3.6)	V
V_{AIN}(1)	Analog input voltage	-0.3		V
V_{ESDHBM}(2)	ESD human body model	-1000, -2000	+1000, +2000	V
T_A	Storage temperature	-65	150	°C
	Junction temperature		125	°C
	RF input power max		16	dBm

Notes:
1. V_{AIN} is for the following analog pins: VDD_RF, RFIOP, RFION, VDD_AMS, XO_N, XO_P, VDD_SXDIG, VDD_VCO
2. For V_{ESDHBM}, each pin is classified as Class1 or Class2
   - The Class1 pins are: TP_P, VDD_RF, RFIOP, RFION, PALDO_OUT, VDD_BATT, VDD_AMS, EFUSE_VDDQ, VBATT_BUCK, VSW, VREG_BUCK, CHIP_EN, XO_N, XO_P, VDD_SXDIG, VCC_VCO, VDDA_IO, TPN. All others are Class2 pins.
   - V_{ESDHBM} is 1kV for Class1 pins. V_{ESDHBM} is 2kV for Class2 pins.

10.2 Recommended Operating Conditions

Table 10-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD_1P2	1.2V supply voltage	1.235	1.30	1.356	V
$VDDIO_L$	I/O supply voltage low range	1.62	1.80	1.98	V
$VDDIO_M$	I/O supply voltage mid range	2.25	2.50	2.75	V
$VDDIO_H$	I/O supply voltage high range	3.00	3.30	3.60	V
VBATT	Battery supply voltage	2.50(1)	3.60	4.20	V
	Operating temperature	-20		85	°C

Note:
1. The Atmel WINC1500 is functional across this range of voltages; however, optimal RF performance is guaranteed for VBATT in the range 3.0V < VBATT < 4.2V.

10.3 DC Characteristics

The Table 10-3 provides the DC characteristics for the digital pads.

Table 10-3. Recommended Operating Conditions

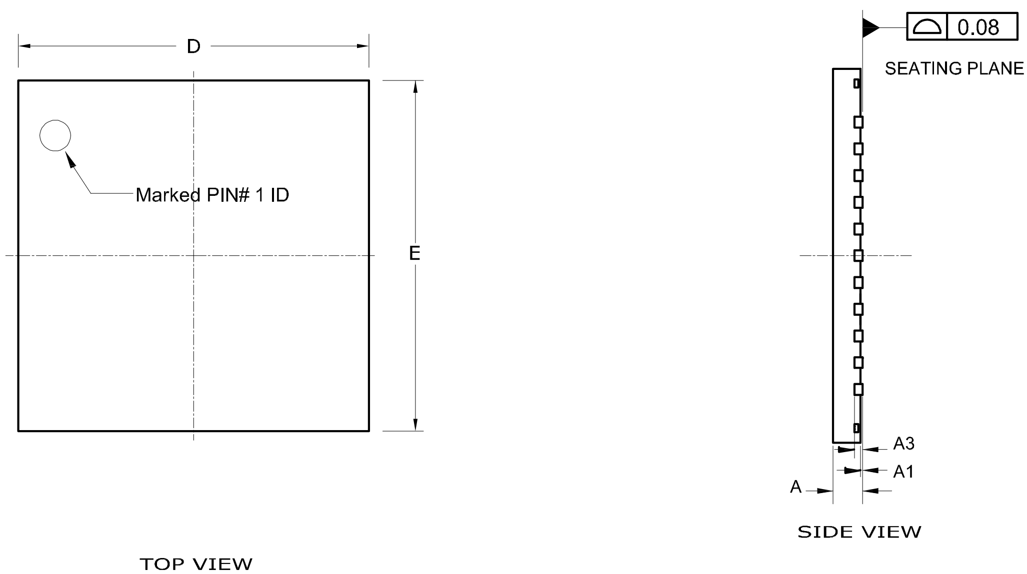
VDDIO	Condition	Min	Max	Unit
$VDDIO_L$	Input low voltage V_{IL}	-0.30	0.63	V
	Input high voltage V_{IH}	1.17	VDDIO+0.30	V
	Output low voltage V_{OL}		0.45	V
	Output high voltage V_{OH}	1.35		V
$VDDIO_M$	Input low voltage V_{IL}	-0.30	0.70	V
	Input high voltage V_{IH}	1.70	VDDIO+0.30	V
	Output low voltage V_{OL}		0.70	V
	Output high voltage V_{OH}	1.70		V
$VDDIO_H$	Input low voltage V_{IL}	-0.30	0.80	V
	Input high voltage V_{IH}	2.00	VDDIO+0.30 (up to 3.60)	V
	Output low voltage V_{OL}		0.40	V
	Output high voltage V_{OH}	2.40		V
All	Output loading		20	pF
All	Digital input load		6	pF

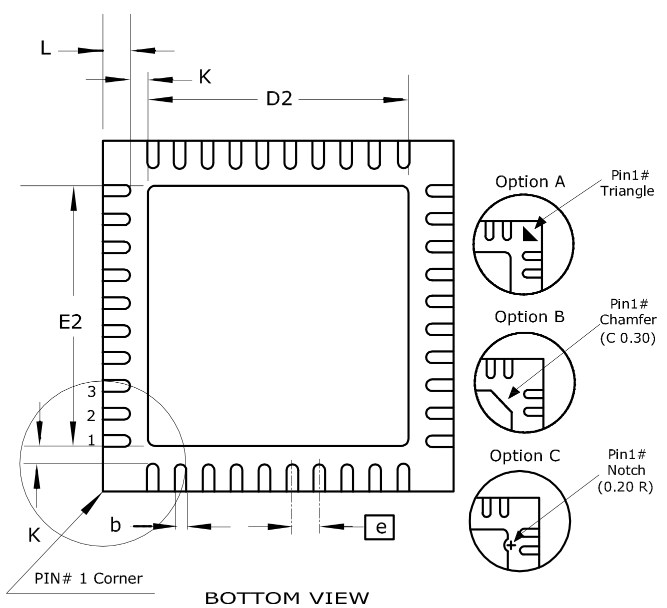
11. Package Drawing

11.1 40QFN 5x5

Figure 11-1. 40QFN Package Drawing

DRAWINGS NOT SCALED





COMMON DIMENSIONS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	-----	0.90
A1	0.00	-----	0.05
A2	-----	0.65	0.70
A3		0.20 REF	
b	0.15	0.2	0.25
D		5.00 bsc	
D2	3.60	3.70	3.80
E		5.00 bsc	
E2	3.60	3.70	3.80
K	0.20	----	----
L	0.35	0.40	0.45
e		0.40 bsc	
R	0.075	-----	----
n		40	

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-1 for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

30/07/2014

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	QFN, 40 Lds - 0.40mm Pitch, 5x5x0.80mm Body size Quad Flat Package (Punched) (QFN)			A

12. Technical Support and Resources

For technical support and other resources visit: http://www.atmel.com/design-support

13. Document History

Doc. Rev.	Date	Comments
42353A	09/2014	Initial release.

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