

## FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - > 1.0GHz  $f_{MAX}$
  - < 20ps within-device skew
  - < 225ps rise/fall times
- **Low jitter design:**
  - Cycle-to-cycle: < 1ps (rms)
  - Total jitter: < 10ps (pk-pk)
- **Low voltage 2.5V and 3.3V supply operation**
- **Four differential 100k LVPECL outputs**
- **Wide operating temperature range: -40°C to +85°C**
- **Includes a 2:1 MUX select input**
- **Accepts single-ended TTL/CMOS inputs and provides four LVPECL outputs**
- **Available in 16-pin (3mm x 3mm) MLF™ package**



Precision Edge™

## DESCRIPTION

The SY89834U is a high-speed, 2GHz LVTTTL/CMOS-to-LVPECL fanout buffer/translator optimized for high-speed ultra-low skew applications. The input stage is designed to accept two single-ended LVTTTL/CMOS compatible signals that feed into a 2:1 MUX. The selected input is translated and distributed as four differential 100K compatible LVPECL outputs. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

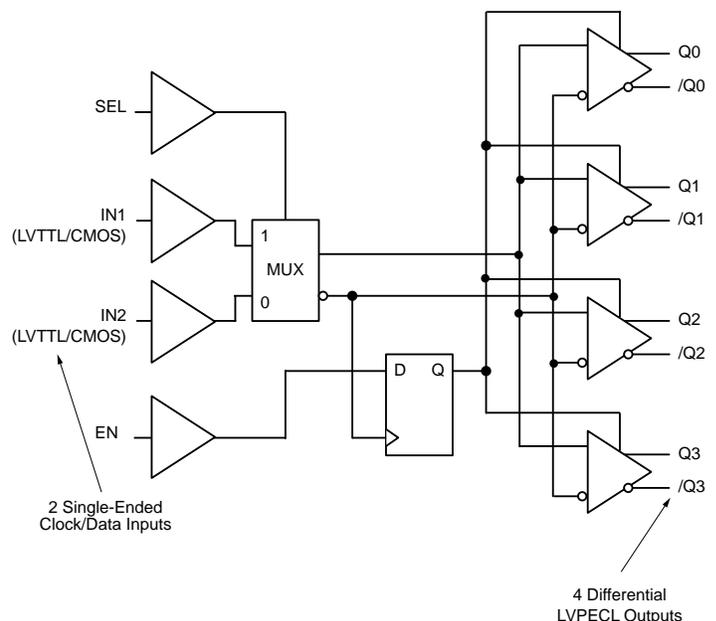
The single-ended input buffers accept TTL/CMOS logic levels. The internal threshold of the buffers is defined as  $V_{CC}/2$ .

The SY89834U is a part of Micrel's high-speed Precision Edge™ family. For applications that require a different I/O combination, consult Micrel's website at [www.micrel.com](http://www.micrel.com), and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

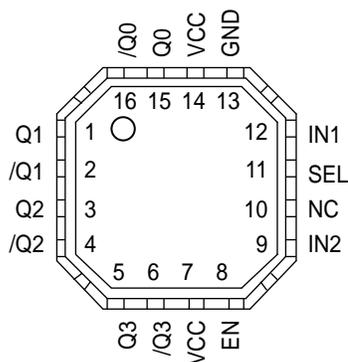
## APPLICATIONS

- **Processor clock distribution/translation**
- **SONET clock distribution/translation**
- **Fibre Channel clock distribution/translation**
- **Gigabit Ethernet clock distribution/translation**
- **Single-ended ASIC-to-differential communication IC signal translation**

## FUNCTIONAL BLOCK DIAGRAM



**PACKAGE/ORDERING INFORMATION**



16-Pin MLF™

**Ordering Information**

Part Number	Package Type	Operating Range	Package Marking
SY89834UMI	MLF-16	Industrial	834U
SY89834UMITR*	MLF-16	Industrial	834U

\*Tape and Reel

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
15, 16 1, 2, 3, 4, 5, 6	(Q0, /Q0) to (Q3, /Q3)	LVPECL Differential (Outputs): Terminate to V <sub>CC</sub> -2V. See "Termination Recommendations" section. Unused outputs may be left floating without impacting jitter and skew.
8	EN	TTL/CMOS Compatible Synchronous Enable: When EN goes LOW, Q outputs will go LOW and /Q outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V <sub>CC</sub> /2V. Includes a 25kΩ pull-up resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal (IN1, IN2).
9, 12	IN2, IN1	TTL/CMOS Compatible Data/Clock (Inputs): IN1 and IN2 include a 25kΩ pull-up resistor. The default state is HIGH when left floating.
10	NC	No Connect. Not internally connected.
11	SEL	TTL/CMOS Compatible Select Input for signals IN1 and IN2. The input threshold is V <sub>CC</sub> /2V. HIGH at the SEL input selects signal IN1. LOW at the SEL input selects signal IN2. SEL includes a 25kΩ pull-up resistor. The default state is HIGH when left floating.
13, Exposed Pad	GND	Ground. Exposed pad internally connected to GND and must be connected to a ground plane for proper termination.
7, 14	VCC	Positive Power Supply: Connect V <sub>CC</sub> pins together on the PCB to maintain the same potential. Bypass with 0.1μF//0.01μF low ESR capacitors.

**TRUTH TABLE**

IN1	IN2	EN	SEL	Q0-Q3	/Q0-Q3
0	X	1	1	0	1
1	X	1	1	1	0
X	0	1	0	0	1
X	1	1	0	1	0
X	X	0	X	0 <sup>(1)</sup>	0 <sup>(1)</sup>

**Note 1.** On next negative transition of the input signal (IN).

### Absolute Maximum Ratings<sup>(Note 1)</sup>

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC} + 0.3V$
ECL Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Input Current ( $I_{IN1}, I_{IN2}$ )	$\pm 50mA$
Lead Temperature (Soldering, 10sec.)	220°C
Storage Temperature ( $T_S$ )	-65°C to +150°C

### Operating Ratings<sup>(Note 2)</sup>

Supply Voltage Range	+2.375V to +3.63V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Package Thermal Resistance	
MLF™ ( $\theta_{JA}$ )	
Still-Air	60°C/W
500lfpm	54°C/W
MLF™ ( $\psi_{JB}$ ) Junction-to-Board, <b>Note 3</b>	32°C/W

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

### DC ELECTRICAL CHARACTERISTICS<sup>(Notes 1, 2)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage Range		2.375		3.63	V
$I_{CC}$	Power Supply Current	No load, maximum supply voltage		50	75	mA
$V_{IN}$	Input Voltage Swing	see Figures 2a–2b.	0.1			
$V_{DIFF\_IN}$	Input Differential Swing	see Figures 2a–2b.	0.2			

**Note 1.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and airflow greater than 500lfpm is maintained.

**Note 2.** Specification for packaged product only.

### LVTTL/CMOS INPUTS DC ELECTRICAL CHARACTERISTICS<sup>(Notes 1, 2)</sup>

$V_{CC} = 2.5V \pm 5\%$  or  $V_{CC} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage		0		0.8	V
$I_{IH}$	Input HIGH Current		-125		20	$\mu\text{A}$
$I_{IL}$	Input LOW Current				-300	$\mu\text{A}$

**Note 1.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**Note 2.** Specification for packaged product only.

### (100KEP) LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS<sup>(Notes 1, 2)</sup>

$V_{CC} = 2.5V \pm 5\%$  or  $V_{CC} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage	$R_L = 50\Omega$ to $V_{CC} - 2V$	$V_{CC} - 1.145$	$V_{CC} - 1.020$	$V_{CC} - 0.895$	V
$V_{OL}$	Output LOW Voltage	$R_L = 50\Omega$ to $V_{CC} - 2V$	$V_{CC} - 1.945$	$V_{CC} - 1.820$	$V_{CC} - 1.695$	V
$V_{OUT}$	Output Voltage Swing	see Figures 2a–2b.	550	800	1050	mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	see Figures 2a–2b.	1100	1600	2100	mV

**Note 1.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

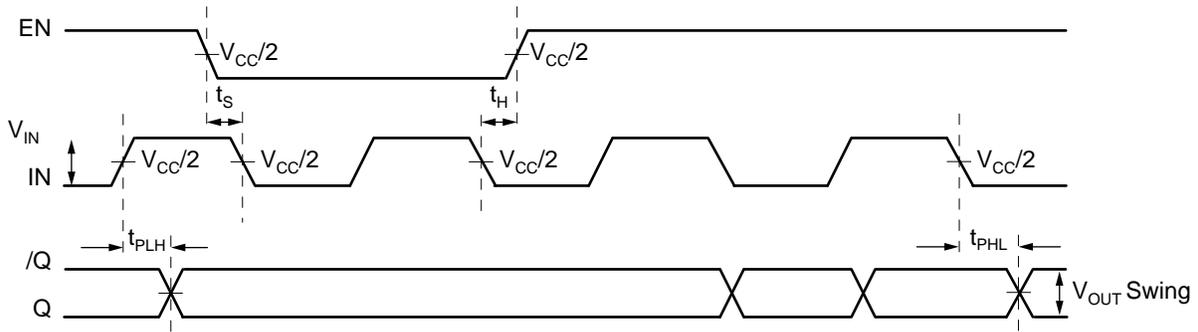
**Note 2.** Specification for packaged product only.

**AC ELECTRICAL CHARACTERISTICS(Notes 1, 2)** $V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ 

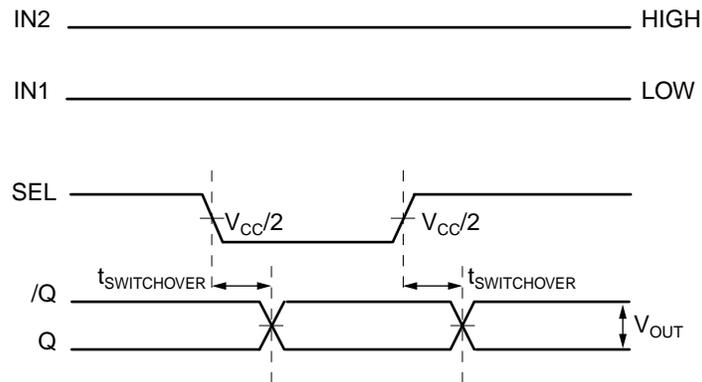
Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Frequency	Input $t_r / t_f \geq 350ps$ , <b>Note 2</b>	1.0			GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay (IN1, IN2-to-Q)	<b>Note 4</b>	200	320	500	ps
$t_{SW}$	Switchover Time (SEL-to-Q)		200	320	500	ps
$t_{SKEW}$	Within-Device Skew	<b>Note 5</b>		5	20	ps
	Part-to-Part Skew				300	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter	<b>Note 6</b> <b>Note 7</b>			1	ps(rms)
	Total Jitter				1	ps(pk-pk)
DC	Duty Cycle	Input $t_r/t_f \geq 350ps$ , <b>Note 8</b>	45	50	55	%
$t_S$	Set-Up Time (EN to IN1, IN2)	<b>Note 9 and Note 10</b>	300			ps
$t_H$	Hold Time (EN to IN1, IN2)	<b>Note 9 and Note 10</b>	500			ps
$t_r, t_f$	Output Rise/Fall Times (20% to 80%)		70	140	225	ps

**Note 1.** Measured with a 2.0V input signal, 50% duty cycle, all PECL loading with  $50\Omega$  to  $V_{CC}-2V$ . Output swing is  $\geq 400mV$ .**Note 2.** Specification for packaged product only.**Note 3.**  $f_{MAX}$  is defined as the maximum input frequency while enduring a valid output.  $f_{MAX}$  is limited by the input stage.**Note 4.**  $V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$ , 50% duty cycle. Delay measured at 100MHz from the crossing of the input signal with  $V_{CC}/2$  as the crossing of the differential output signal. See Figure 1.**Note 5.** Skew is measured between outputs under identical transitions.**Note 6.** Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs.  $T_{JITTER\_CC} = T_n - T_{n+1}$ , where T is the time between rising edges of the output signal.**Note 7.** Total jitter definition: with an ideal clock input frequency of  $\leq f_{MAX}$  (device), no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.**Note 8.** If  $t_r/t_f$  is less than 350ps, the duty cycle distortion will increase beyond the duty cycle limits.**Note 9.** Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications set-up and hold times do not apply.**Note 10.** See "Timing Diagrams," Figure 1a.

**TIMING DIAGRAMS**

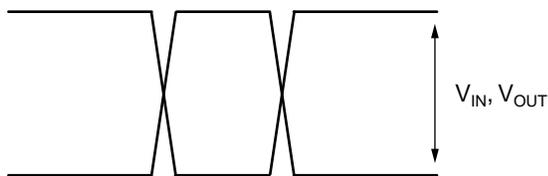


**Figure 1a. Timing Diagram (EN, IN1, IN2)**

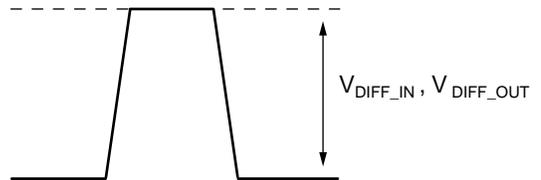


**Figure 1b. Timing Diagram (SEL)**

**DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING**



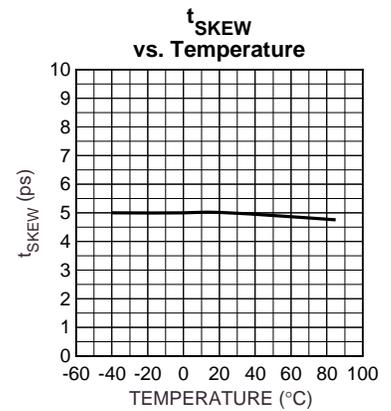
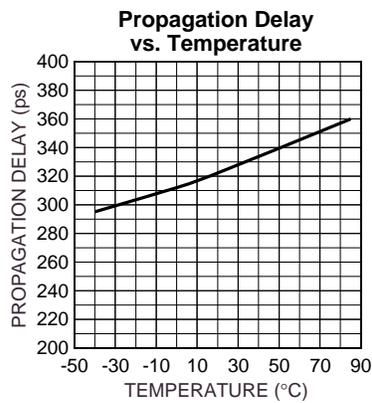
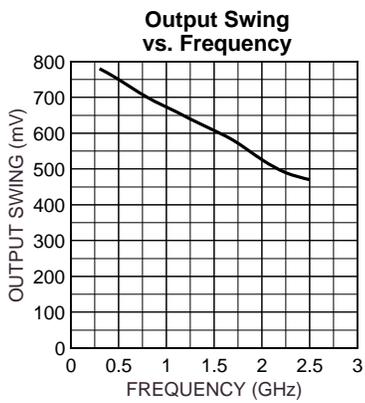
**Figure 2a. Single-Ended Swing**



**Figure 2b. Differential Swing**

**TYPICAL OPERATING CHARACTERISTICS**

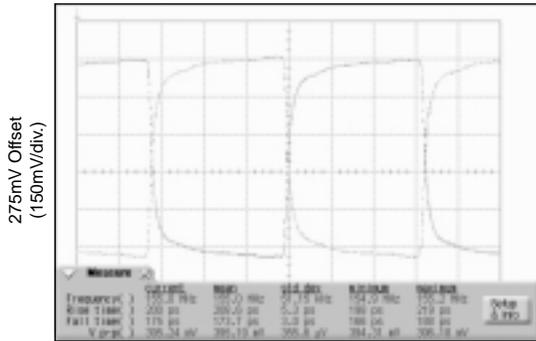
$V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $V_{IN} = 2.0V$ , unless otherwise stated.



**FUNCTIONAL CHARACTERISTICS**

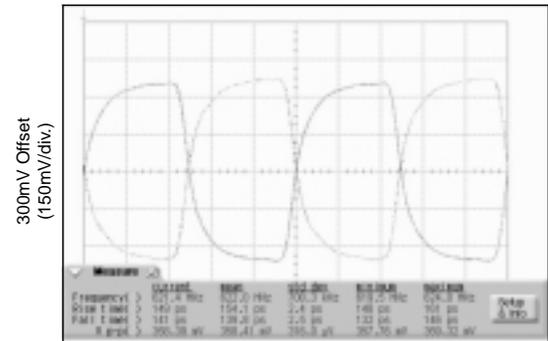
$V_{CC} = 3.3V$ ,  $V_{EE} = 0V$ ,  $V_{IN} = 800mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.

**155MHz Output**



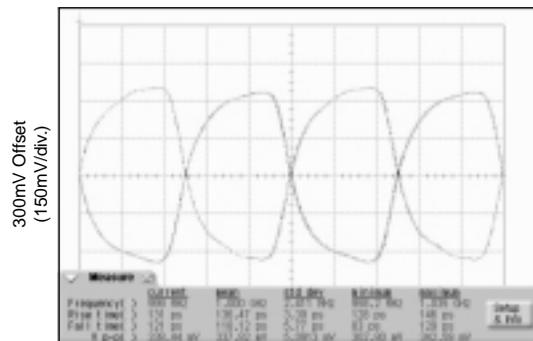
TIME (1ns/div.)

**622MHz Output**



TIME (321.9ps/div.)

**1GHz Output**



TIME (200ps/div.)

**DIFFERENTIAL INPUT**

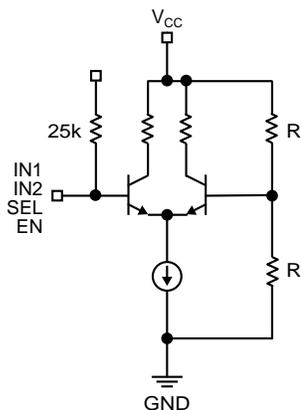
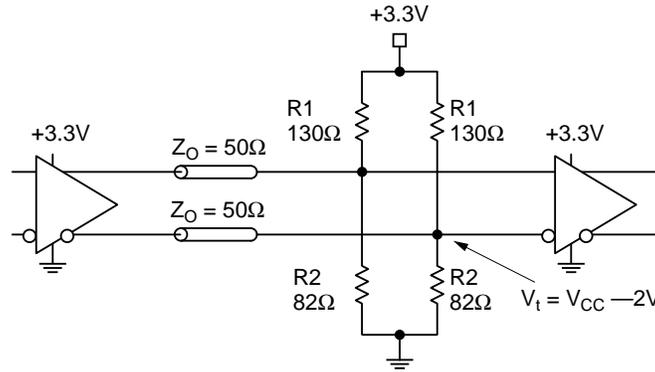


Figure 3. Simplified TTL/CMOS Input Buffer

**RELATED PRODUCTS AND SUPPORT DOCUMENTATION**

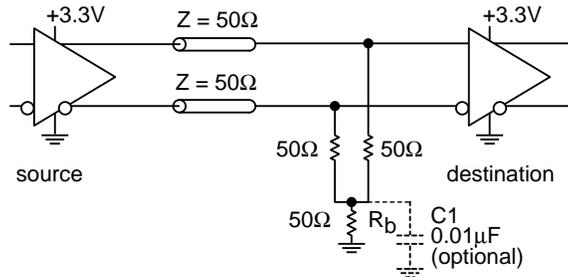
Part Number	Function	Data Sheet Link
SY89830U	2.5V/3.3V/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input Mux	<a href="http://www.micrel.com/product-info/products/sy89830u.shtml">http://www.micrel.com/product-info/products/sy89830u.shtml</a>
SY89831U	2GHz Ultra Low-Jitter and Skew 1:4 LVPECL Fanout Buffer/Translator w/ Internal Termination	<a href="http://www.micrel.com/product-info/products/sy89831u.shtml">http://www.micrel.com/product-info/products/sy89831u.shtml</a>
SY89832U	2GHz Ultra Low-Jitter and Skew 1:4 LVPECL Fanout Buffer/Translator w/ Internal Termination	<a href="http://www.micrel.com/product-info/products/sy89832u.shtml">http://www.micrel.com/product-info/products/sy89832u.shtml</a>
SY89833U	2GHz Any Differential INPUT-to-LVDS Out 1:4 Fanout Buffer Translator w/ Internal Termination	<a href="http://www.micrel.com/product-info/products/sy89833u.shtml">http://www.micrel.com/product-info/products/sy89833u.shtml</a>
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	<a href="http://www.amkor.com/products/notes-papers/MLF-appnote-0301.pdf">http://www.amkor.com/products/notes-papers/MLF-appnote-0301.pdf</a>
HBW Solutions	New Products + Termination App Note	<a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>

**TERMINATION RECOMMENDATIONS**



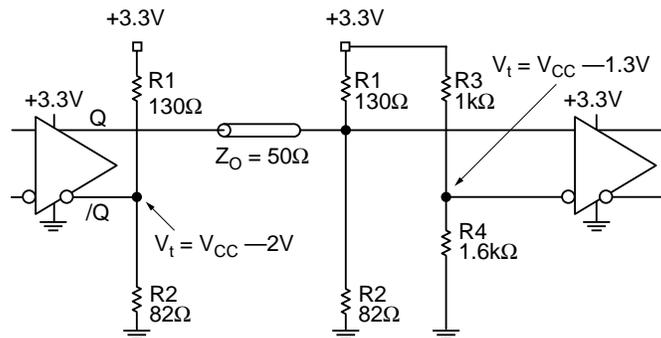
**Figure 4a. Parallel Termination-Thevenin Equivalent**

- Note 1.** For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω  
For +3.3V systems: R1 = 130Ω, R2 = 82Ω



**Figure 4b. Three-Resistor "Y-Termination"**

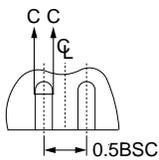
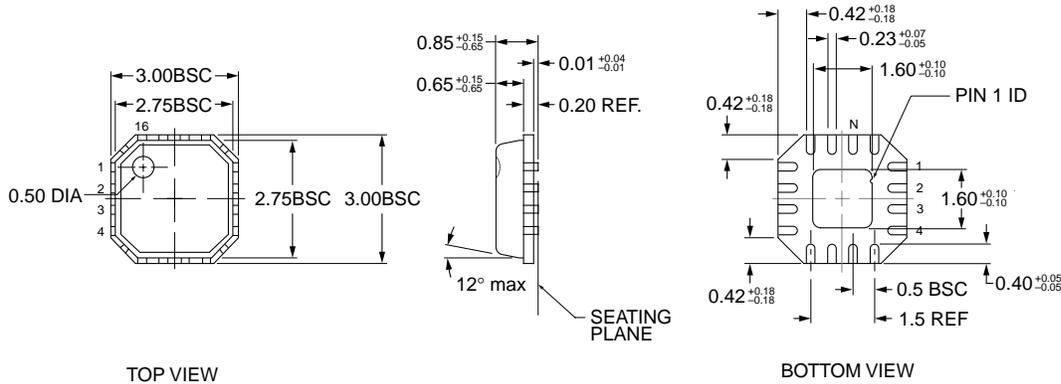
- Note 1.** Power-saving alternative to Thevenin termination.  
**Note 2.** Place termination resistors as close to destination inputs as possible.  
**Note 3.** R<sub>b</sub> resistor sets the DC bias voltage, equal to V<sub>t</sub>. For +3.3V systems R<sub>b</sub> = 50Ω. For +2.5V systems R<sub>b</sub> = 39Ω.



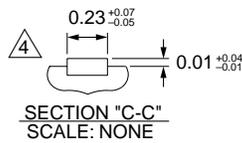
**Figure 4c. Terminating Unused LVPECL I/O**

- Note 1.** Unused output (/Q) must be terminated to balance the output.  
**Note 2.** For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.  
**Note 3.** Unused output pairs (Q and /Q) may be left floating.

**16 LEAD EPAD *MicroLeadFrame*™ (MLF-16)**

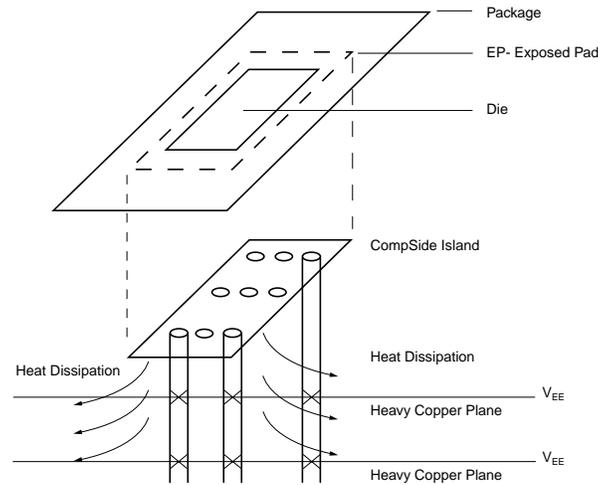


FOR EVEN TERMINAL/SIDE



1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02



**PCB Thermal Consideration for 16-Pin MLF™ Package  
(Always solder, or equivalent, the exposed pad to the PCB.)**

**Package Notes:**

- Note 1.** Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
- Note 2.** Exposed pads must be soldered to a ground for proper thermal management.

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