

3.3V 1:4 CLOCK DISTRIBUTION

Precision Edge[®] SY100EL15L

FEATURES

- 3.3V power supply
- 50ps output-to-output skew
- Low power
- Synchronous enable/disable
- Multiplexed clock input
- 75KΩ internal input pull-down resistors
- Available in 16-pin SOIC package



Precision Edge[®]

DESCRIPTION

The SY100EL15L is a low skew 1:4 clock distribution IC designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. If a single-ended input is to be used the VBB output should be connected to the CLK input and bypassed to ground via a 0.01 μ F capacitor. The VBB output is designed to act as the switching reference for the input of the EL15 under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor) the SEL pin will select the differential clock input.

The common enable (EN) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/ disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

When both differential inputs are left open, CLK input will pull down to VEE and \overline{CLK} input will bias around Vcc/2.

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
SCLK	Synchronous Clock Input
ĒN	Synchronous Enable
SEL	Clock Select Input
VBB	Reference Output
Q0-3	Differential Clock Outputs

TRUTH TABLE

CLK	SCLK	SEL	ĒN	Q
L	Х	L	L	L
Н	Х	L	L	Н
Х	L	Н	L	L
Х	Н	Н	L	Н
Х	Х	Х	Н	L*

* On next negative transition of CLK or SCLK

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PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EL15LZC	Z16-2	Commercial	SY100EL15LZC	Sn-Pb
SY100EL15LZCTR ⁽²⁾	Z16-2	Commercial	SY100EL15LZC	Sn-Pb
SY100EL15LZI	Z16-2	Industrial	SY100EL15LZI	Sn-Pb
SY100EL15LZITR ⁽²⁾	Z16-2	Industrial	SY100EL15LZI	Sn-Pb
SY100EL15LZG ⁽³⁾	Z16-2	Industrial	SY100EL15LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EL15LZGTR ^(2, 3)	Z16-2	Industrial	SY100EL15LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^{\circ}C$, DC Electricals only.

2. Tape and Reel.

3. Pb-Free package is recommended for new designs.



16-Pin SOIC (Z16-2)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit	
Vee	Power Supply (Vcc = 0V)		-8.0 to 0	VDC
Vin	Input Voltage (Vcc = 0V)		0 to -6.0	VDC
Ιουτ	Output Current			
		-Continuous	50	mA
		–Surge	100	
TLEAD	Lead Temperature (soldering, 20sec.)		+260	°C
ТА	Operating Temperature Range		-40 to +85	°C

-3.0V to -3.8V

Notes:

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.

2. Parametric values specified at: 3 volt Power Supply Range 100EL15L Series

DC ELECTRICAL CHARACTERISTICS

		TA = -	$TA = -40^{\circ}C \qquad TA = 0^{\circ}C$: 0°C	TA = +25°C			TA = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Unit
Vон	Output HIGH Voltage ⁽²⁾	-1085	-880	-1025	-880	-1025	-955	-880	-1025	-880	mV
Vol	Output LOW Voltage ⁽²⁾	-1830	-1555	-1810	-1620	-1810	-1705	-1620	-1810	-1620	mV
Vона	Output HIGH Voltage ⁽³⁾	-1095	_	-1035	_	-1035	—	_	-1035	—	mV
Vola	Output LOW Voltage ⁽³⁾		-1555		-1610	_	_	-1610	_	-1610	mV
Viн	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	_	-880	-1165	-880	mV
VIL	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	—	-1475	-1810	-1475	mV
Ін	Input High Current		150		150	_	—	150	_	150	μΑ
lil	Input LOW Current ⁽⁴⁾ CLK	0.5 300	_	0.5 300	_	0.5 300	_	_	0.5 300		μA
IEE	Power Supply Current		35		35	_	25	35	_	38	mA
Vвв	Output Reference Voltage	-1.38	-1.26	-1.38	-1.26	-1.38	_	-1.26	-1.38	-1.26	V

Notes:

1. This table replaces the three traditionally seen in ECL 100K data books. Outputs are terminated through a 50Ω resistor to -2.0V.

2. VIN = VIH(Max) or VIL(Min).

3. VIN = VIH(Min) or VIL(Max).

4. VIN = VIL(Max).

DC ELECTRICAL CHARA

VEE = 3.3V ±10%; VCC = GND⁽¹⁾

AC ELECTRICAL CHARACTERISTICS

VEE = 3.3V ±10%; VCC = GND⁽¹⁾

		T A = ·	–40°C	TA =	0°C	TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Unit
tPD	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	460 410 410	660 710 710	470 420 420	670 720 720	470 420 420		670 720 720	500 450 470	700 750 750	ps
tskew	Part-to-Part Skew ⁽¹⁾ Within-Device Skew		200 50		200 50		_	200 50		200 50	ps
ts	Setup Time EN	150	_	150	_	150	_	_	150	—	ps
tн	Hold Time EN	400	_	400	—	400	—	—	400	—	ps
Vpp	Minimum Input Swing CLK	250	_	250	_	250	_	_	250	_	mV
VCMR	Common Mode Range ⁽²⁾ VPP < 500mV VPP ≥ 500mV	-2.0 -1.8	0.4 0.4	-2.1 -1.9	-0.4 -0.4	-2.1 -1.9	_	-0.4 -0.4	-2.1 -1.9	-0.4 -0.4	mV
tr tf	Output Rise/Fall TimesQ (20% – 80%)	375	625	325	575	325	—	575	325	575	ps

Notes:

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.

 VCMR is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the VCMR range and the input swing is greater than VPP(Min.) and <1V. The lower end of the VCMR range varies 1:1 with VEE. The numbers in the spec table assume a nominal VEE = -3.3V. Note for PECL operation, the VCMR(Min) will be fixed at 3.3V – |VCMR(Min)|.

16-PIN SOIC .150" WIDE (Z16-2)



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