# **Sensitive Gate Silicon Controlled Rectifiers**

## **Reverse Blocking Thyristors**

PNPN devices designed for line powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in surface mount package for use in automated manufacturing.

#### **Features**

- Sensitive Gate Trigger Current
- Blocking Voltage to 600 V
- Glass Passivated Surface for Reliability and Uniformity
- Surface Mount Package
- These Devices are Pb-Free and are RoHS Compliant

## **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage (Note 1) (Sine Wave, $R_{GK} = 1 \text{ k}\Omega$ $T_{.l} = 25 \text{ to } 110^{\circ}\text{C}$ )	V <sub>DRM,</sub> V <sub>RRM</sub>		V
MCR08B MCR08M		200 600	
On-State Current RMS (All Conduction Angles; T <sub>C</sub> = 80°C)	I <sub>T(RMS)</sub>	0.8	Α
Peak Non-repetitive Surge Current (1/2 Cycle Sine Wave, 60 Hz, T <sub>C</sub> = 25°C)	I <sub>TSM</sub>	8.0	Α
Circuit Fusing Considerations (t = 8.3 ms)	l <sup>2</sup> t	0.4	A <sup>2</sup> s
Forward Peak Gate Power (T <sub>C</sub> = 80°C, t = 1.0 μs)	P <sub>GM</sub>	0.1	W
Average Gate Power (T <sub>C</sub> = 80°C, t = 8.3 ms)	P <sub>G(AV)</sub>	0.01	W
Operating Junction Temperature Range	TJ	-40 to +110	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to +150	°C

#### THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient PCB Mounted per Figure 1	$R_{\theta JA}$	156	°C/W
Thermal Resistance, Junction-to-Tab Measured on Anode Tab Adjacent to Epoxy	$R_{ heta JT}$	25	°C/W
Maximum Device Temperature for Soldering Purposes (for 10 Seconds Maximum)	T <sub>L</sub>	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $V_{DRM}$  and  $V_{RRM}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant source such that the voltage ratings of the devices are exceeded.



#### ON Semiconductor®

http://onsemi.com

## **SCRs** 0.8 AMPERES RMS 200 thru 600 VOLTS



#### **MARKING DIAGRAM**



SOT-223 CASE 318F STYLE 10



CR08x = Device Code

x = B or M

= Assembly Location

= Year W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT			
1 Cathode			
2	Anode		
3	Gate		
4	Anode		

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MCR08BT1G	SOT-223 (Pb-Free)	1000/Tape &Reel
MCR08MT1G	SOT-223 (Pb-Free)	1000/Tape & Reel

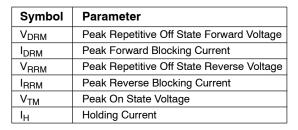
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

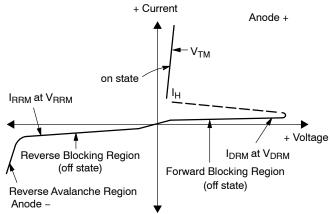
### **ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted)

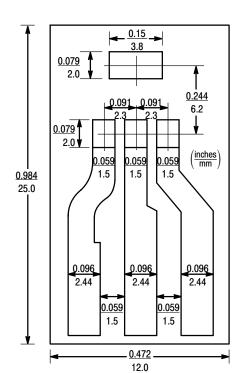
Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Peak Repetitive Forward or Reverse Blocking Current (Note 3) $(V_{AK} = Rated V_{DRM} \text{ or } V_{BRM}, R_{GK} = 1 \text{ k}\Omega$	I <sub>DRM</sub> , I <sub>RRM</sub>				
$T_J = 25^{\circ}\text{C}$ $T_J = 110^{\circ}\text{C}$		_	_ _	10 200	μ <b>Α</b> μ <b>Α</b>
ON CHARACTERISTICS					
Peak Forward On-State Voltage (Note 2) (I <sub>T</sub> = 1.0 A Peak)	V <sub>TM</sub>	_	_	1.7	V
Gate Trigger Current (Continuous dc) (Note 4) ( $V_{AK}$ = 12 Vdc, $R_L$ = 100 $\Omega$ )	I <sub>GT</sub>	-	_	200	μΑ
Holding Current (Note 3) (V <sub>AK</sub> = 12 Vdc, Initiating Current = 20 mA)	I <sub>H</sub>	-	-	5.0	mA
Gate Trigger Voltage (Continuous dc) (Note 4) ( $V_{AK}$ = 12 Vdc, $R_L$ = 100 $\Omega$ )	V <sub>GT</sub>	-	_	0.8	V
Turn-On Time (V <sub>AK</sub> = 12 Vdc, I <sub>TM</sub> = 5 Adc, I <sub>GT</sub> = 5 mA)	t <sub>gt</sub>	_	1.25	-	μs
DYNAMIC CHARACTERISTICS					
Critical Rate-of-Rise of Off State Voltage $(V_{pk} = Rated\ V_{DRM},\ T_C = 110^{\circ}C,\ R_{GK} = 1\ k\Omega,\ Exponential\ Method)$	dv/dt	10	-	-	V/μs

- 2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- 3.  $R_{GK}$  = 1000  $\Omega$  is included in measurement.
- 4. R<sub>GK</sub> is not included in measurement.

## **Voltage Current Characteristic of SCR**







BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR. BOARD THICKNESS = 65 MIL., FOIL THICKNESS = 2.5 MIL. MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

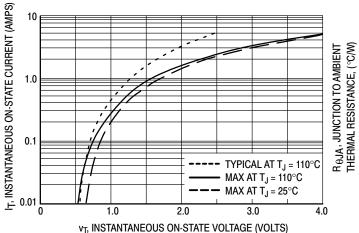


Figure 2. On-State Characteristics

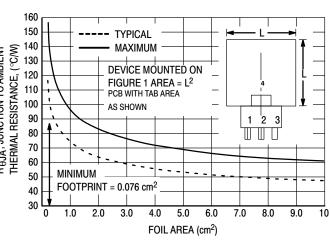


Figure 3. Junction to Ambient Thermal Resistance versus Copper Tab Area

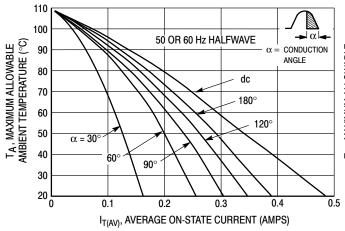


Figure 4. Current Derating, Minimum Pad Size Reference: Ambient Temperature

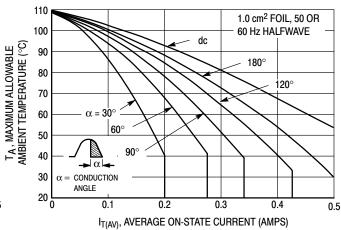


Figure 5. Current Derating, 1.0 cm Square Pad Reference: Ambient Temperature

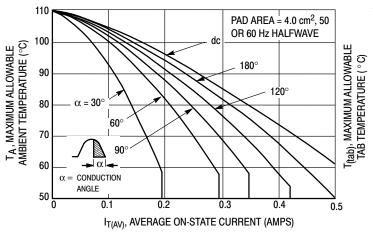


Figure 6. Current Derating, 2.0 cm Square Pad Reference: Ambient Temperature

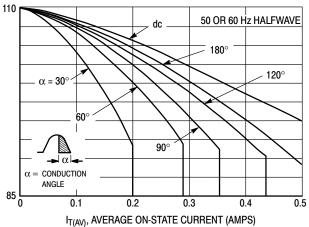


Figure 7. Current Derating Reference: Anode Tab

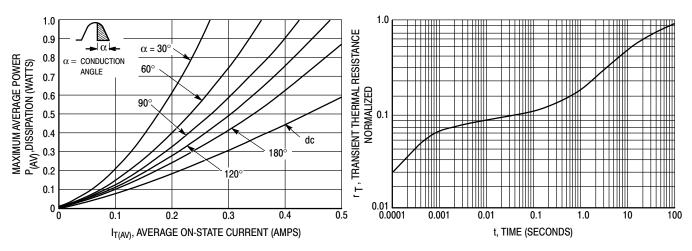


Figure 8. Power Dissipation

Figure 9. Thermal Response Device Mounted on Figure 1 Printed Circuit Board

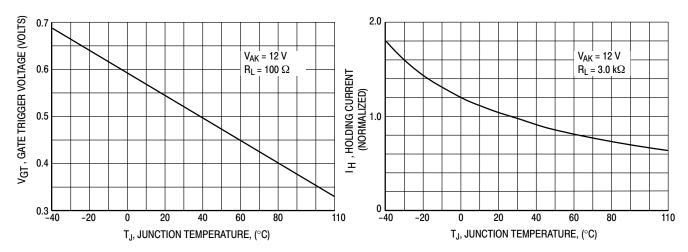


Figure 10. Typical Gate Trigger Voltage versus Junction Temperature

Figure 11. Typical Normalized Holding Current versus Junction Temperature

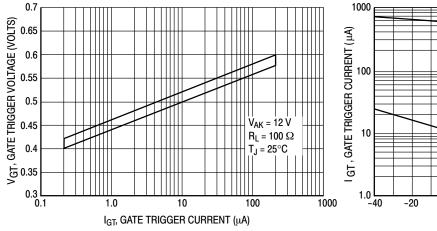


Figure 12. Typical Range of  $V_{GT}$  versus Measured  $I_{GT}$ 

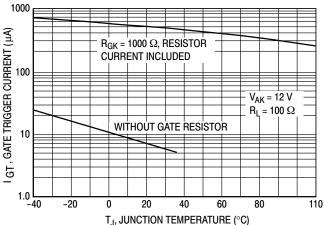


Figure 13. Typical Gate Trigger Current versus Junction Temperature

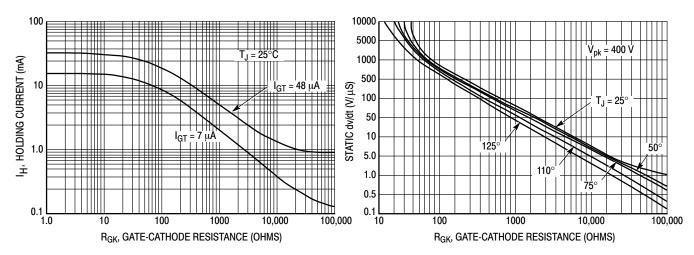


Figure 14. Holding Current Range versus Gate-Cathode Resistance

Figure 15. Exponential Static dv/dt versus Junction Temperature and Gate-Cathode Termination Resistance

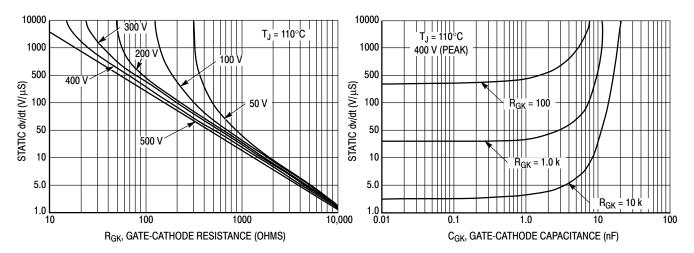


Figure 16. Exponential Static dv/dt versus Peak Voltage and Gate-Cathode Termination Resistance

Figure 17. Exponential Static dv/dt versus Gate-Cathode Capacitance and Resistance

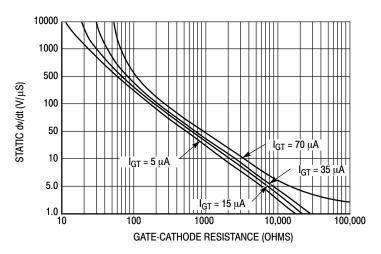
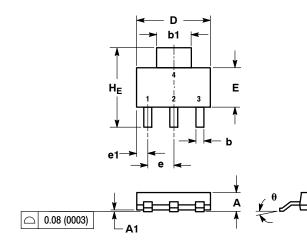


Figure 18. Exponential Static dv/dt versus Gate-Cathode Termination Resistance and Product Trigger Current Sensitivity

#### PACKAGE DIMENSIONS

#### SOT-223 (TO-261) CASE 318E-04 **ISSUE L**



NOTES: DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982

CONTROLLING DIMENSION: INCH.

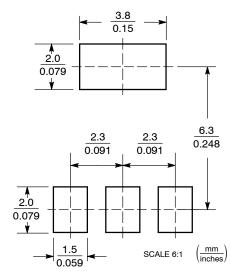
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
С	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
е	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	_	10°	0°	-	10°

STYLE 10:

PIN 1. CATHODE 2. ANODE

GATE
ANODE

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and (III) are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all Claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada

Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910 Japan Customer Focus Center

Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative