

## Single Digitally-Controlled (XDCP™) Potentiometer

The X9118 integrates a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

The digital controlled potentiometer is implemented using 1023 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Power-up recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

## Features

- 1024 Resistor Taps – 10-Bit Resolution
- 2-Wire Serial Interface for Write, Read and Transfer Operations of the Potentiometer
- Wiper Resistance, 40Ω Typical @ 5V
- Four Non-Volatile Data Registers for Each Potentiometer
- Non-Volatile Storage of Multiple Wiper Positions
- Power On Recall: Loads Saved Wiper Position on Power-Up
- Standby Current < 15μA Max
- System V<sub>CC</sub>: 2.7V to 5.5V Operation
- Analog V<sub>+</sub>/V<sub>-</sub>: -5V to +5V
- 100kΩ End to End Resistance
- Endurance: 100,000 Data Changes Per Bit Per Register
- 100 yr. Data Retention
- 14 Ld TSSOP
- Low Power CMOS
- Pb-Free Available (RoHS Compliant)

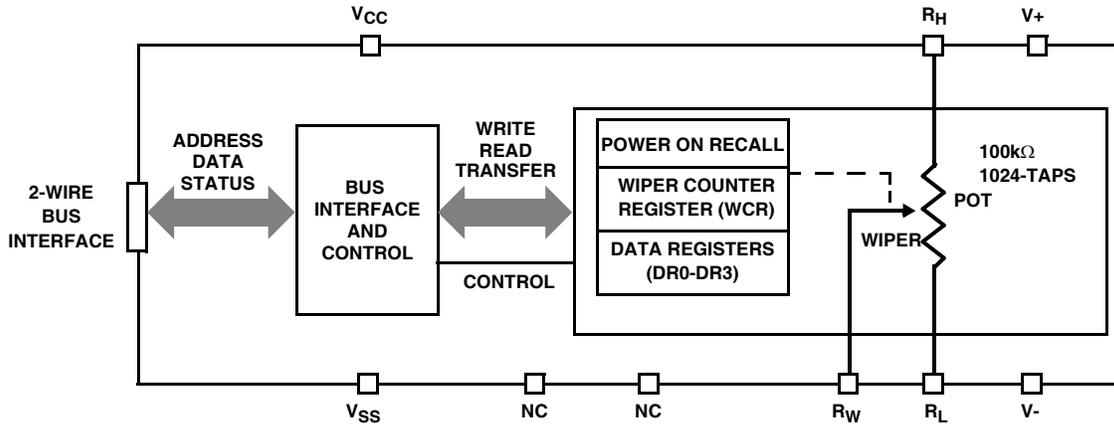
## Ordering Information

PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
X9118TV14	X9118 TV	5 ±10%	100	0 to +70	14 Ld TSSOP	M14.173
X9118TV14Z (Note 1)	X9118 TVZ			0 to +70	14 Ld TSSOP (Pb-free)	M14.173
X9118TV14I (Note 2)	X9118 TVI			-40 to +85	14 Ld TSSOP	M14.173
X9118TV14IZ (Note 1)	X9118 TVZI			-40 to +85	14 Ld TSSOP (Pb-free)	M14.173
X9118TV14-2.7 (Note 2)	X9118 TVF	2.7 to 5.5		0 to +70	14 Ld TSSOP	M14.173
X9118TV14Z-2.7 (Note 1)	X9118 TVZF			0 to +70	14 Ld TSSOP (Pb-free)	M14.173
X9118TV14I-2.7 (Note 2)	X9118 TVG			-40 to +85	14 Ld TSSOP	M14.173
X9118TV14IZ-2.7 (Note 1)	X9118 TVZG			-40 to +85	14 Ld TSSOP (Pb-free)	M14.173

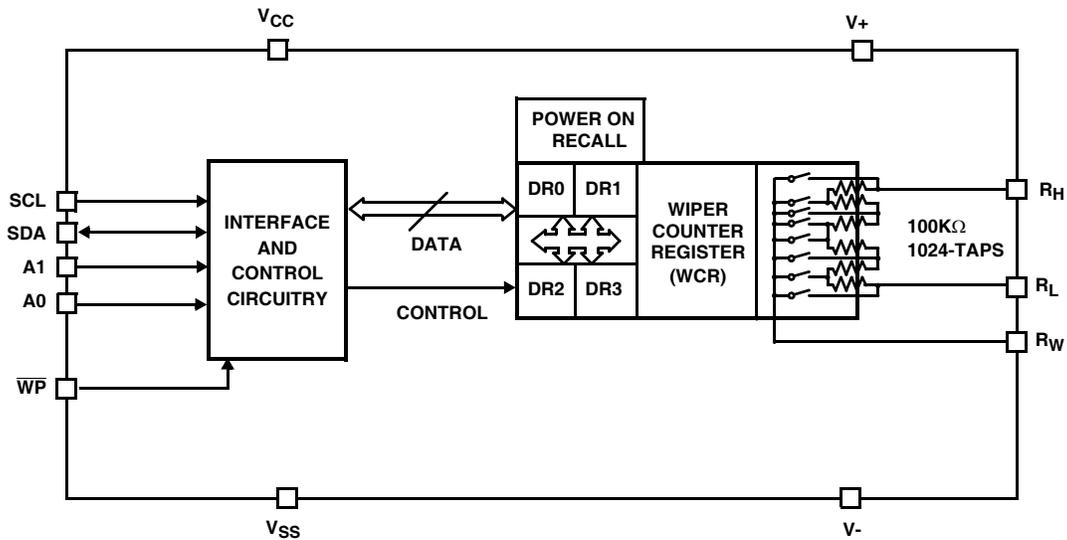
### NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Not recommended for new designs.

**Functional Diagram**



**Detailed Functional Diagram**



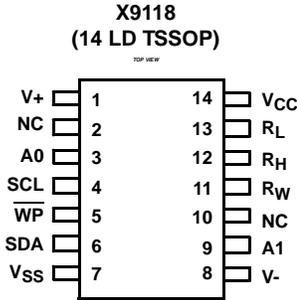
**Circuit Level Applications**

- Vary the gain of a voltage amplifier
- Provide programmable DC reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the DC biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

**System Level Applications**

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

**Pin Configuration**



**Pin Assignments**

PIN (TSSOP)	SYMBOL	FUNCTION
1	V+	Analog Supply Voltage
2	NC	No Connect
3	A0	Device Address for 2-wire bus
4	SCL	Serial Clock for 2-wire bus
5	$\overline{WP}$	Hardware Write Protect
6	SDA	Serial Data Input/Output for 2-wire bus
7	V <sub>SS</sub>	System Ground
8	V-	Analog Supply Voltage
9	A1	Device Address for 2-wire bus
10	NC	No Connect
11	R <sub>W</sub>	Wiper terminal of the Potentiometer
12	R <sub>H</sub>	High terminal of the Potentiometer
13	R <sub>L</sub>	Low terminal of the Potentiometer
14	V <sub>CC</sub>	System Supply Voltage

**Pin Descriptions**

**Bus Interface Pins**

**SERIAL DATA INPUT/OUTPUT (SDA)**

The SDA is a bidirectional serial data input/output pin for a 2-wire slave device and is used to transfer data into and out of the device. It receives device address, opcode, wiper register address and data sent from a 2-wire master at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

**SERIAL CLOCK (SCL)**

This input is used by 2-wire master to supply 2-wire serial clock to the X9118.

**DEVICE ADDRESS (A1–A0)**

The address inputs are used to set the least significant 2 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9118. A maximum of 4 XDCP devices may occupy the 2-wire serial bus.

**HARDWARE WRITE PROTECT INPUT ( $\overline{WP}$ )**

The  $\overline{WP}$  pin when LOW prevents nonvolatile writes to the Data Registers.

**Potentiometer Pins**

**R<sub>H</sub>, R<sub>L</sub>**

The R<sub>H</sub> and R<sub>L</sub> pins are equivalent to the terminal connections on a mechanical potentiometer.

**R<sub>W</sub>**

The wiper pin is equivalent to the wiper terminal of a mechanical potentiometer.

**Bias Supply Pins**

**SYSTEM SUPPLY VOLTAGE (V<sub>CC</sub>) AND SUPPLY GROUND (V<sub>SS</sub>)**

The V<sub>CC</sub> pin is the system or digital supply voltage. The V<sub>SS</sub> pin is the system ground.

**ANALOG SUPPLY VOLTAGES (V+ AND V-)**

These supplies are the analog voltage supplies for the potentiometer. The V+ supply is tied to the wiper switches while the V- supply is used to bias the switches and the internal P+ substrate of the integrated circuit. Both of these supplies set the voltage limits of the potentiometer.

**Other Pins**

**NO CONNECT**

No connect pins should be left open. These pins are used for Intersil manufacturing and testing purposes.

**Principles of Operation**

The X9118 is an integrated microcircuit incorporating a resistor array and its registers and counters and the serial interface logic providing direct communication between the host and the digitally controlled potentiometer. This section provides a detailed description of the following:

- Resistor Array Description
- Serial Interface Description
- Instruction and Register Description

**Resistor Array Description**

The X9118 is comprised of a resistor array. The array contains 1023, in effect, discrete resistive segments that are connected in series (see Figure 1). The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R<sub>H</sub> and R<sub>L</sub> inputs).

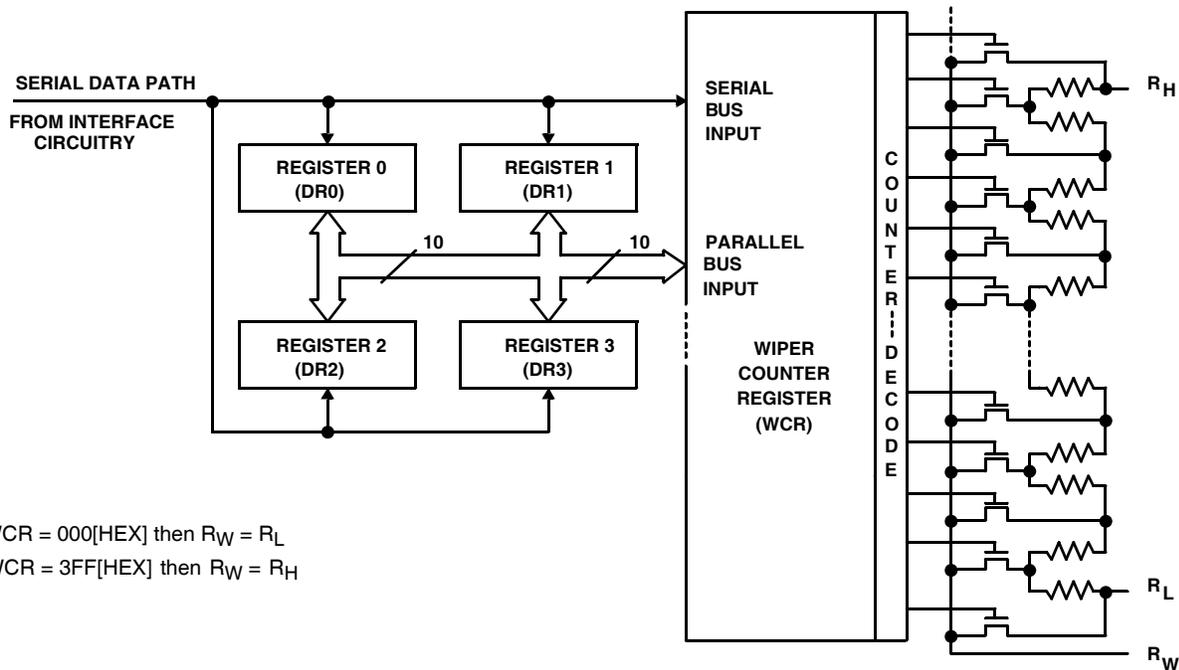


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

At both ends of each array and between each resistor segment is a CMOS switch (transmission gate) connected to the wiper ( $R_W$ ) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The 10-bits of the WCR (WCR[9:0]) are decoded to select, and enable, one of 1024 switches.

The WCR may be written directly. The Data Registers and the WCR can be read and written by the host system.

**Serial Interface Description**

**SERIAL INTERFACE – 2-WIRE**

The X9118 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9118 will be considered a slave device in all applications.

**CLOCK AND DATA CONVENTIONS**

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 3.

**START CONDITION**

All commands to the X9118 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X9118 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met. See Figure 3.

**STOP CONDITION**

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. See Figure 3.

**ACKNOWLEDGE**

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9118 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte, the X9118 will respond with a final acknowledge. See Figure 2.

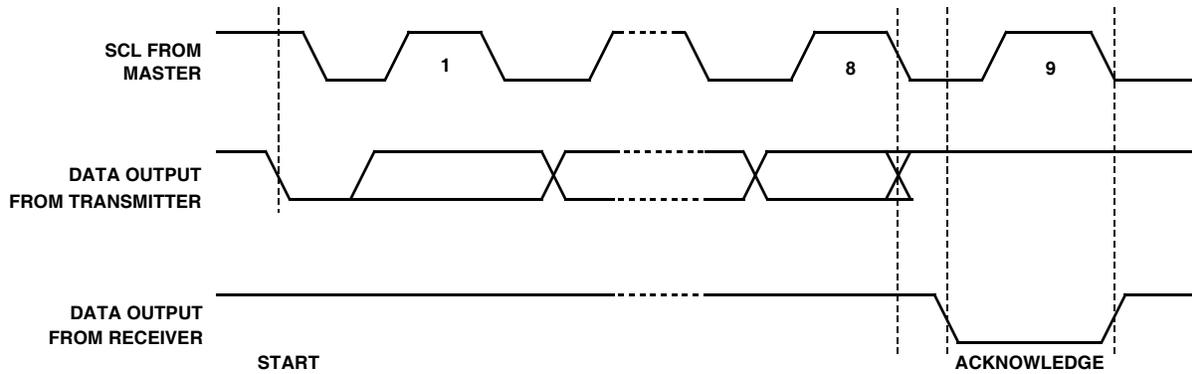
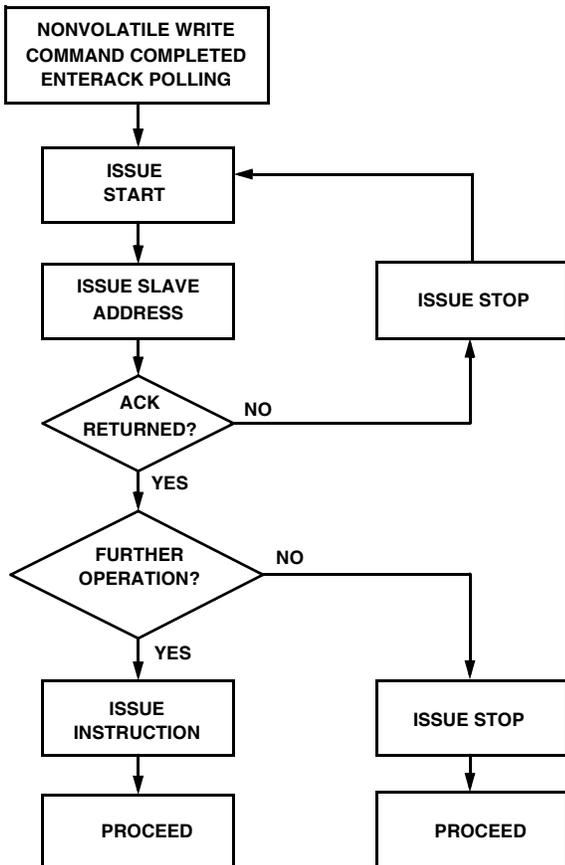


FIGURE 2. ACKNOWLEDGE RESPONSE FROM RECEIVER

**ACKNOWLEDGE POLLING**

The disabling of the inputs during the internal nonvolatile write operation can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9118 initiates the internal write cycle. ACK polling, Flow 1, can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9118 is still busy with the write operation no ACK will be returned. If the X9118 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

**Flow 1. ACK Polling Sequence**



**INSTRUCTION AND REGISTER DESCRIPTION**

**Device Addressing: Identification Byte (ID and A)**

Following a start condition, the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier. The ID[3:0] bits is the device ID for the X9118; this is fixed as 0101[B] (refer to Table 1).

The A[1:0] bits in the ID byte are the internal slave address. The physical device address is defined by the state of the A1-A0 input pins. The slave address is externally specified by the user. The X9118 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9118 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A1-A0 inputs can be actively driven by CMOS input signals or tied to V<sub>CC</sub> or V<sub>SS</sub>. The R/W bit is the LSB and is used to set the device for read or write operations.

**INSTRUCTION BYTE AND REGISTER SELECTION**

The next byte sent to the X9118 contains the instruction and register pointer information. The three most significant bits are used to provide the instruction opcode (I[2:0]). The RB and RA bits point to one of the four registers. The format is shown in Table 2.

Table 3 provides a complete summary of the instruction set opcodes.

TABLE 1. IDENTIFICATION BYTE FORMAT

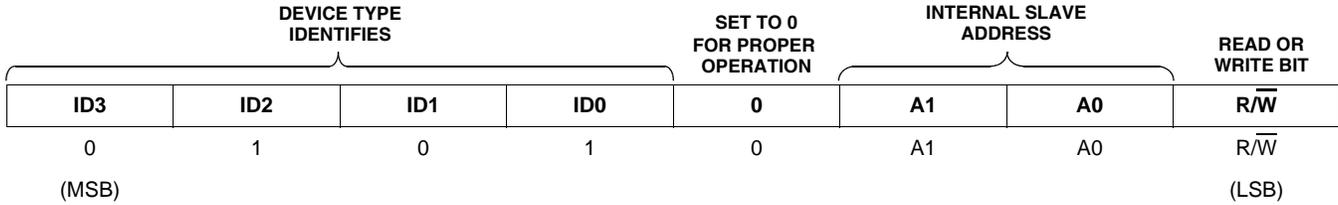
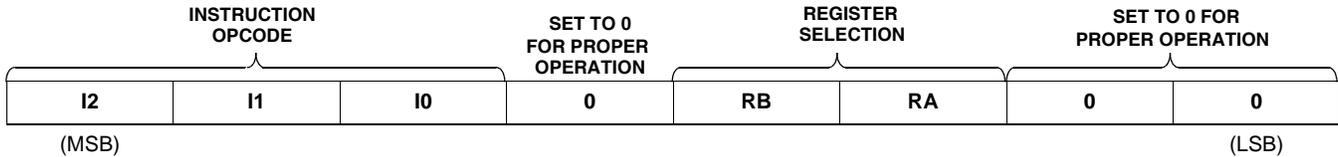


TABLE 2. INSTRUCTION BYTE FORMAT



REGISTER SELECTED	RB	RA
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

TABLE 3. INSTRUCTION SET

INSTRUCTION	R/W	INSTRUCTION SET								OPERATION
		I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	0	RB	RA	0	0	
Read Wiper Counter Register	1	1	0	0	0	0	0	0	0	Read the contents of the Wiper Counter Register
Write Wiper Counter Register	0	1	0	1	0	0	0	0	0	Write new value to the Wiper Counter Register
Read Data Register	1	1	0	1	0	1/0	1/0	0	0	Read the contents of the Data Register pointed to RB-RA.
Write Data Register	0	1	1	0	0	1/0	1/0	0	0	Write new value to the Data Register pointed to RB-RA.
XFR Data Register to Wiper Counter Register	1	1	1	0	0	1/0	1/0	0	0	Transfer the contents of the Data Register pointed to by RB-RA to the Wiper Counter Register
XFR Wiper Counter Register to Data Register	0	1	1	1	0	1/0	1/0	0	0	Transfer the contents of the Wiper Counter Register to the Data Register pointed to by RB-RA.

NOTE:

3. 1/∅ = data is one or zero.

**Instruction and Register Description**

**DEVICE ADDRESSING**

**Wiper Counter Register (WCR)**

The X9118 contains a Wiper Counter Register (see Table 4) for the XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of 1024 switches along its resistor array. The contents of the WCR can be altered in one of three ways:

1. It may be written directly by the host via the write Wiper Counter Register instruction (serial load)
2. It may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data register
3. It is loaded with the contents of its Data Register zero (R0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9118 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR.

**Data Registers (DR)**

The potentiometer has four 10-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four data registers and the Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bit 9–Bit 0 are used to store one of the 1024 wiper position (0 ~1023).

Four of the six instructions are four bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the potentiometer,
- **Write Wiper Counter Register** – change current wiper position of the potentiometer,
- **Read Data Register** – read the contents of the selected Data Register;
- **Write Data Register** – write a new value to the selected Data Register.

The basic sequence of the four byte instructions is illustrated in Figure 3. These four-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a data register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by  $t_{WR}$ . A transfer from the WCR (current wiper position), to a data register is a write to nonvolatile memory and takes a minimum of  $t_{WR}$  to complete. The transfer can occur between the potentiometer and one of its associated registers.

Two instructions (see Figure 4) require a two-byte sequence to complete. These instructions transfer data between the host and the X9118; either between the host and one of the Data Registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** –This transfers the contents of the specified Wiper Counter Register to the specified Data Register.

See “Instruction Format” on page 8 for more details.

**Other**

**POWER-UP AND DOWN REQUIREMENTS**

At all times, the V+ voltage must be greater than or equal to the voltage at  $R_H$  or  $R_L$ , and the voltage at  $R_H$  or  $R_L$  must be greater than or equal to the voltage at V-. During power-up and power down,  $V_{CC}$ , V+, and V- must reach their final values within 1ms of each other.

**TABLE 4. WIPER CONTROL REGISTER, WCR (10-BIT), WCR9–WCR0: USED TO STORE THE CURRENT WIPER POSITION (VOLATILE, V)**

WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V	V	V
(MSB)									(LSB)

**TABLE 5. DATA REGISTER, DR (10-BIT), BIT 9–BIT 0: USED TO STORE WIPER POSITIONS OR DATA (NON-VOLATILE, NV)**

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NV									
MSB									LSB

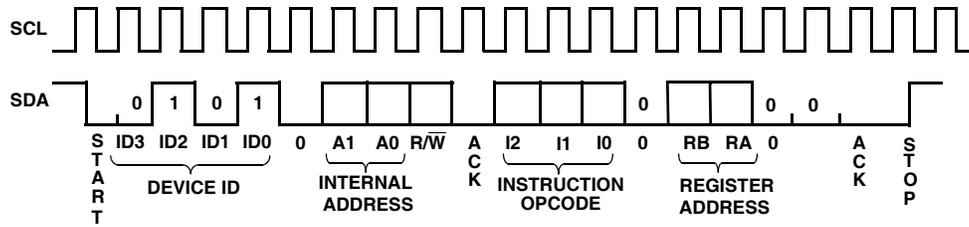


FIGURE 3. TWO-BYTE INSTRUCTION SEQUENCE

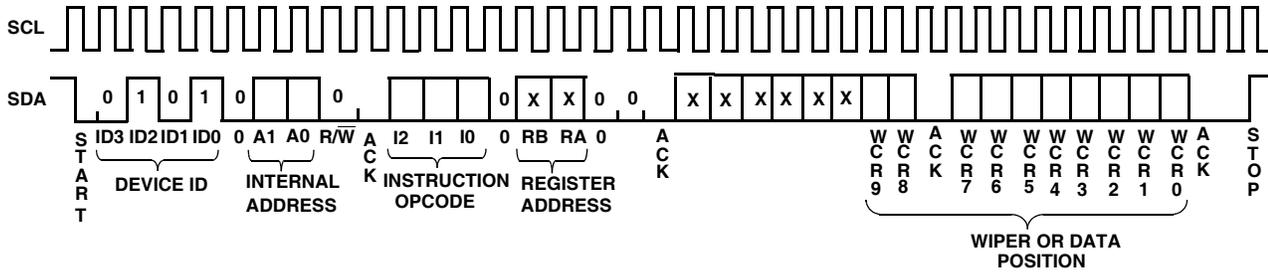


FIGURE 4. FOUR-BYTE INSTRUCTION SEQUENCE (WRITE OR READ FOR WCR OR DATA REGISTERS)

**Instruction Format**

**Read Wiper Counter Register (WCR)**

START	Device Type Identifier				Device Addresses			S A C K	Instruction Opcode				Register Addresses				S A C K	Wiper Position (Sent by Slave on SDA)						M A C K	Wiper Position (Sent by Slave on SDA)						M A C K	STOP
	0	1	0	1	0	A1	A0		R/W = 1	1	0	0	0	0	0	0		0	X	X	X	X	X		X	W C R 9	W C R 8	W C R 7	W C R 6	W C R 5		
	0	1	0	1	0	A1	A0	R/W = 1	1	0	0	0	0	0	0	0	X	X	X	X	X	X	W C R 9	W C R 8	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0

**Write Wiper Counter Register (WCR)**

START	Device Type Identifier				Device Addresses			S A C K	Instruction Opcode				Register Addresses				S A C K	Wiper Position (Sent by Master on SDA)						S A C K	STOP							
	0	1	0	1	0	A1	A0		R/W = 0	1	0	1	0	0	0	0		0	X	X	X	X	X			X	W C R 9	W C R 8	W C R 7	W C R 6	W C R 5	W C R 4
	0	1	0	1	0	A1	A0	R/W = 0	1	0	1	0	0	0	0	0	X	X	X	X	X	X	W C R 9	W C R 8	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0

**Read Data Register (DR)**

START	Device Type Identifier				Device Addresses			S A C K	Instruction Opcode				Register Addresses				S A C K	Wiper Position (Sent by Slave on SDA)						M A C K	Wiper Position or Data (Sent by Slave on SDA)						M A C K	STOP
	0	1	0	1	0	A1	A0		R/W = 1	1	0	1	0	RB	RA	0		0	X	X	X	X	X		X	W C R 9	W C R 8	W C R 7	W C R 6	W C R 5		
	0	1	0	1	0	A1	A0	R/W = 1	1	0	1	0	RB	RA	0	0	X	X	X	X	X	X	W C R 9	W C R 8	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0

**Write Data Register (DR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				Register Addresses				S A C K	Wiper Position or Data (Sent by Master on SDA)						S A C K	Wiper Position or Data (Sent by Master on SDA)						S A C K	S T O P	H I G H- V O L T A G E  W R I T E  C Y C L E	
	0	1	0	1	0	A1	A0	R/W = 0		1	1	0	0	RB	RA	0	0		X	X	X	X	X	X		W C R 9	W C R 8	W C R 7	W C R 6	W C R 5	W C R 4				W C R 3
	0	1	0	1	0	A1	A0	R/W = 0	1	1	0	0	RB	RA	0	0	X	X	X	X	X	X	W C R 9	W C R 8	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0			

**Transfer Wiper Counter Register (WCR) to Data Register (DR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				Register Addresses				S A C K	S T O P	H I G H- V O L T A G E  W R I T E  C Y C L E			
	0	1	0	1	0	A1	A0	R/W = 0		1	1	1	0	RB	RA	0	0						
	0	1	0	1	0	A1	A0	R/W = 0	1	1	1	0	RB	RA	0	0							

**Transfer Data Register (DR) to Wiper Counter Register (WCR)**

S T A R T	Device Type Identifier				Device Addresses				S A C K	Instruction Opcode				Register Addresses				S A C K	S T O P				
	0	1	0	1	0	A1	A0	R/W = 1		1	1	0	0	RB	RA	0	0						
	0	1	0	1	0	A1	A0	R/W = 1	1	1	0	0	RB	RA	0	0							

NOTES:

1. "A1 ~ A0": stands for the device addresses sent by the master.
2. WCRx refers to wiper position data in the Wiper Counter Register.

**Absolute Maximum Ratings**

Temperature Under Bias	-65°C to +135°C
Voltage on SCL, SDA, or Any Address Input with Respect to VSS	-1V to +7V
Voltage on V+ (referenced to V <sub>SS</sub> ) (Note 7)	10V
Voltage on V- (referenced to V <sub>SS</sub> ) (Note 7)	-10V
(V+) – (V-)	12V
Any Voltage on R <sub>H</sub> /R <sub>L</sub>	V+
Any Voltage on R <sub>L</sub> /R <sub>H</sub>	V-
I <sub>W</sub> (10s)	±6mA
Supply Voltage (VCC) Limits (Note 7)	
X9118	5V ±10%
X9118-2.7	2.7V to 5.5V

**Thermal Information**

Thermal Resistance (Typical, Note 3)	θ <sub>JA</sub> (°C/W)
14 Ld TSSOP	110
Storage Temperature	-65°C to +150°C
Pb-Free Reflow Profile	see link below
<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

**Recommended Operating Conditions**

Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Power Rating (each pot)	50mW
Wiper current (max)	±3mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ<sub>JA</sub> is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Analog Specifications** Over the recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
R <sub>TOTAL</sub>	End to End Resistance			100		kΩ
	End to End Resistance Tolerance				±20	%
R <sub>W</sub>	Wiper Resistance	I <sub>W</sub> = (V <sub>RH</sub> - V <sub>RL</sub> )/R <sub>TOTAL</sub> , V <sub>CC</sub> = 3V, V <sub>RL</sub> = -3V		150	500	Ω
R <sub>W</sub>	Wiper Resistance	I <sub>W</sub> = (V <sub>RH</sub> - V <sub>RL</sub> )/R <sub>TOTAL</sub> , V <sub>CC</sub> = 5V, V <sub>RL</sub> = 0V		40	100	Ω
V <sub>v+</sub>	Voltage on V+ Pin	X9118 (Note 7)	+4.5		+5.5	V
		X9118-2.7 (Note 7)	+2.7		+5.5	V
V <sub>v-</sub>	Voltage on V- Pin	X9118	-5.5		-4.5	V
		X9118-2.7	-5.5		-2.7	V
V <sub>TERM</sub>	Voltage on any R <sub>H</sub> or R <sub>L</sub> Pin	V <sub>SS</sub> = 0V	V-		V+	V
	Noise	Ref: 1kHz		-120		dBV
	Resolution			0.1		%
	Absolute Linearity (Note 4)	R <sub>w(n)(actual)</sub> - R <sub>w(n)(expected)</sub> , where n = 1 to 1023			±1.5	MI (Note 6)
	Relative Linearity (Note 5)	R <sub>w(m+1)</sub> - [R <sub>w(m)</sub> + MI], where m = 1 to 1023			±1.5	MI (Note 6)
	Temperature Coefficient of R <sub>TOTAL</sub>			±300		ppm/°C
	Ratiometric Temperature Coefficient	Wiper at middle point		±20		ppm/°C
C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub>	Potentiometer Capacitances	See Macro model		10/10/25		pF

NOTES:

- Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
- Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
- MI = R<sub>TOT</sub>/1023 or (R<sub>H</sub> - R<sub>L</sub>)/1023, single pot
- V<sub>CC</sub>, V<sub>+</sub>, V<sub>-</sub> must reach their final values within 1ms of each other.
- n = 0, 1, 2, ..., 1023; m = 0, 1, 2, ..., 1022.

**DC Operating Specifications** Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current (Active)	f <sub>SCL</sub> = 400kHz; V <sub>CC</sub> = +5.5V; SDA = Open; (for 2-wire, Active, Read and Volatile Write States only)			3	mA
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Nonvolatile Write)	f <sub>SCL</sub> = 400kHz; V <sub>CC</sub> = +5.5V; SDA = Open; (for 2-wire, Active, Non-volatile Write State only)			7	mA
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)	V <sub>CC</sub> = +5.5V; V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub> ; SDA = V <sub>CC</sub> ; (for 2-wire, Standby State only)			15	μA
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>			10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>			10	μA
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> × 0.7		V <sub>CC</sub> + 1	V
V <sub>IL</sub>	Input LOW Voltage		-1		V <sub>CC</sub> × 0.3	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 3mA			0.4	V

**Endurance and Data Retention**

PARAMETER	MIN	UNITS
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	years

**Capacitance**

SYMBOL	TEST	TYP	UNITS	TEST CONDITIONS
C <sub>IN/OUT</sub> (Note 9)	Input/Output Capacitance (SI)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> (Note 9)	Input Capacitance (SCL, $\overline{WP}$ , A1 and A0)	6	pF	V <sub>IN</sub> = 0V

**Power-Up Timing**

SYMBOL	PARAMETER	MIN	MAX	UNITS
t <sub>r</sub> V <sub>CC</sub> (Note 9)	V <sub>CC</sub> Power-up Rate	0.2	50	V/ms
t <sub>PUR</sub> (Note 10)	Power-up to Initiation of Read Operation		1	ms
t <sub>Puw</sub> (Note 10)	Power-up to Initiation of Write Operation		50	ms

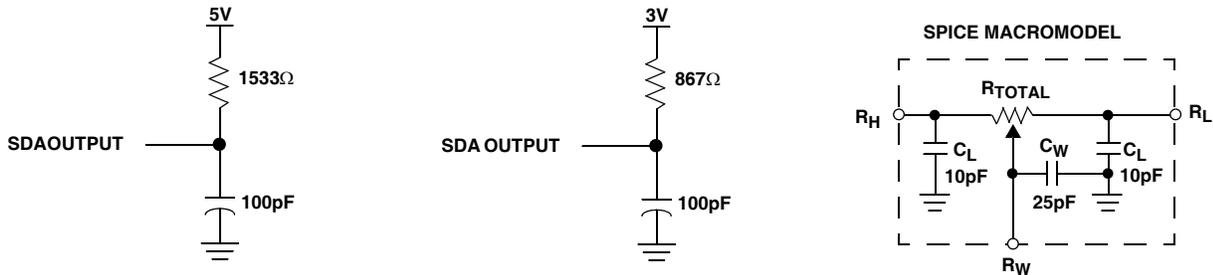
NOTES:

- This parameter is not 100% tested
- t<sub>PUR</sub> and t<sub>Puw</sub> are the delays required from the time the (last) power supply (V<sub>CC</sub>) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

**AC Test Conditions**

Input Pulse Levels	V <sub>CC</sub> × 0.1 to V <sub>CC</sub> × 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V <sub>CC</sub> × 0.5

**Equivalent A.C. Load Circuit**



**AC Timing High-Voltage Write Cycle Timing**

SYMBOL	PARAMETER	MIN	MAX	UNITS
f <sub>SCL</sub>	Clock Frequency		400	kHz
t <sub>CYC</sub>	Clock Cycle Time	2500		ns
t <sub>HIGH</sub>	Clock High Time	600		ns
t <sub>LOW</sub>	Clock Low Time	1300		ns
t <sub>SU:STA</sub>	Start Setup Time	600		ns
t <sub>HD:STA</sub>	Start Hold Time	600		ns
t <sub>SU:STO</sub>	Stop Setup Time	600		ns
t <sub>SU:DAT</sub>	SDA Data Input Setup Time	100		ns
t <sub>HD:DAT</sub>	SDA Data Input Hold Time	30		ns
t <sub>R</sub>	SCL and SDA Rise Time		300	ns
t <sub>F</sub>	SCL and SDA Fall Time		300	ns
t <sub>AA</sub>	SCL Low to SDA Data Output Valid Time	250		ns
t <sub>DH</sub>	SDA Data Output Hold Time	0		ns
t <sub>i</sub>	Noise Suppression Time Constant at SCL and SDA inputs	50		ns
t <sub>BUF</sub>	Bus Free Time (Prior to Any Transmission)	1300		ns
t <sub>SU:WPA</sub>	A0, A1 Setup Time	0		ns
t <sub>HD:WPA</sub>	A0, A1 Hold Time	0		ns

**High-Voltage Write Cycle Timing**

SYMBOL	PARAMETER	TYP	MAX	UNITS
t <sub>WR</sub>	High-Voltage Write Cycle Time (store instructions)	5	10	ms

**XDCP Timing**

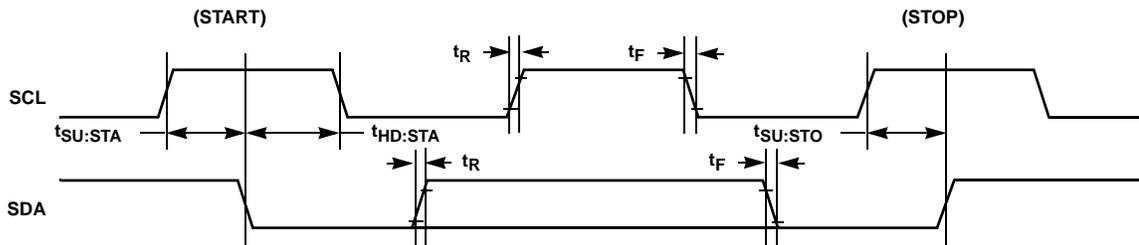
SYMBOL	PARAMETER	TYP	UNITS
t <sub>WRPO</sub>	Wiper Response Time After the Third (last) Power Supply is Stable	8	μs
t <sub>WRL</sub>	Wiper Response Time After Instruction Issued (all load instructions)	8	μs

**Symbol Table**

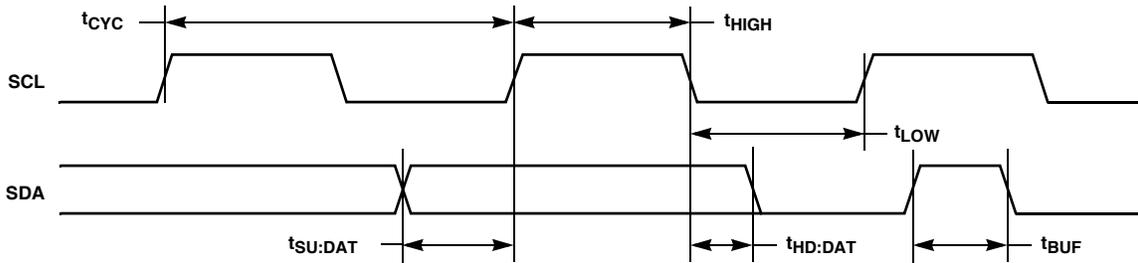
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**Timing Diagrams**

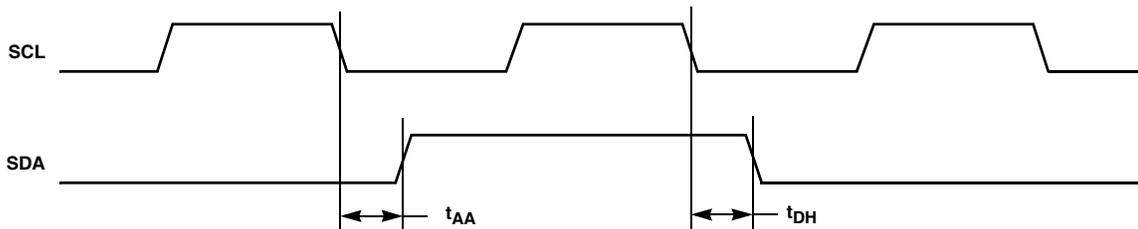
**Start and Stop Timing**



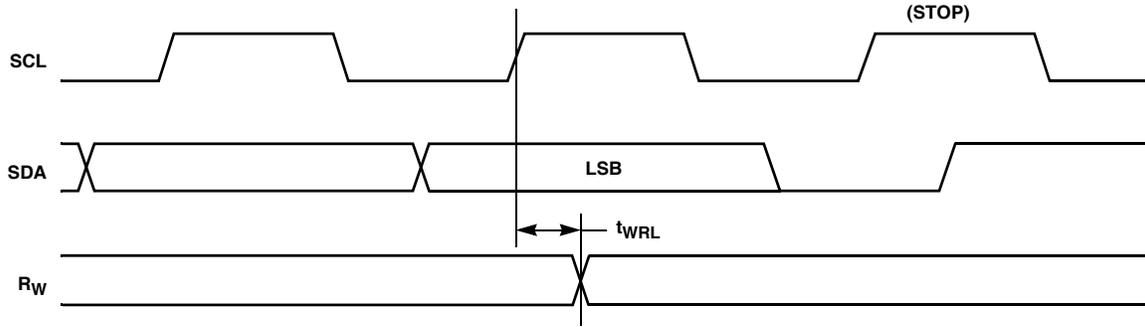
**Input Timing**



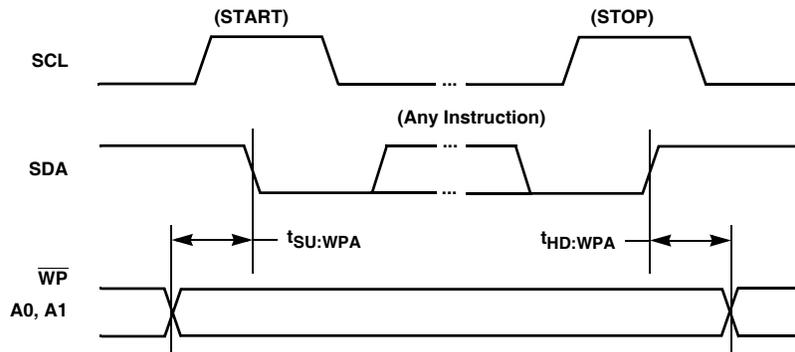
**Output Timing**



**XDCP Timing (For All Load Instructions)**

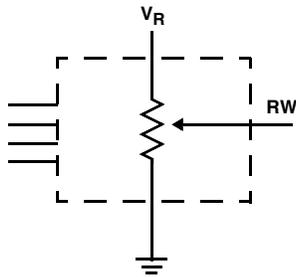


**Write Protect and Device Address Pins Timing**

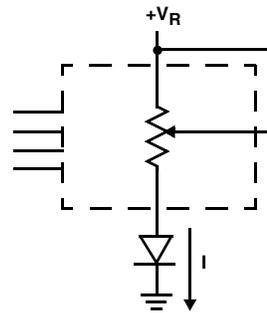


**Applications Information**

**Basic Configurations of Electronic Potentiometers**



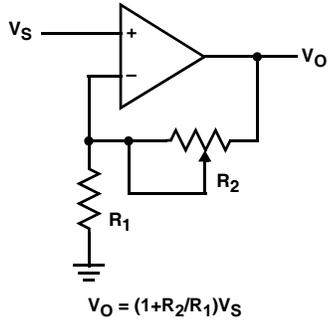
Three terminal Potentiometer;  
Variable voltage divider



Two terminal Variable Resistor;  
Variable current

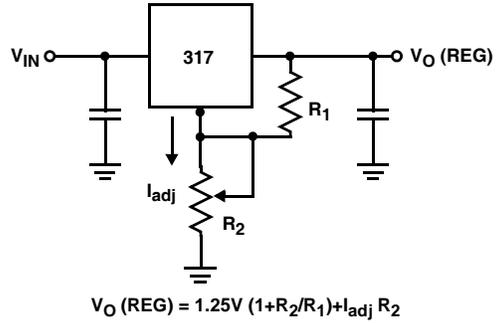
Application Circuits

NONINVERTING AMPLIFIER



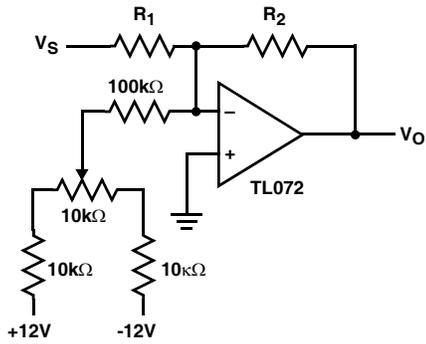
$$V_O = (1 + R_2/R_1)V_S$$

VOLTAGE REGULATOR

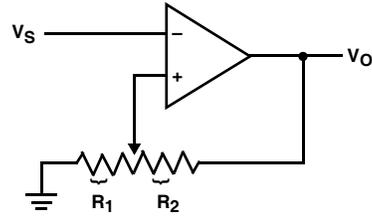


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

OFFSET VOLTAGE ADJUSTMENT



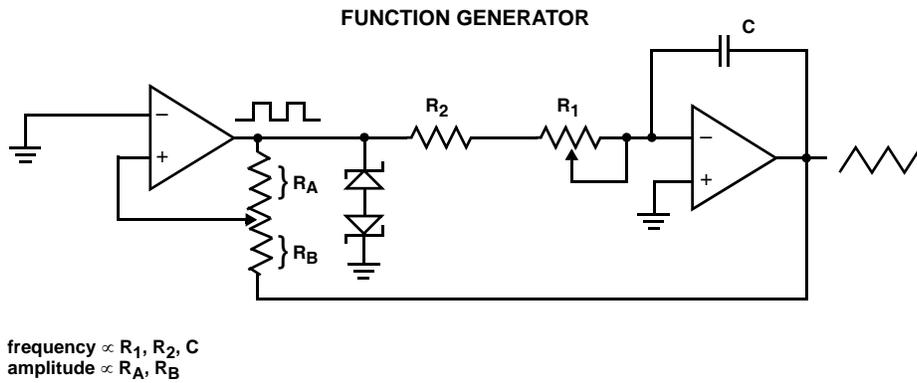
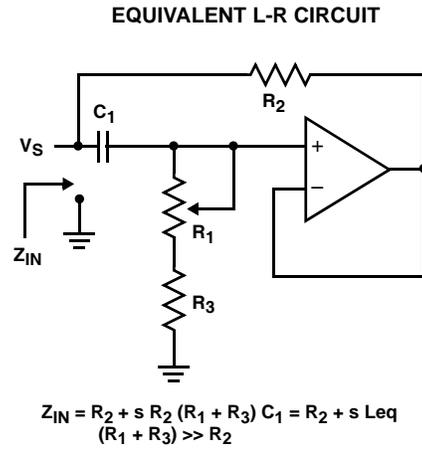
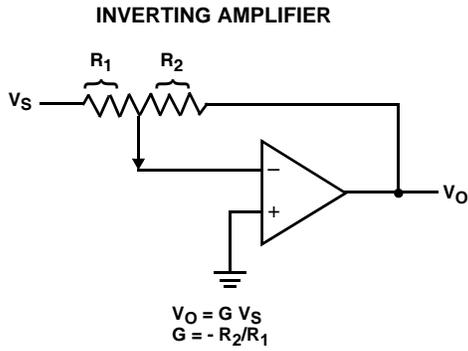
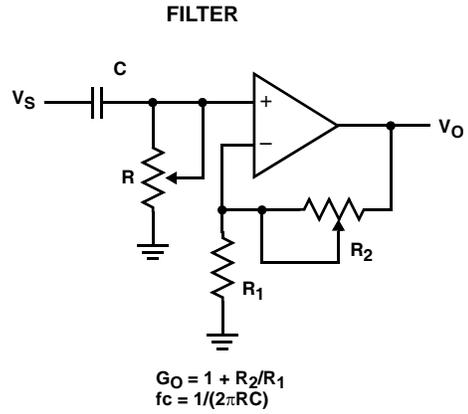
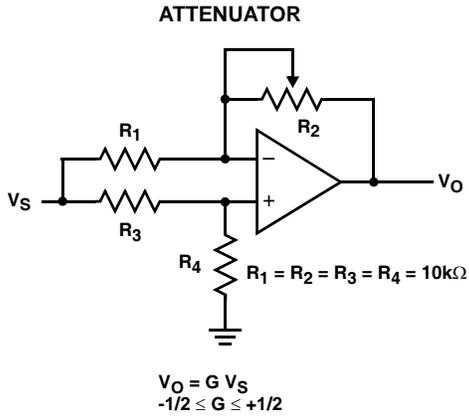
COMPARATOR WITH HYSTERESIS



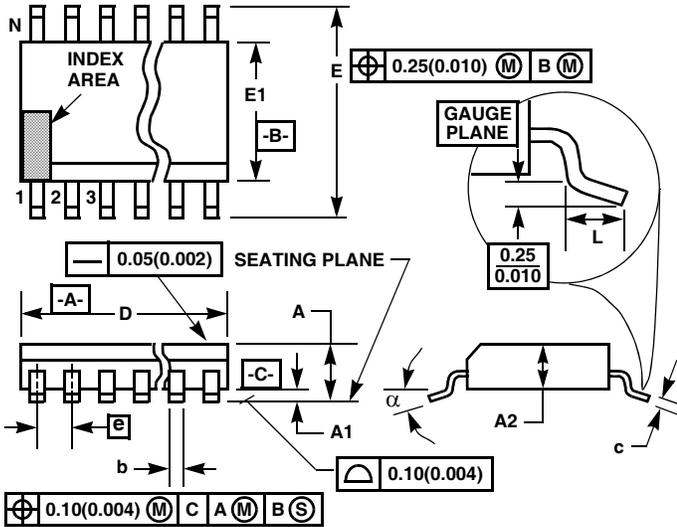
$$V_{UL} = \{R_1/(R_1+R_2)\} V_O(\text{max})$$

$$V_{LL} = \{R_1/(R_1+R_2)\} V_O(\text{min})$$

Application Circuits (Continued)



**Thin Shrink Small Outline Plastic Packages (TSSOP)**



**M14.173**  
**14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
alpha	0°	8°	0°	8°	-

Rev. 2 4/06

**NOTES:**

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)