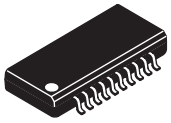
Clock Generator for PowerQUICC and PowerPC Microprocessors and Microcontrollers

MPC9819

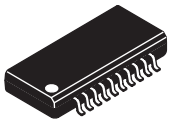
DATA SHEET

The MPC9819 is a PLL-based clock generator specifically designed for Freescale Microprocessor and Microcontroller applications including the PowerPC and PowerQUICC. This device generates the microprocessor input clock and other microprocessor system and bus clocks at any one of four output frequencies. These frequencies include the popular 66- and 133-MHz PCI/X bus frequencies. The device offers five low-skew clock outputs plus three reference outputs. The clock input reference is 25 MHz and may be derived from an external source or by the addition of a 25-MHz crystal to the on-chip crystal oscillator. The extended temperature range of the MPC9819 supports telecommunication and networking requirements.

MICROPROCESSOR CLOCK GENERATOR



SD SUFFIX
20 SSOP PACKAGE
CASE 1461-02



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Features

- 5 LVCMOS outputs for processor and other system circuitry
- 3 Buffered 25-MHz reference clock outputs
- Crystal oscillator or external reference input
- 25-MHz input reference frequency
- Selectable output frequencies include: 66, 100, 125, or 133 MHz
- Low cycle-to-cycle and period jitter
- Package: 20-lead SSOP
- 3.3-V supply
- Supports computing, networking, and telecommunications applications
- Ambient temperature range: –40°C to +85°C

Functional Description

The MPC9819 uses a PLL with a 25-MHz input reference frequency to generate a single bank of five configurable LVCMOS output clocks. The output frequency of this bank is configurable to either 66, 100, 125, or 133 MHz by two FSEL pins. The 25-MHz reference may be either an external frequency source or a 25-MHz crystal. The 25-MHz crystal is directly connected to the XTAL_IN and XTAL_OUT pins with no additional components required. An external reference may be applied to the XTAL_IN pin with the XTAL_OUT pin left floating. The input reference, whether provided by a crystal or an external input, is also directly buffered to a second bank of three LVCMOS outputs. These outputs may be used as the clock source for processor I/O applications such as an Ethernet PHY.

The MPC9819 is packaged in a 20-lead SSOP package.

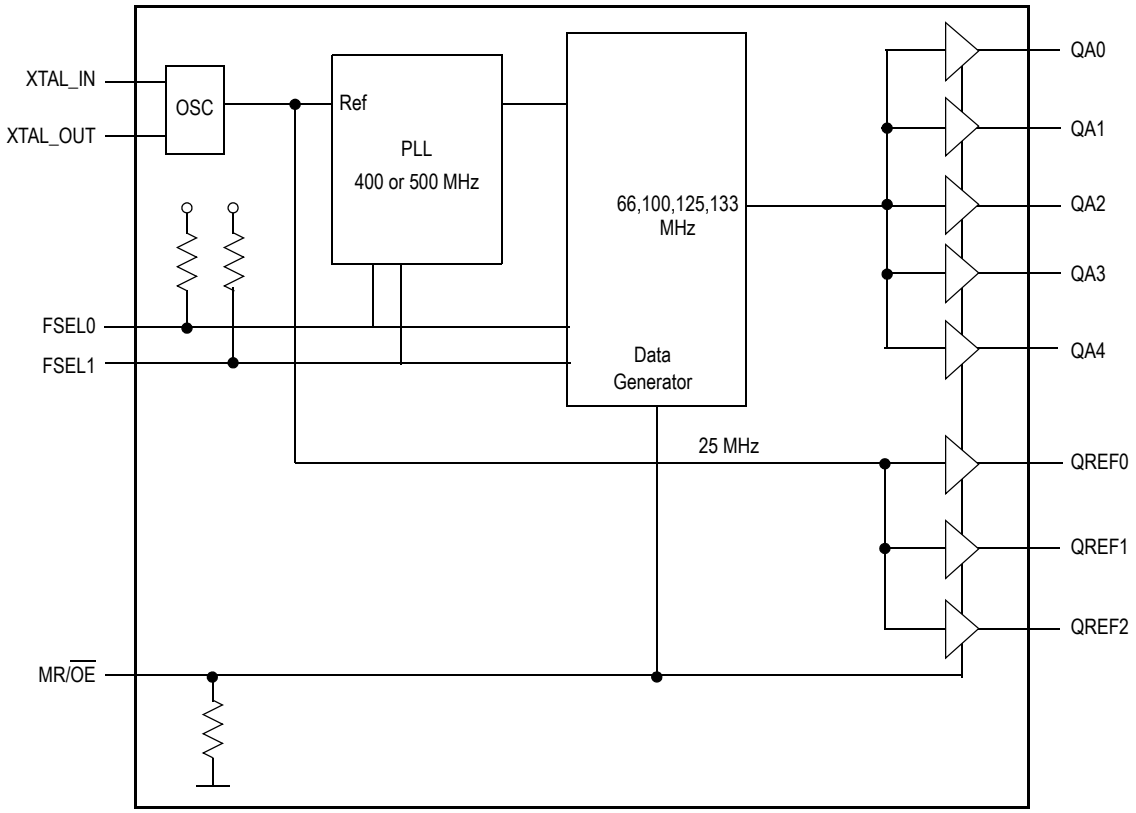


Figure 1. MPC9819 Logic Diagram

Table 1. Pin Configurations

Pin	I/O	Type	Function
QA0, QA1, QA2, QA3, QA4	Output	LVCMOS	Clock Outputs
QREF0, QREF1, QREF2	Output	LVCMOS	Reference Output (25 MHz)
XTAL_IN	Input	LVCMOS	Crystal Oscillator Input Pin
XTAL_OUT	Output	LVCMOS	Crystal Oscillator Output Pin
FSEL0, FSEL1	Input	LVCMOS	Configures Bank A Clock Output Frequency (pull-up)
MR/$\overline{OE}$	Input	LVCMOS	Enables All Outputs (pull-down)
V_{DD}	—	—	3.3-V Supply
GND	—	—	Ground

Table 2. Function Table

Control	Default	00	01	10	11
FSEL0, FSEL1	11	66 MHz	125 MHz	100 MHz	133 MHz

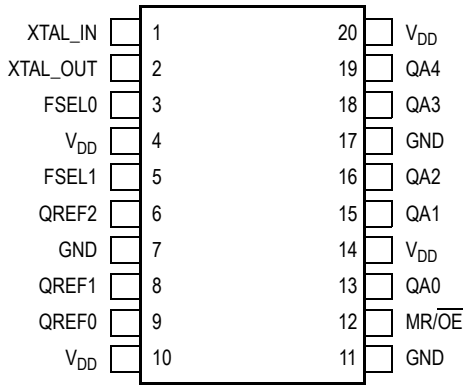


Figure 2. MPC9819 20-Lead SSOP Package Pinout (Top View)

MPC9819 OPERATION

Crystal Oscillator

The MPC9819 features a fully integrated Pierce oscillator to minimize system implementation costs. Other than the addition of a 25-MHz crystal, no external components are required.The crystal selection should be: 25 MHz, parallel resonant type with a load specification of C_L = 10 pF. Crystals with a load specification of C_L = 20 pF may be used, however, the reference frequency may be higher than the specified 25 MHz. Externally supplied capacitors on both the XTAL_IN and XTAL_OUT pins may be used to trim the frequency as desired.

The crystal should be located as close to the MPC9819 XTAL_IN and XTAL_OUT pins as possible to avoid any board level parasitic.

Table 3. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Shunt Capacitance (C_O)	5–7 pF
Load Capacitance (C_L)	10 pF
Equivalent Series Resistance (ESR)	20–60 Ω

Power Supply Bypassing

The MPC9819 should have all V_{DD} pins bypassed with 0.01 capacitors and a minimum of one 1.0 capacitor for the overall package. All capacitors should be located as close to the SSOP pins as possible.

External Clock Source

An external reference source of 25 MHz may be applied to the XTAL_IN pin. In this mode of operation, the XTAL_OUT pin should be left floating.

Table 4. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage	–0.3	3.8	V	
I_{IN}	DC Input Current	—	±20	mA	
I_{OUT}	DC Output Current	—	±75	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage	—	$V_{DD} \div 2$	—	V	
MM	ESD Protection (machine model)	200	—	—	V	
HBM	ESD Protection (human body model)	2000	—	—	V	
LU	Latch-Up Immunity	200	—	—	mA	
C_{IN}	Input Capacitance	—	4	—	pF	Inputs
C_{pd}	Power Dissipation Capacitance	—	8.5	—	pF	
θ_{JA}	Thermal Resistance (junction-to-ambient)	—	80.8	—	°C/W	
T_C	Ambient Temperature	–40		85	°C	

Table 6. DC Characteristics (V_{DD} = 3.3 V ± 5%, T_A = –40° to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage (XTAL_IN)	2.4	—	V_{DD} + 0.3	V	Input threshold = $V_{DD}/2$
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	—	—	0.8	V	LVCMOS
I_{IN}	Input Current(1)	—	—	150	µA	V_{IN} = V_{DDL} or GND
V_{OH}	Output High Voltage	2.4	—	—	V	I_{OH} = –12 mA
V_{OL}	Output Low Voltage	—	—	0.4	V	I_{OL} = 12 mA
Z_{OUT}	Output Impedance	—	14	—	Ω	
I_{DD}	Maximum Supply Current f_A = 66 MHz f_A = 133 MHz	— —	23 32	40 50	mA	25 MHz reference frequency
I_{DDBASE}	Base Supply Current(2) (for dynamic power dissipation calculation)	—	14	—	mA	

1. Inputs have pull-down resistors affecting the input current.
2. $P_D = (V_{DD} * I_{DDBASE}) + 5 (V_{DD}^2) * C_{pd} * f_A$.

Table 7. AC Characteristics[1] [2] (V_{DD} = 3.3 V ± 5%, T_A = –40° to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
Input and Output Timing Specification							
f_{ref}	Input Reference Frequency	25 MHz Input XTAL Input		25 25		MHz MHz	
f_{VCO}	VCO Frequency Range	FSEL0, FSEL1 = 00,01,11 FSEL0, FSEL1 = 10		400 500		MHz MHz	
f_{MCX}	Output Frequency (QAx)	FSEL0, FSEL1 = 00 FSEL0, FSEL1 = 10 FSEL0, FSEL1 = 01 FSEL0, FSEL1 = 11 Output Frequency (QREFx)		66.66 100 125 133.33 25	— — — — —	MHz MHz MHz MHz MHz	PLL locked
f_{refPW}	Reference Input Pulse Width		10	—	—	ns	@ 25 MHz
DC	Output Duty Cycle		45	50	55	%	
f_{out}	Output Frequency Accuracy	Crystal[3] External Reference		— —	100 0	ppm ppm	With recommended crystal see Table 3
PLL Specifications							
BW	PLL Closed Loop Bandwidth[4]			500		kHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	
Skew and Jitter Specifications							
$t_{sk(O)}$	Output-to-Output Skew (within a bank)				75	ps	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter				150	ps	@ 25 MHz Input Reference Q_A output
$t_{JIT(PER)}$	Period Jitter				100	ps	@ 25 MHz Input Reference Q_A output
t_r, t_f	Output Rise/Fall Time				1	ns	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
3. Based upon recommended crystal specifications as outlined in operation section.
4. –3 dB point of PLL transfer characteristics.

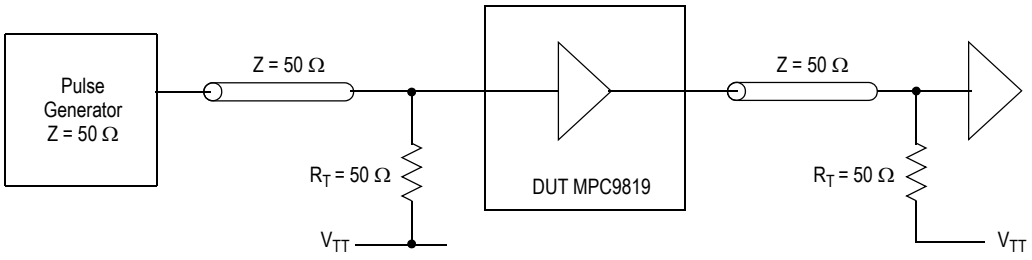
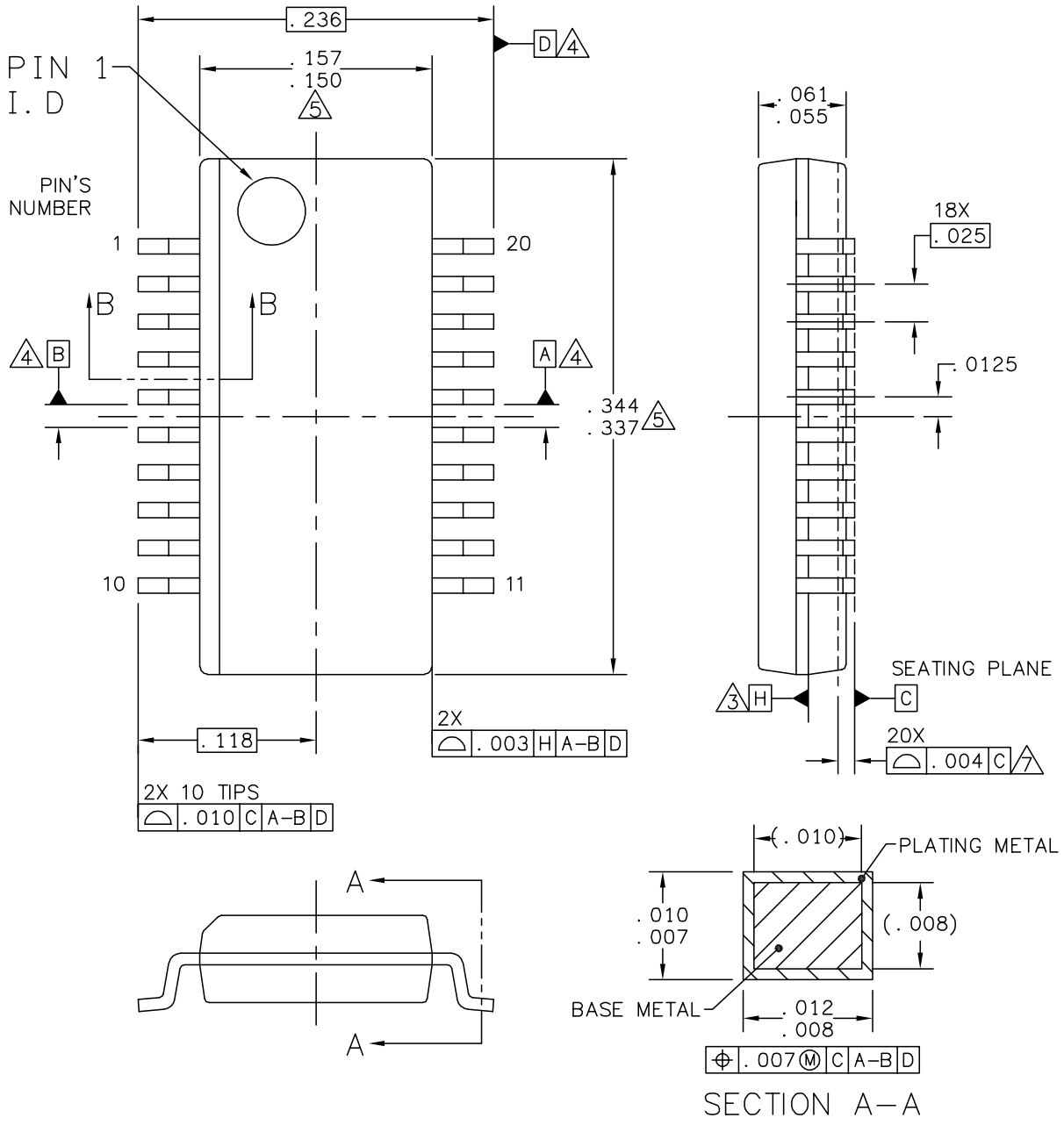


Figure 3. MPC9819 AC Test Reference (LVCMOS Outputs)

Table 8. MPC9819 Pin List

Pin	Description	Pin	Description
1	XTAL_IN	11	GND
2	XTAL_OUT	12	MR/$\overline{OE}$
3	FSEL0	13	QA0
4	V_{DD}	14	V_{DD}
5	FSEL1	15	QA1
6	QREF2	16	QA2
7	GND	17	GND
8	QREF1	18	QA3
9	QREF0	19	QA4
10	V_{DD}	20	V_{DD}

PACKAGE DIMENSIONS



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	CASE NUMBER: 1461-02	20 APR 2005
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CASE 1461-02
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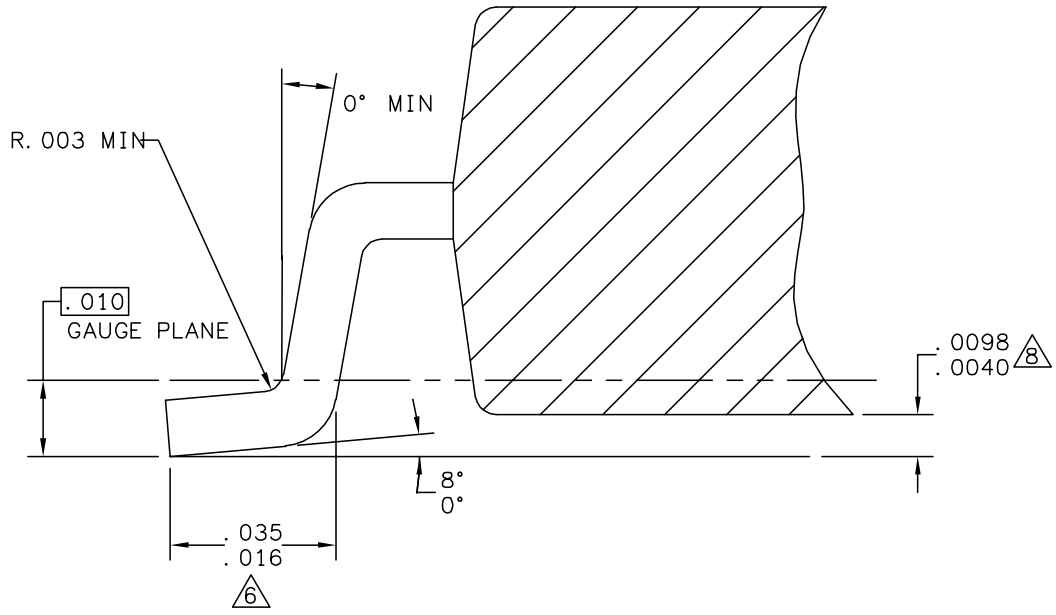
PACKAGE DIMENSIONS



SECTION B–B

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PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUM A, B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES FOR ENDS AND .008 INCHES FOR SIDES.
6. THIS DIMENSION IS LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 INCHES AT SEATING PLANE.
8. THIS DIMENSION IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

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